IBIS Open Forum Minutes

Meeting Date: **November 15, 2017**
Meeting Location: **Taipei, Taiwan**

VOTING MEMBERS AND 2017 PARTICIPANTS

ANSYS	Curtis Clark, Toru Watanabe, Baolong Li, Benson Wei*
Applied Simulation Technology	(Fred Balistreri)
Broadcom	[Bob Miller], (Cathy Liu)
Cadence Design Systems	Brad Brim, Sivaram Chillarige, Debabrata Das Ambrish Varma, Kumar Keshavan, Ken Willis Brad Griffin, Aileen Chen, Lanbing Chen Guoyu Cui, Wei Dai, Zhiyu Guo, Henry He Jinsong Hu, Liang Jiang, Skipper Liang* Ping Liu, Feng Miao, Zuli Qin, Haisan Wang Hui Wang, Yitong Wen, Clark Wu, Janie Wu Susan Wu, Benny Yan, Haidong Zhang Alex Zhao, Zhangmin Zhong, Kent Ho*, Angel Lai* Muse Shao*, Candy Yu*
Cisco Systems	Lei (Jason) Liu, Cassie (Xu) Yan
CST	Stefan Paret, Matthias Troescher, Burkhard Doliwa Danilo Di Febo, Alexander Melkozerov
Ericsson	Zilwan Mahmod, Guohua Wang, Amy X Zhang
GLOBALFOUNDRIES	Steve Parker
Huawei Technologies	Haiping Cao, Wei (Richard) Gu, Zhenxing Hu Peng Huang, Hongxing Jiang, Longfang Lv Luya Ma, Guangjiang Wang, Huichao Weng Zhengrong Xu, Hang (Paul) Yan, Chen (Jeff) Yu Xiaojun (Steve) Zhou, Zhengyi Zhu, Huajun Chen Shengli Wang, Zen Wei
Huawei Technologies (Hisilicon)	Fangxu Yang
IBM	Luis Armenta, Adge Hawes, Greg Edlund
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Michael Mirmak, Hsinho Wu, Eddie Frie Gianni Signorini, Barry Grquinovic Masashi Shimanouchi, Denis Chen*, Jimmy Hsu* Cucumber Lin*, Zoe Li*, Thonas (Yiren) Su*
IO Methodology	Lance Wang*
Keysight Technologies	Radek Biernacki, Pegah Alavi, Fangyi Rao Stephen Slater, Jian Yang, Heidi Barnes Kuen Yew Lam*
Maxim Integrated	Joe Engert, Don Greer, Yan Liang, Hock Seow

Mentor, A Siemens Business (formerly Mentor Graphics)	Arpad Muranyi, Nitin Bhagwath, Praveen Anmula Fadi Deek, Raj Raghuram, Dmitry Smirnov Bruce Yuan, Carlo Bleu, Chao Jiang, David Xu
Micron Technology	Randy Wolff, Justin Butterfield, Jeff Shiba, Harry Shin
NXP	(John Burnett)
Qualcomm	Tim Michalka, Kevin Roselle, Irwin (Zhilong) Xue*
Raytheon	Joseph Aday
SiSoft	Mike LaBonte*, Walter Katz, Todd Westerhoff Steve Silva
Synopsys	Kevin Li, Ted Mido, John Ellis, Scott Wedge Wonsae Sim, Xuefeng Chen, Jinghua Huang Yijiang Huang, Deng Shi, Yuyang Wang
Teraspeed Labs	Bob Ross
Xilinx	(Raymond Anderson)
ZTE Corporation	Rongxing Ban, Xinjian Chen, Fengling Gao Tao Guo, Lili Wei, Yangye Yu, Shunlin Zhu
Zuken	Ralf Bruening, Michael Schaeder, Alfonso Gambuzza

OTHER PARTICIPANTS IN 2017

Accton	Raul Lozano
ADLINK Technology	Alvis Hsu*
Amphenol	Fred Shen, Holly Wang
ASR Microelectronics	Lili Dia, Shulong Wu
ASRock Rack	Eric Chien*
ASUS	Nick Huang*, Bin-chyi Tseng, Andrew Huang*
Aurora System	Murong Lu, Jiaxin Sun
Avant Technology	Jyam Huang*, Chloe Yang*
BasiCAE	Kiki Li, Darcy Liu, July Tao, Lisa Wu
Brite Semiconductor	Haonan Wang
Celestica	Wilson Chen, Sophia Feng, Lurker Li Weiqing Liiu, Vincent Wen
Continental AG	Stefanie Schatt
eASIC	David Banas
Edadoc	Deheng Chen, Bruce (Jun) Wu, Hong Zhang
Extreme Networks	Bob Haller
Flextronics	Renjun Sun
Foxconn Electronics	Gino (Chunjen) Chen*, Joe (Chienhusn) Chen* Alex Tang*
Ghent University	Paolo Manfredi
H3C	Xinming Hu
Hamburg University of Technology	Torsten Revschel, Torsen Wendt
Hewlett Packard Enterprise	Passor Ho*, Corey Huang*, Hellen Lo*
IdemWorks	Michelangelo Bandinu
Ilia State University	Nana Dikhaminjia

Independent	Dian Yang, Lawrence Der
Inspur Technologies	Josh Chen*, Dane Huang*, Nieves Lee*, Ian Yu*
Institute for Information Industry	Joseph Lang*
Inventec	Ian Chen*, Ellen Tseng*
John Baprawski, Inc.	John Baprawski
KEI Systems	Shinichi Maeda
Lattice Semiconductor	Maryam Shahbazi, Dinh Tran
Leading Edge	Pietro Vergine
Lenovo Group	Shaogao Zheng, Paul Chu*, John Lin*, Alan Sun*
Lexington Consulting	Mike Barg
Lite-On Technology	Sam (Dongru) Lyu*
Missouri Science and Technology EMC Lab	Giorgi Maghlakelidze
Mostec	Nelly Li, Clark Zhang
Nanya Technology Corp.	Chingfeng Chen*, Chiwei Chen*, Andy (Weishen) Chih* Minlun Lan*, George Lee*, Allen Ye*
Novatek	Jerrcik Cheng*, Vincent Lin*
Pegatron Corp.	Melissa Huang*, James Lee*
Politecnico di Torino	Claudio Siviero, Stefano Grivet-Talocia, Igor Stievano
Quanta Computer	Eriksson Chuang*, Aaron Lee*, Scott Lee*, Jerry Syue*
Rockchip	Junming Shi
SAE-ITC	(Thomas Munns), Jose Godoy
SAIC Motor Corp.	Weng Yang
Samsung	Jung Hwan Choi
Shanghai Fudan Microelectronics Group	Zhenghui Chen, Liu Lu Fang, Xin Li, Yuezhi Liu Xiao Lei Luo, Canghai Tang
Shinewave	Nike Yang*
Signal Metrics	Ron Olisar
SMICS	Sheral (Xuejiao) Qi
SPISim (Peace Giant Corp.)	Wei-hsing Huang*, Walter Huang*
Spreadtrum Communications	Junyong Deng, Ganyue Wang, Shiqing Si
Stanford University	Tom Lee
STMicroelectronics	Fabio Brina, Olivier Bayet
Tatung Technology	Barry Chen*, Daniel Chen*
Teledyne Lecroy	Facun Li, Yifeng Wu
TopBrain	Ye Li
Toshiba	Yasuki Torigoshi
U-Creative	Amber Wu
Université Blaise Pascal	Mohamed Toure
Université de Bretagne Occidentale	Mihai Telescu
VIA Labs	Shengyuan Lee*
VIA Technologies	Terence Hsieh*, Justin Hsu*
Winbond	Yumin Hou*, Albert Lee*
Xpeedic	Tuhui Gui
Yi Chuan Technology	Wei Ming Lu

Zhaoxin	Liam Li, Eddrick Wang
Zhejiang Uniview Technologies	Busen Cai, Jilun Fang

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
November 17, 2017	Tokyo IBIS Summit – no teleconference	
December 1, 2017	624 999 876	IBISfriday11

For teleconference dial-in information, use the password at the following website:

http://tinyurl.com/zeulerr

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The Asian IBIS Summit took place on Wednesday, November 15, 2017 at the Sherwood Hotel in Taipei. About 62 people representing 28 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.ibis.org/summits/nov17b/

Mike LaBonte welcomed participants on behalf of the IBIS Open Forum and convened the meeting.

Mike continued by thanking all the co-sponsors including IO Methodology, Peace Giant Company (SPISim), and Synopsys.

IBIS UPDATE

Mike LaBonte (SiSoft, USA)

Mike LaBonte detailed the activities of the IBIS Open Forum over the past year. He showed a

possible timeline for the passage of IBIS 7.0, as well as the status of all current BIRDs that may or may not be part of IBIS 7.0. Mike gave a brief summary of the changes in three BIRDs likely to become part of IBIS 7.0.

A comment was made about the lack of defined message protocols for BIRD147, that they should be defined because most PCIe analyses involve a TX and RX from different vendors. Mike responded that the protocols would be posted on the IBIS website, and this would allow for quicker implementation than if we were to wait for a new IBIS specification.

IBIS INTERCONNECT MODELING USING IBIS-ISS AND TOUCHSTONE

Michael Mirmak (Intel Corporation, USA)
[Presented by Mike LaBonte (SiSoft, USA)]

Mike LaBonte presented on behalf of Michael Mirmak. The concepts found in BIRD189.x were summarized. The new format is an improvement over existing IBIS [Define Package Model] in several ways, allowing for both cascaded model sections as well as coupling in any combination. The Touchstone format and the ability to separately model buffer to pad and pad to pin connections would be helpful for the high speed signals used today. The addition of die pads for rails allowed for circuit topologies suitable for modeling the power and ground rails in chips.

LEVERAGING IBIS CAPABILITIES FOR MULTI-GIGABIT INTERFACES

Ken Willis (Cadence Design Systems, USA)
[Presented by Skipper Liang (Cadence Design Systems, ROC)]

Skipper Liang noted that the presentation related to the EDI CON paper “Signal Integrity Methodology for Double-Digit Multi-Gigabit Interfaces”. Use of Spice [External Model]s makes it easy to write simple parameterized Spice subcircuits for I/O buffers when IBIS availability does not align with a project schedule. The EDA tool user can select parameter values from a GUI using the [External Model] “Parameters” and “Converter_Parameters” syntax.

Skipper described the typical modules of an Rx AMI model including gain, CTLE and DFE. These modules typically adapt at different rates, and the initial modules like gain and CTLE usually adapt more slowly than the DFE. He showed how adjusting the adaptation algorithms of the AMI model led to better adaptation and a significant difference in final eye height. Skipper showed details of the backchannel flow from BIRD147. He went on to show the application of IBIS-AMI modeling and simulation techniques to DDR4/5. Cadence developed an IBIS-AMI model for a DDR4 controller that included equalization. He showed correlation between an IBIS-AMI model-based channel simulation and a transistor-level circuit simulation.

COMPARISON OF TIME DOMAIN AND STATISTICAL IBIS-AMI ANALYSES

Mike LaBonte (SiSoft, USA)

Mike LaBonte noted that a dual IBIS-AMI model has an AMI file with GetWave_Exists set to true and Init_Returns_Impulse set to true. This is the best option for running both time domain and statistical analysis. Mike reviewed some fundamentals of channel simulation including inputs

and outputs of time-domain and statistical simulations, channel impairments, step response and pulse response analysis, eye height prediction from pulse response cursor analysis, and methods for all the ISI in a given channel. He then discussed jitter and noise impairments and equalization methods. He concluded that IBIS-AMI time domain simulation with AMI_GetWave can model non-linear effects such as DFE and saturation, but it can be impossible to simulate enough bits to prove the low BER requirements of some technologies. IBIS-AMI statistical simulation can quickly evaluate low BER, but it cannot see time-variant effects such as DFE and saturation. So, dual IBIS-AMI models are required.

CHARACTERIZING AND MODELING OF A LINEAR CTE

Skipper Liang (Cadence Design Systems, ROC)

Skipper Liang noted that when creating an IBIS-AMI model for an RX, it is necessary to divide the buffer between the analog part and the algorithmic part. He showed a method in which modelers no longer need to model the RX IBIS (analog part) model. A dummy IBIS model is used, and the buffer characteristics are put in the AMI model. The CTE is modeled using a step response time domain characterization. The method is only valid when the equalizer is purely linear.

USING DATA FILES FOR IBIS-AMI MODELS

Lance Wang (IO Methodology, USA)

Lance Wang noted that creating IBIS-AMI models can require making executables for many platforms and OS's. He presented the concept of creating a single DLL/SO file that references external data files, allowing reuse of code for different transceivers by only modifying the data file. If using data files, the DLL/SO contains AMI standard functions, data processing functions and data file processing functions that might include decryption of the data file. The data file can contain code, data, parameters, and it could be encrypted. With this approach, the DLL/SO file could be developed by professional programmers and used for many different data files. The data file can then be created by designers or modelers and would not require compilation. A test case was shown that pointed to the data file through a Model_Specific parameter.

IBIS-AMI MODELING USING SCRIPTS AND SPICE MODELS

Wei-hsing Huang (SPISim, USA)

Wei-hsing Huang investigated the creation of IBIS-AMI models using scripting languages and existing SPICE models. The flow could reduce AMI modeling time and serve as an intermediate step towards full C/C++ implementation. Considerations include performance and the redistribution and use of models that could rely on an external SPICE simulator.

CLOSING REMARKS

Mike LaBonte thanked the co-sponsors, presenters and attendees for their participation and support.

NEXT MEETING

The next IBIS Open Forum teleconference meeting will be held December 1, 2017. The following IBIS Open Forum teleconference meeting is tentatively scheduled on December 15, 2017.

The Asian IBIS Summit in Tokyo will be held November 17, 2017. No teleconference will be available for the Summit meeting.

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NOTES

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This meeting was conducted in accordance with ANSI guidance.

All inquiries may be sent to info@ibis.org. Examples of inquiries are:

- To obtain general information about IBIS.
- To ask specific questions for individual response.
- To subscribe to the official ibis@freelists.org and/or ibis-users@freelists.org email lists (formerly ibis@eda.org and ibis-users@eda.org).
- To subscribe to one of the task group email lists: ibis-macro@freelists.org, ibis-interconn@freelists.org, or ibis-quality@freelists.org.
- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.
- To report bugs or request enhancements to the free software tools: ibischk6, tschk2, icmchk1, s2ibis, s2ibis2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.ibis.org/bugs/ibischk/
http://www.ibis.org/ bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.ibis.org/bugs/tschk/
http://www.ibis.org/bugs/tschk/bugform.txt

The BUG Report Form for icmchk resides along with reported BUGs at:

http://www.ibis.org/bugs/icmchk/
http://www.ibis.org/bugs/icmchk/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.ibis.org/bugs/s2ibis/bugs2i.txt
http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt
http://www.ibis.org/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.ibis.org/

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

http://www.ibis.org/directory.html

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SAE STANDARDS BALLOT VOTING STATUS

Organization	Interest Category	Standards Ballot Voting Status	October 18, 2017	October 27, 2017	November 13, 2017	November 15, 2017
ANSYS	User	Active	X	X	-	X
Applied Simulation Technology	User	Inactive	-	-	-	-
Broadcom Ltd.	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Active	-	-	X	X
Cisco Systems	User	Inactive	-	-	X	-
CST	User	Inactive	-	-	-	-
Ericsson	Producer	Inactive	-	-	X	-
GLOBALFOUNDRIES	Producer	Inactive	-	X	-	-
Huawei Technologies	Producer	Inactive	-	-	X	-
IBM	Producer	Inactive	-	-	-	-
Infineon Technologies AG	Producer	Inactive	-	X	-	-
Intel Corp.	Producer	Active	X	X	-	X
IO Methodology	User	Active	-	X	X	X
Keysight Technologies	User	Active	X	X	-	X
Maxim Integrated	Producer	Inactive	-	-	-	-
Mentor, A Siemens Business	User	Active	X	X	X	-
Micron Technology	Producer	Inactive	-	X	-	-
NXP	Producer	Inactive	-	-	-	-
Qualcomm	Producer	Inactive	X	-	-	X
Raytheon	User	Inactive	-	-	-	-
SiSoft	User	Active	-	X	X	X
Synopsys	User	Active	X	X	X	-
Teraspeed Labs	General Interest	Inactive	X	X	-	-
Xilinx	Producer	Inactive	-	-	-	-
ZTE Corp.	User	Inactive	-	-	X	-
Zuken	User	Inactive	-	-	-	-

Criteria for SAE member in good standing:

- Must attend two consecutive meetings to establish voting membership
- Membership dues current
- Must not miss two consecutive meetings

Interest categories associated with SAE standards ballot voting are:

- Users - members that utilize electronic equipment to provide services to an end user.
- Producers - members that supply electronic equipment.
- General Interest - members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations and associations, and/or consumers.