

**IBIS Open Forum Minutes**

Meeting Date: **October 18, 2017**

Meeting Location: **EPEPS 2017 IBIS Summit, San Jose, California, USA**

**VOTING MEMBERS AND 2017 PARTICIPANTS**

ANSYS Curtis Clark, Toru Watanabe, Baolong Li\*

Applied Simulation Technology (Fred Balistreri)

Broadcom [Bob Miller], (Cathy Liu)

Cadence Design Systems Brad Brim, Sivaram Chillarige, Debabrata Das

Ambrish Varma, Kumar Keshavan, Ken Willis

Brad Griffin

Cisco Systems (Bidyut Sen)

CST Stefan Paret, Matthias Troescher, Burkhard Doliwa

Danilo Di Febo, Alexander Melkozerov

Ericsson Zilwan Mahmod

GLOBALFOUNDRIES Steve Parker

Huawei Technologies (Jinjun Li)

IBM Luis Armenta, Adge Hawes, Greg Edlund

Infineon Technologies AG (Christian Sporrer)

Intel Corporation Michael Mirmak, Hsinho Wu\*, Eddie Frie

Gianni Signorini, Barry Grquinovic

Masashi Shimanouchi\*

IO Methodology Lance Wang

Keysight Technologies Radek Biernacki, Pegah Alavi\*, Fangyi Rao

Stephen Slater\*, Jian Yang, Heidi Barnes\*

Maxim Integrated Joe Engert, Don Greer, Yan Liang, Hock Seow

Mentor, A Siemens Business Arpad Muranyi, Nitin Bhagwath, Praveen Anmula

(formerly Mentor Graphics) Fadi Deek, Raj Raghuram\*, Dmitry Smirnov

Bruce Yuan, Carlo Bleu

Micron Technology Randy Wolff, Justin Butterfield, Jeff Shiba, Harry Shin

NXP (John Burnett)

Qualcomm Tim Michalka, Kevin Roselle\*

Raytheon Joseph Aday

SiSoft Mike LaBonte, Walter Katz, Todd Westerhoff

Steve Silva

Synopsys Kevin Li, Ted Mido\*, John Ellis, Scott Wedge

Wonsae Sim\*

Teraspeed Labs Bob Ross\*

Xilinx (Raymond Anderson)

ZTE Corporation (Shunlin Zhu)

Zuken Ralf Bruening, Michael Schaeder, Alfonso Gambuzza

**OTHER PARTICIPANTS IN 2017**

Accton Raul Lozano

ASUS Nick Huang, Bin-chyi Tseng

Continental AG Stefanie Schatt

eASIC David Banas

Extreme Networks Bob Haller

Ghent University Paolo Manfredi

Hamburg University of Technology Torsten Revschel, Torsen Wendt

IdemWorks Michelangelo Bandinu

Ilia State University Nana Dikhaminjia\*

Independent Dian Yang, Lawrence Der

John Baprawski, Inc. John Baprawski

KEI Systems Shinichi Maeda

Lattice Semiconductor Maryam Shahbazi, Dinh Tran

Leading Edge Pietro Vergine

Lexington Consulting Mike Barg

Missouri Science and Technology Giorgi Maghlakelidze\*

EMC Lab

Politecnico di Torino Claudio Siviero, Stefano Grivet-Talocia, Igor Stievano

SAE International (Thomas Munns)

Samsung Jung Hwan Choi\*

Signal Metrics Ron Olisar

SPISim Wei-hsing Huang\*

Stanford University Tom Lee\*

STMicroelectronics Fabio Brina, Olivier Bayet

Toshiba Yasuki Torigoshi

Université Blaise Pascal Mohamed Toure

Université de Bretagne Occidentale Mihai Telescu

In the list above, attendees at the meeting are indicated by \*. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

**UPCOMING MEETINGS**

The bridge numbers for future IBIS teleconferences are as follows:

Date Meeting Number Meeting Password

October 27, 2017 624 999 876 IBISfriday11

November 13, 2017 Asian IBIS Summit (Shanghai) – no teleconference

November 15, 2017 Asian IBIS Summit (Taipei) – no teleconference

November 17, 2017 Asian IBIS Summit (Tokyo) – no teleconference

For teleconference dial-in information, use the password at the following website:

<http://tinyurl.com/zeulerr>

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

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**OFFICIAL OPENING**

The IBIS Open Forum Summit was held in the DoubleTree Hilton Hotel after the EPEPS 2017 workshop. About 16 people representing 12 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

<http://www.ibis.org/summits/oct17/>

Bob Ross welcomed everyone to the Summit, opening the meeting at 1:15 p.m. He thanked the sponsors including EPEPS, Keysight Technologies, and Synopsys. Bob noted that Keysight provided the projector in spite of fire-related difficulties at their Santa Rosa, California location. Everyone in the room introduced themselves.

**KEYNOTE SPEECH**

**GO BIG OR GO HOME: THE FIRST TRANSATLANTIC TELEGRAPH CABLE AND THE BIRTH OF ELECTRICAL ENGINEERING**

Tom Lee (Stanford University)

Bob Ross introduced Tom Lee by displaying his biography. Tom joined Stanford in 1994. He has extensive academic accomplishments, several awards, and significant industrial experience. Tom holds over 60 patents and has authored textbooks. He owns many oscilloscopes and electronic components.

Tom’s biography and abstract are uploaded. Per Tom’s request, the presentation itself is not publicly distributed because it is used in many other settings and for student orientation. Tom’s abstract plus some additional details are presented here.

"Abstract: Electrical engineers are the children of a failure so traumatic that we don't even talk about it. American paper magnate Cyrus West Field wanted to span the Atlantic in the 1850s with a telegraph cable; it was the Victorian era's equivalent of shooting for the moon. Amplifiers would not exist for another half-century, so success would require mastery of a number of complex technical disciplines. Regrettably, the project's technical head was a medical doctor. A British board of inquiry convened to assess the resulting failures noted that the electrical arts lacked even a basic vocabulary to describe the failure. William Thomson was eventually named the new head of the project, and final success followed in 1866. The volt, ohm and ampere were formally defined shortly thereafter and the profession of electrical engineering was born. Thomson -- arguably the first professional electrical engineer -- became Lord Kelvin, and EEs have been busy making mischief ever since."

Tom added many interesting details. Based on Moore's law, many transistors now support five million cell phones sold daily. This contributes to producing 100 TPA every year (100 transistors per ant on earth annually). The story of the transatlantic cable reveals that the secret to Greatness is a function of Money, Ignorance, Luck, and Craziness, as expressed in the formula G = f{M,I,L,C}. In the path to greatness, Murphy's law also seems to prevail. Luck may also prevail as new technologies emerge at convenient times.

One technology was the discovery of Gutta-Percha, a natural substance from trees mainly in Singapore/Malaysia. It is a thermoplastic, chemically stable, and has tolerance of water. This was useful to protect the cable from corrosion. Another key technology was the highly sensitive mirror galvanometer by Lord Kelvin to detect small voltages. Magnets canceled out the earth's magnetic field.

The transmission data rate target for the transatlantic cable was 1-2 words per minute, but the first cable in 1857/1858 achieved only 0.1 words per minute. Many problems arose, and the cable went silent after 23 days. It took 16 hours to transmit a 98-word message perhaps with the operator using context to fill in the somewhat garbled transmission. Perhaps this was a first application of what would be done today by artificial intelligence. After much debate, a new, heavier cable was proposed. However, it required a five times bigger ship than had currently existed to lay it. As luck would have it, a new class of ships were being constructed to hold enough fuel to travel non-stop from England to Australia.

The overall cable properties were length of 3000 nautical miles, series resistance of 8 kohms, shunt capacitance of 740 uF, and shunt resistance of 200 kohms. This provided an RC time constant of 6 seconds. Five words per minute could be transmitted, exceeding the original target. The cable snapped several times before finally being placed in service in 1866. By 1891, more cables formed a global communications network.

Many legacies emerged from Cyrus West Field’s initial money, ignorance, luck and craziness. They include the unit of resistance, the electrical engineering profession emerging as the Institution of Electrical Engineers, and several EE degree programs at universities in the 1880s. The cable descendants include networks that contribute to 250,000 texts per second.

The full story of successes and failures illustrates all aspects of the bottom line: “May you always have as much MILC as you need.”

Bob asked what the electrical transmission line characteristics were, and Tom responded that it had characteristics similar to RG-58.

**IBIS UPDATE**

Mike LaBonte (SiSoft)

[Presented by Bob Ross (Teraspeed Labs)]

Bob Ross showed the 26 current members of IBIS, the IBIS officers, and he detailed the many IBIS Open Forum and task group meetings and Summits. The parent organization of the IBIS Open Forum is the SAE Industry Technologies Consortia. IBIS version 7.0 is under development, and it has been just over two years since version 6.1 was ratified. He discussed a possible timeline for release of IBIS version 7.0 and a list of BIRDs to be included and excluded. He gave an overview of some prominent BIRDs targeted for inclusion in IBIS version 7.0 including BIRD147 for backchannel support, BIRD158 for AMI Touchstone analog buffer model support, BIRD188 for expanded Rx noise support for AMI, and BIRD189 for interconnect modeling using IBIS-ISS and Touchstone.

Nana Dikhaminjia asked about two different back-channel proposals that had been discussed in the past. Pegah Alavi responded that the proposals have been merged into the current one. Bob added that the combined proposal is much simpler and defines only five new parameters for IBIS-AMI.

**IBIS-AMI MODELING USING SCRIPTS AND SPICE MODELS**

Wei-hsing Huang (SPISim)

Wei-hsing provided a motivation and IBIS-AMI background for using scripts and existing SPICE models to overcome some existing barriers. Python and other scripting languages can be used. Several open-source SPICE simulators that support API/shared libraries are available. Wei-hsing showed development flows using scripts. He also showed a development flow with SPICE that can be used to dynamically generate piece-wise linear (PWL) inputs based on a high-Z assumption.

Ted Mido and others asked whether the models could be used in commercial EDA tools. Wei-hsing responded yes, but he added that these models might be used for initial quick prototyping. The models are created assuming LTI behavior.

**EQUALIZATIONS FOR MULTI-LEVEL SIGNAL**

Nana Dikhaminjia, Ilia State University

Nana Dikhaminjia presented a fast, improved optimization algorithm for MMSE (minimum mean squared error) to recover signals using equalizers such as FFE (feed forward equalizer), CTE (continuous time equalizer), and DFE (decision feedback equalizer). She displayed the equations for DFE. For best results, the desired training signal should be normalized to the maximum of the un-equalized signal. The optimization algorithm will always converge. Nana showed the equations and displayed results for NRZ improvements versus several different parameters such as eye-opening, data rates, number of taps, loss, and FFE-DFE combination.

Nana also presented some formulas and results for PAM-4 improvement with DFE. She also showed PAM-4 de-emphasis, PAM-4 equalization of a signal by bit and by symbol, and showed some comparisons. She provided a number of conclusions. One conclusion is that when the signal is not heavily emphasized, the eye-height is significantly improved. But a limitation is that the compensation value is proportional to the C1 tap strength, causing PAM-4 signals to overshoot and to close the eye by mixing with each other.

In the discussion, Nana concluded that the optimization approach can be used to find and produce better tap coefficients.

**INTERCONNECT MODELING USING IBIS-ISS AND TOUCHSTONE**

Michael Mirmak (Intel Corporation)

[Presented by Bob Ross (Teraspeed Labs)]

Bob Ross stated that BIRD189.x by the Interconnect Task Group is available for review. The BIRD is intended for IBIS Version 7.0, and its purpose is to improve package and on-die interconnect models by supporting IBIS-ISS and Touchstone models. This includes models of both I/O and supply connections. An optional die pad interface between pins and buffers is introduced. A one-to-one path connection is assumed for I/Os. Supply rails can have multiple terminals and be merged at the various interfaces.

Bob showed some details of new keywords and subparameters as well as syntax examples. Some changes include [Interconnect Model Set Group] and the subparameter File\_TS0 (along with File\_TS for declaring a global ground or an explicit rail as a Touchstone reference. The rules have changed for unused ports (or nodes in IBIS-ISS). For IBIS-ISS, unused nodes are illegal. There is still discussion concerning the options of Open or Reference for terminating unused ports in Touchstone files. More revisions are in progress from the Interconnect Task Group.

A question was asked if Touchstone references for each port can be supported. Bob responded that this can be supported by the IBIS-ISS format with an S model.

**INTERCONNECT MODELS: NEW FEATURES FOR RAIL CONNECTIONS**

Bob Ross (Teraspeed Labs)

Bob Ross mentioned that the main point of this presentation is to introduce some features that are planned for Version 7.0 that have not been discussed. They involve extended ways to define bus\_label entries used in [Pin Mapping] and for terminals in the BIRD189.x.

Existing [Pin Mapping] support requires that all rail (POWER, GND) model pin\_names be listed. BIRD182 gives meaning to the [Pin] signal\_name entry for rails, and a missing pin\_name entry in [Pin Mapping] still can provide a bus\_label = signal\_name entry for that missing pin\_name. Pending BIRD189 also explicitly defines with a new [Bus Label] keyword a bus\_label entry for a given signal\_name value. Finally, the new [Die Supply Pads] keyword, used to define pad\_names on a one-to-many, or many-to-one basis, associates pad\_names with signal\_names and with bus\_labels. The later association can provide another way to define bus\_label entries that are terminals in interconnect models, but not necessarily used in [Pin Mapping].

Bob summarized these features by showing a simplified example that could combine all four ways to enter bus\_labels. Any combination of these methods can be used.

**CLOSING REMARKS**

Bob Ross again thanked the sponsors EPEPS, Keysight Technologies, and Synopsys and the presenters and everyone for attending.

The meeting concluded at approximately 5:15 PM.

**NEXT MEETING**

The next IBIS Open Forum teleconference meeting is scheduled for October 27, 2017. A vote on holding an IBIS Summit meeting at DesignCon 2018 is scheduled. Votes on BIRD158.6 and BIRD161.1 are also scheduled. The following IBIS Open Forum teleconference meeting is tentatively scheduled on December 1, 2017.

The Asian IBIS Summit in Shanghai will be held November 13, 2017. The Asian IBIS Summit in Taipei will be held November 15, 2017. The Asian IBIS Summit in Tokyo will be held November 17, 2017. No teleconferences will be available for the Summit meetings.

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**NOTES**

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This meeting was conducted in accordance with ANSI guidance.

All inquiries may be sent to [info@ibis.org](mailto:info@ibis.org). Examples of inquiries are:

* To obtain general information about IBIS.
* To ask specific questions for individual response.
* To subscribe to the official [ibis@freelists.org](mailto:ibis@freelists.org) and/or [ibis-users@freelists.org](mailto:ibis-users@freelists.org) email lists (formerly [ibis@eda.org](mailto:ibis@eda.org) and [ibis-users@eda.org](mailto:ibis-users@eda.org)).
* To subscribe to one of the task group email lists: [ibis-macro@freelists.org](mailto:ibis-macro@freelists.org), [ibis-interconn@freelists.org](mailto:ibis-interconn@freelists.org), or [ibis-quality@freelists.org](mailto:ibis-quality@freelists.org).
* To inquire about joining the IBIS Open Forum as a voting Member.
* To purchase a license for the IBIS parser source code.
* To report bugs or request enhancements to the free software tools: ibischk6, tschk2, icmchk1, s2ibis, s2ibis2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

<http://www.ibis.org/bugs/ibischk/>   
[http://www.ibis.org/ bugs/ibischk/bugform.txt](http://www.ibis.org/%20bugs/ibischk/bugform.txt)

The BUG Report Form for tschk2 resides along with reported BUGs at:

<http://www.ibis.org/bugs/tschk/>   
<http://www.ibis.org/bugs/tschk/bugform.txt>

The BUG Report Form for icmchk resides along with reported BUGs at:

<http://www.ibis.org/bugs/icmchk/>   
<http://www.ibis.org/bugs/icmchk/icm_bugform.txt>

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

<http://www.ibis.org/bugs/s2ibis/bugs2i.txt>   
<http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt>   
<http://www.ibis.org/bugs/s2iplt/bugsplt.txt>

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

<http://www.ibis.org/>

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

<http://www.ibis.org/directory.html>

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**SAE STANDARDS BALLOT VOTING STATUS**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Organization** | **Interest Category** | **Standards Ballot Voting Status** | **September 13, 2017** | **September 15, 2017** | **October 6, 2017** | **October 18, 2017** |
| ANSYS | User | Active | X | - | X | X |
| Applied Simulation Technology | User | Inactive | - | - | - | - |
| Broadcom Ltd. | Producer | Inactive | - | - | X | - |
| Cadence Design Systems | User | Active | X | - | X | - |
| Cisco Systems | User | Inactive | - | - | - | - |
| CST | User | Inactive | - | - | X | - |
| Ericsson | Producer | Inactive | - | - | - | - |
| GLOBALFOUNDRIES | Producer | Inactive | - | - | X | - |
| Huawei Technologies | Producer | Inactive | - | - | - | - |
| IBM | Producer | Inactive | - | - | X | - |
| Infineon Technologies AG | Producer | Inactive | - | - | X | - |
| Intel Corp. | Producer | Active | - | X | X | X |
| IO Methodology | User | Active | X | X | X | - |
| Keysight Technologies | User | Active | - | X | X | X |
| Maxim Integrated | Producer | Inactive | - | - | - | - |
| Mentor, A Siemens Business | User | Active | - | X | X | X |
| Micron Technology | Producer | Active | X | X | X | - |
| NXP | Producer | Inactive | - | - | X | - |
| Qualcomm | Producer | Inactive | - | - | - | X |
| Raytheon | User | Inactive | - | - | X | - |
| SiSoft | User | Active | X | X | X | - |
| Synopsys | User | Active | - | X | X | X |
| Teraspeed Labs | General Interest | Active | - | X | X | X |
| Xilinx | Producer | Inactive | - | - | X | - |
| ZTE | User | Inactive | - | - | - | - |
| Zuken | User | Inactive | - | - | X | - |

Criteria for SAE member in good standing:

* Must attend two consecutive meetings to establish voting membership
* Membership dues current
* Must not miss two consecutive meetings

Interest categories associated with SAE standards ballot voting are:

* Users - members that utilize electronic equipment to provide services to an end user.
* Producers - members that supply electronic equipment.
* General Interest - members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations and associations, and/or consumers.