IBIS Open Forum Minutes

Meeting Date: **November 11, 2016**
Meeting Location: **Shanghai, China**

VOTING MEMBERS AND 2016 PARTICIPANTS

ANSYS	Curtis Clark, Toru Watanabe
Broadcom (Avago Technologies)	Bob Miller
Cadence Design Systems	Ken Willis, Brad Brim, Aileen Chen*, Lanbing Chen* Zhiyu Guo*, Mohan Jiang*, Rachel Li*, Ping Liu* Haisan Wang*, Yitong Wen*, Clark Wu*, Dingru Xiao* Benny Yan*, Haidong Zhang*, Wenjian Zhang* Zhangmin Zhong*, Hui Wang*, Jinsong Hu*, Wei Dai* Rong Zhang*
Cisco Systems	Giuseppi Selli, Brian Baek, Hannah Bian*, Tonghao Ding* Amanda Liao*, Cassie Yan*
CST	Stefan Paret
Ericsson	Anders Ekholm*, David Zhang*, Zilwan Mahmod Guohua Wang*
GLOBALFOUNDRIES	Steve Parker
Huawei Technologies	Yuanbin Cai*, Haiping Cao*, Zhenxing Hu*, Peng Huang* Xusheng Liu*, Longfang Lv*, Guanjiang Wang* Chen Yu*, Cheng Zhang*, Gezi Zhang*, Zhengyi Zhu* Fangxu Yang*, Huajun Chen*, Xiao Peng* Zhengrong Xu*, Xianbiao Wang*, Lin Shi* Hongcheng Yin*
IBM	Adge Hawes, Luis Armenta, Trevor Timpane
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Hsinho Wu, Mohammad Bapi, Michael Mirmak, Masahi Shimanouchi, Todd Bermensolo, Zao Liu, Gong Ouyang, Udy Shrivastava, Gianni Signorini, Richard Mellitz, Youqing Chen*, Jennifer Liu* Luping Liu*, Bruce Qin*, Yuyang Wang*
IO Methodology	Lance Wang*
Keysight Technologies	Radek Biernacki, Heidi Barnes, Jian Yang, Fangyi Rao, Stephen Slater, Pegah Alavi, Edwin Young
Maxim Integrated	Yan Liang, Don Greer, Thinh Nguyen, Joe Engert, Hock Seon, Ahmed Gendy
Mentor Graphics	Arpad Muranyi, Vladimir Dmitriev-Zdorov, John Angulo, Mikael Stahlberg
Micron Technology	Randy Wolff, Justin Butterfield
Signal Integrity Software	Mike LaBonte*, Walter Katz, Todd Westerhoff, Richard Allred

Synopsys	Ted Mido, Kevin Li, Massimo Prando, Xuefeng Chen* Andy Tai*, Jinghua Huang*
Teraspeed Labs	Bob Ross
Xilinx	(Raymond Anderson)
ZTE Corporation	Shunlin Zhu*, Fengling Gao*, Lili Wei*, Zhongmin Wei* Bi Yi*, Changgang Yin*, Yang Yang*, Xiaoli Yu*
Zuken	Michael Schaeder, Amir Wallrabenstein

OTHER PARTICIPANTS IN 2016

Alcatel-Lucent	Yishan Li*, Yiqing Mao*
Aurora System	Dian Yang*
BasiCAE Software Technology	Darcy Liu*
Celestica	Allen Wang*, Vincent Wen*
eASIC	David Banas
Edadoc	Deheng Chen*, Hong Zhang*
FiberHome Technologies	Yejing Jia*
Fujitsu Advanced Technologies	Shogo Fujimori
Ghent University	Paolo Manfredi
Gowin Semiconductor	Xiaozhi Lin*, Qi Zhou*
H3C	Bin Chen*, Mao Jun, Xing Hu*
Hamburg University of Technology	Jan Preibisch, David Dahl
Hanghou Hikvision Digital Technology	Wenquan Hu*
Hisilicon	Wei Zhen*,
Independent	Carl Gabrielson
Info TM Microelectronics	Aofeng Qian*
Institut Supérieur des Sciences Appliquées et de Technologie de Sousse	Wael Dghais
Inventec	Zhong Peng*
JEITA	Yosuke Kanamaru
John Baprawski, Inc.	John Baprawski
KEI Systems	Shinichi Maeda
Lattice Semiconductor	Dinh Tran, Maryam Shahbazi
Leading Edge	Pietro Vergine
Marvell	Jie Pan*, Weizhe Li*, Liang Wu*, BL Qian*, Fang Lv*
MathWorks	Mike Mulligan, Corey Mathis
Monsoon Solutions	Nathan Hirsch
Mostec	Ninghua Li*, Kaihe Zhang*
Northrup Grumman	Alex Golian
NXP	Jon Burnett
Politecnico di Torino	Claudio Siviero, Stefano Grivet-Talocia, Igor Simone Stievano
Qualcomm Technologies	Guobing Han*
Rambus	John Yan

Raytheon	Joseph Aday
SAE International	(Logen Johnson)
SAIC Motor Corp	Weng Yang*
Shanghai Zhaoxin Semiconductor	Jude Ji*
Shenzhen Zhongzeling Electronics	Nick Huang*
SILABTECH	Biman Chattopadhyary
Signal Metrics	Ron Olisar
SiGuys	Donald Telian
SMICS	Sheral Qi*
Sony Corporation	Hiroaki Ammo
Sony LSI Design	Takashi Hasegawa
SPISim	Wei-hsing Huang*
Spreadtrum Communications	Junyong Deng*, Steven Guo*, Baoping Bian* Yanbiao Chu*, Nikki Xie*, Zhi Wang*
STMicroelectronics	Fabio Brina, Olivier Bayet
Technoprobe	Alberto Berizzi, Lorenzo Bernasconi, Simona Cucchi
Teledyne LeCroy	Denny Li*, Yifeng Wu*
Université de Bretagne Occidentale	Mihai Telescu
Vendorchain	Jun Zhao*, Jing Luo*, Dong Lei*
Xpeedic Technology	Max Cang*, Mingcan Zhao*, Zhouxiang Su*, Rui Wang* Qionhui Gui*, Wenliang Dai*, Yuqing Shen* Haitao Zhang*
Zhejiang Uniview Technologies	Weiqi Chen*, Jiayun Dai*

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
November 14, 2016	Asian IBIS Summit Taipei – no teleconference	
November 18, 2016	Asian IBIS Summit Tokyo – no teleconference	
December 2, 2016	628 078 024	IBISfriday11

For teleconference dial-in information, use the password at the following website:

https://sae.webex.com/sae/j.php?MTID=m0a07ee0ddc25e28af96b4bbad3c17f4b

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The Asian IBIS Summit took place on Friday, November 11, 2016 at the Parkyard Hotel in Shanghai. About 112 people representing 34 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.ibis.org/summits/nov16a/

Gezi Zhang of Huawei welcomed the participants to the 12th annual Asian IBIS Summit (China) on behalf of Shuyao Liu of Huawei. She expressed her appreciation to the IBIS Open Forum and all the sponsors for co-organizing the event. She looked forward to working with IBIS members in China and to expanding participation in the region. She noted that Huawei hopes to resolve high speed link issues with the IBIS Open Forum, EDA vendors and IC vendors.

Mike LaBonte welcomed participants on behalf of the IBIS Open Forum and convened the meeting, noting that only technical presentations would be on the agenda, and there would be no voting.

Mike continued by thanking all the co-sponsors. The primary sponsor was Huawei Technologies, and the co-sponsors were Cadence Design Systems, IO Methodology, SPISim, Synopsys, Teledyne LeCroy, Xpeedic Technology and ZTE Corporation.

IBIS CHAIR'S REPORT

Mike LaBonte (Signal Integrity Software (SiSoft), USA)

Mike LaBonte presented updates on work in progress in the ATM, Interconnect and Quality task groups. This includes an IBIS 6.2 release, backchannel support, C_comp model enhancements, redriver flow enhancements, and an interconnect modeling BIRD. Several BIRDs have been approved for IBIS 6.2 while some are still in progress. The IBIS Open Forum has 22 members and regular teleconference and Summit meetings. The China regional forum is a new group affiliated with IBIS.

IBIS MODEL SIMULATION WITH RLC_DUT

Xuefeng Chen (Synopsys, PRC)

Xuefeng Chen presented an enhanced IBIS algorithm to support the R/L/C_dut subparameters in V-T tables. The algorithm shows a large improvement in matching IBIS to Spice transistor-level models when these subparameters are used versus traditional algorithms. The Ku and Kd results of V-T solving are sensitive to R/L/C_dut subparameters, so using these subparameters requires caution. With the new algorithm, a more complicated C_comp model could also be supported.

One attendee noted that very few IBIS models are seen that contain R/L/C_dut subparameters

and questioned the importance of the new algorithm. Xuefeng responded that the algorithm will give more accurate results if the subparameters are used.

CASE STUDY: MODELING IBIS FOR OPEN_DRAIN TRUE DIFFERENTIAL PAIR BUFFER

Lance Wang*, Yan Liang** (*IO Methodology and **Maxim Integrated, USA)

Lance Wang presented. An Open_drain differential pair presents a special case for IBIS modeling. The Open_drain model type does not use Pullup I-V data, but this data is useful for modeling this type of buffer. Using an Output or I/O model type to model this type of buffer allows inclusion of Pullup I-V data and is a better solution. Improvements to the C_comp model to capture voltage and frequency dependencies would improve the model further.

A question was asked why one should use the Output model type instead of the Open_drain type. Lance responded that there needs to be Pullup curve data in the IBIS model to capture the current due to the true differential buffer features.

DIFFERENTIAL MODELING FLOW WITH SERIES MODEL IN VERILOG-A

Wei-hsing Huang* and Sanjeev Gupta** (*SPISim, USA and **Sigintegrity Solutions, India)

Wei-hsing Huang presented. Half/true differential buffers are modeled including a series model for the effects of differential current and differential capacitance. The rigid syntax of the series model can lead to many inaccuracies. Replacing the series model with a Verilog-A model using [External Model] syntax streamlines the modeling flow, improves V-T extraction accuracies, and removes the rigid series model syntax. A modeling flow for creating the Verilog-A model was presented.

IBIS-AMI MODEL GENERATION WITH QUALITY

Skipper Liang (Cadence Design Systems, ROC)

Yitong Wen presented starting with an overview of channel simulation equations and IBIS-AMI models. IBIS-AMI model generation flow involves many steps, and validation is the key. Validation includes comparisons to Spice transistor-level model simulations. An example was shown of USB 3.0 RX and TX IBIS-AMI models in simulation including real channel characteristics.

A comment was made that IBIS-AMI model validation cannot just look at waveforms and eye openings.

SUGGESTION ON ISSUING VSR/CAUI-4 BASED IBIS-AMI MODEL

Zhengrong Xu (Huawei Technologies, PRC)

Zhengrong Xu presented. For electrical interface compliance testing of a VSR/CAUI-4 optical module, the test point is inside the CDR device after the CTLE. This test point can’t be

measured, so a standard “Reference CTLE” and “Golden PLL” model is defined. This model can be used as a software reference in an oscilloscope to post process measurement waveforms. An equivalent simulation solution is needed. Zhengrong suggested the IBIS organization issue a standard VSR/CAUI-4 compliant IBIS-AMI model including the reference CTLE and golden PLL. This may also provide a way for optical CDR vendors to do correlation between their settings and the equalization settings defined in the standard.

NECESSITY FOR INTEGRATING FEC FUNCTIONALITY FOR PAM4 IN AMI SIMULATIONS

Xiaoqing Dong* and Nick Huang** (*Huawei Technologies, **Shenzhen Zhongzeling Electronics, PRC)

Nick Huang presented. Conventional IBIS-AMI simulation does not take into account forward error correction (FEC) functionalities. Industry standards on PAM4 require FEC to achieve basic BER targets given similar channel insertion loss as NRZ systems. FEC gain can be modeled using error propagation theories. The concept was proven for feasibility of PAM4 simulation to integrate FEC functionalities through two case studies. It is recommended that IBIS-AMI consider FEC simulation functionality for PAM4.

THE IMPACT OF CHANNEL PERFORMANCE TO 56G PAM4 SYSTEMS

Changgang Yin, Shunlin Zhu (ZTE Corporation, PRC)

Changgang Yin presented. The 56G PAM4 standard is still a work in progress. IBIS-AMI modeling for PAM4 is new but works well in simulation. A detailed analysis was performed to determine the impact of channel characteristics on 56G PAM4 systems. One conclusion was that the insertion loss resonance frequency should be greater than 29 GHz and the resonance depth should be as small as possible. The impedance tolerance is recommended to be smaller than +/- 8% and impedance discontinuity points should be reduced as much as possible. Crosstalk is dominated by NEXT, so more attention should be paid to NEXT than FEXT. ICN of crosstalk must be less than 4mV and is recommended to be less than 3mV.

A question was asked if other channels were used to verify the methodology. Changgang responded that only the channel shown was used.

DISCUSSION

Lance Wang introduced the IBIS China Regional Forum and discussed its formation. The group is led by Huawei, ZTE and Celestica for now. The main purpose for this regional forum is to have an environment for Chinese engineers to be involved in IBIS developments and changes. The group plans to have its own technical teleconference and even a face-to-face conference to have discussions about recent IBIS changes, new technologies and anything that needs to feed back to the IBIS Open Forum for IBIS specification updates. Lance also introduced the freelists mailing list and WeChat group.

ACHIEVING FULL SYSTEM SIGNAL INTEGRITY FOR HIGH SPEED BACKPLANE SYSTEM

Wenliang Dai (Xpeedic Technology, PRC)

Wenliang Dai presented. The presentation included an introduction of backplane systems, challenges to backplane system simulation, components of EM simulation, an analysis workflow, and details of full backplane system SI simulation. Wenliang concluded that passive channel modeling and simulation is essential to high speed channel design. Optimal channel design requires user friendly EDA tools to do layout extraction, via optimization, trace simulation, S-parameter cascading and S-parameter exploration. Full backplane system SI simulation is achieved by sweeping all the channels with correct models.

ON-DIE DECOUPLING MODEL IMPROVEMENTS FOR IBIS POWER AWARE MODELS

Randy Wolff# and Aniello Viscardi## (Micron Technology, #USA, ##Italy)

Lance Wang presented. He noted that on-die decoupling models for power aware modeling must be added external to the IBIS model currently. To correlate an IBIS model simulation with a transistor model simulation, the decoupling model may need multiple terminals. A Spice model may include a pre-driver on a separate power supply from the driver, and coupling may exist between the pre-driver supply and the final driver supply. The pre-driver and final driver may also share a common ground. One method for creating a non-proprietary decoupling model involves creating an S-parameter model. The S-parameter model could have multiple port options and may require a node 0 reference. Lance showed results of two simulations including package models with either an ideal or non-ideal connection to the pre-driver supply of the Spice model. A 2-port decoupling model was necessary for good correlation in the case with the ideal connection to the pre-driver supply. A 3-port decoupling model was necessary for good correlation in the case with the non-ideal connection to the pre-driver supply. Lance concluded that a multi-port decoupling model is most versatile. Unused ports not connected to a package model should be connected to node 0, which is also the reference port for the S-parameter model.

IBISCHK6 V6.1.3 AND EXECUTABLE MODEL FILE CHECKING

Bob Ross (Teraspeed Labs, USA)

Mike LaBonte presented. New ibischk6 version 6.1.3 executables are available that resolve BUGs 174-180. The executable names include 32 and 64-bit operating system designations. An enhancement is executable model file checking per BUG179 for [Algorithmic Model] executable lines. Executable files are checked for the existence of required functions based on .ami file Reserved_Parameters settings.

TOUCHSTONE CONVERSION WRAPPER

Anders Ekholm (Ericsson, Sweden)

Anders Ekholm presented. The tschk2 Touchstone file parser can be used to convert Touchstone models to Touchstone 2 models using the –canonical option. Using this option strips out any comments from the original Touchstone file which may contain useful port information. Anders wrote a Perl script named TS1toTS2 that solves this issue. The script is available on the IBIS Open Forum website.

CLOSING REMARKS

Mike LaBonte surveyed participants to see their relationship to IBIS. A show of hands revealed that the group was predominantly IBIS users, followed by IC companies, with EDA vendors last. Mike also brought up the China Regional Forum, expressing a hope that this group would at some point be working on BIRDs originating in China, so that IBIS could be more responsive to their needs.

Mike thanked the co-sponsors, presenters and attendees for their participation and support. The meeting adjourned at 5:30 PM.

NEXT MEETING

The next IBIS Open Forum teleconference meeting will be held December 2, 2016. The Asian IBIS Summit in Taipei will be held November 14, 2016. The Asian IBIS Summit in Tokyo will be held November 18, 2016. No teleconferences will be available for the Summit meetings.

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NOTES

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This meeting was conducted in accordance with ANSI guidance.

All inquiries may be sent to info@ibis.org. Examples of inquiries are:

- To obtain general information about IBIS.
- To ask specific questions for individual response.
- To subscribe to the official ibis@freelists.org and/or ibis-users@freelists.org email lists (formerly ibis@eda.org and ibis-users@eda.org).
- To subscribe to one of the task group email lists: ibis-macro@freelists.org, ibis-interconn@freelists.org, or ibis-quality@freelists.org.
- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.
- To report bugs or request enhancements to the free software tools: ibischk6, tschk2, icmchk1, s2ibis, s2ibis2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.ibis.org/bugs/ibischk/
http://www.ibis.org/ bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.ibis.org/bugs/tschk/
http://www.ibis.org/bugs/tschk/bugform.txt

The BUG Report Form for icmchk resides along with reported BUGs at:

http://www.ibis.org/bugs/icmchk/
http://www.ibis.org/bugs/icmchk/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.ibis.org/bugs/s2ibis/bugs2i.txt
http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt
http://www.ibis.org/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.ibis.org/

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

http://www.ibis.org/directory.html

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SAE STANDARDS BALLOT VOTING STATUS

Organization	Interest Category	Standards Ballot Voting Status	September 23, 2016	October 14, 2016	November 4, 2016	November 11, 2016
ANSYS	User	Active	X	X	X	-
Broadcom Ltd.	Producer	Inactive	-	X	-	-
Cadence Design Systems	User	Active	X	X	X	X
Cisco Systems	User	Inactive	-	-	-	X
CST	User	Inactive	-	-	-	-
Ericsson	Producer	Inactive	-	-	-	X
GLOBALFOUNDRIES	Producer	Active	X	X	X	-
Huawei Technologies	Producer	Inactive	-	-	-	X
Infineon Technologies AG	Producer	Inactive	-	-	-	-
IBM	Producer	Active	X	X	X	-
Intel Corp.	Producer	Active	X	X	X	X
IO Methodology	User	Active	X	X	X	X
Keysight Technologies	User	Active	X	X	X	-
Maxim Integrated	Producer	Inactive	-	-	-	-
Mentor Graphics	User	Active	X	X	X	-
Micron Technology	Producer	Active	X	X	X	-
Signal Integrity Software	User	Active	X	X	X	X
Synopsys	User	Active	X	X	X	X
Teraspeed Labs	General Interest	Active	X	X	X	-
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	-	-	X
Zuken	User	Inactive	-	-	-	-

Criteria for SAE member in good standing:

- Must attend two consecutive meetings to establish voting membership
- Membership dues current
- Must not miss two consecutive meetings

Interest categories associated with SAE standards ballot voting are:

- Users - members that utilize electronic equipment to provide services to an end user.
- Producers - members that supply electronic equipment.
- General Interest - members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations and associations, and/or consumers.