IBIS Open Forum Minutes

Meeting Date: **November 16, 2015**
Meeting Location: **Tokyo, Japan**

VOTING MEMBERS AND 2015 PARTICIPANTS

Altera	[David Banas], Masashi Shimanouchi, Hsinho Wu Amanda Liao
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	Yui Shimizu*, Atsushi Tomishima*, Yasuki Torigoshi*
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Toshiba Semiconductor & Storage	Yasunobu Umemoto*
Xilinx	(Raymond Anderson)
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Zuken	Michael Schaeder, Markus Buecker, Griff Derryberry
	Ralf Bruening, Kiyohisa Hasegawa*, Yoshiaki Manage*

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	Peter Lee, Hank Lin, Vincent Lu, Bin-Chyi Tseng
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Kyocera Circuit Solutions	Kiyoiko Kaiya*
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SAIC Motor	Weng Yang
Sanei Hytechs Co.	Hiroyuki Kai*
Saxa	Takayuki Ito*
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Shanghai Lefu Educational Technology	Peter Sun, Leo Yi
Siemens AG	Boris Kogan, Michael Flint
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Simberian	Yuriy Shlepnev
SMICS	Xuejiao Qi
Socionext	Shinichiro Ikeda*, Motoaki Matsumura*, Megumi Ono* Yumiko Sugaya*, Yukiko Tanaka*, Kazuo Toda* Kohichi Yasuda*
Sohwa & Sophia Technologies	Tomoki Yamada*
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Spreadtrum Communications	Linping Chen, Yanbiao Chu, Lily Dai, Junyong Deng

	Steven Guo, Weiquan Jia, Xiaobin Lu, Mengying Ma Ye Ping, Zheng Qin, Baoqin Su, Tim Wang, Nikki Xie Honggiu Xu, Eric Zhang
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Technische Universität Hamburg-Harburg	Jan Preibisch
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Xpeedic Technology	Wenliang Dia, Qionghui Gui, Zhouxiang Su Mingcan Zhao
Zhejiang Uniview Technologies	Busen Cai, Weiqi Chen
ZI Consulting	Iliya Zamek

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
November 20, 2015	205 475 958	IBIS

For teleconference dial-in information, use the password at the following website:

https://ciscosales.webex.com/ciscosales/j.php?J=205475958

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The Asian IBIS Summit took place on Monday, November 16, 2015 at the Akihabara UDX building in Tokyo. About 106 people representing 61 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.ibis.org/summits/nov15c/

Toru Watanabe welcomed everyone to the meeting, explaining the role of the JEITA IBIS Promotion working group in facilitation the advancement of IBIS. Shogo Fujimori (Fujitsu Advanced Technologies and JEITA IBIS Promotion Working Group Chair) provided welcomed everyone and explained the meeting agenda and logistics. Mike LaBonte opened the official IBIS Summit.

Mike continued by thanking the co-sponsors: the major organizational sponsors JEITA and the IBIS Open Forum and also the co-sponsors ANSYS, Cadence Design Systems, Cybernet Systems, Keysight Technologies, Mentor Graphics Corporation, Toshiba and Zuken.

IBIS CHAIR'S REPORT

Mike LaBonte (Signal Integrity Software (SiSoft), USA)

Mike LaBonte described the activities of the IBIS Open Forum including its various specifications and formal standards, as well as the passage of IBIS 6.1. He introduced the new IBIS website and gave information on how to participate in IBIS activities. Mike said one of his goals as chair is to reduce the time that some BIRDs remain unresolved.

IBIS PROMOTION WORKING GROUP REPORT

Shogo Fujimori (Fujitsu Advanced Technologies, Japan)

Shogo Fujimori reported on the status of the JEITA IBIS Promotion Working Group, noting that a Quality Framework web page and a JEITA book are available. The group has provided useful summaries of IBIS keywords and guidelines for the use of advanced IBIS technologies. An IBIS workshop had been conducted the same day, ahead of the IBIS summit meeting.

INTRODUCING IBIS VERSION 6.1

Michael Mirmak (Intel Corporation, USA)
[Presented by Mike LaBonte (Signal Integrity Software (SiSoft), USA)]

Mike LaBonte gave a brief overview of the major changes in IBIS Version 6.1, covering both the AMI and traditional IBIS portions. For the IBIS-AMI areas, model dependencies are supported, PAM4 is included, and bi-directionality is explicitly included. For traditional IBIS, initial delays are

explicitly defined to assist with overclocking, and clarifications are made to package diagonals and package pin assignments for power delivery.

IBIS SIMULATION FOR HIGH-SPEED MEMORY INTERFACE BOARD SUGGESTIONS: HOW TO USE IBIS MODEL CORRECTLY

Masaki Kirinaka and Akiko Tsukada (Fujitsu Interconnect Technologies Limited, Japan)
[Presented by Masaki Kirinaka (Fujitsu Interconnect Technologies Limited, Japan)]

Masaki Kirinaka presented an overview of typical IBIS model quality issues that have been observed in the past and in the present. He noted that some issues are not in the models themselves but are due to user errors such as failure to observe notes provided with models, such as correct [Model Selector] settings for different cases. Other issues external to the models include lack of support in simulators for some IBIS keywords and subparameters such as C_comp_power_clamp and C_comp_ground_clamp. The importance of having two [Rising Waveform] and two [Falling Waveform] keywords was demonstrated. He concluded by showing how to incorporate socket model elements directly into an EBD model, bypassing the need for a separate connector model.

IBIS INTERCONNECT BIRD UPDATE

Walter Katz (Signal Integrity Software (SiSoft), USA)
[Presented by Mike LaBonte (Signal Integrity Software (SiSoft), USA)]

Mike LaBonte gave an overview of the new IBIS [Interconnect Model] syntax proposed to allow IBIS-ISS subcircuits to be used as both on-die and package interconnect models. Mike showed a number of examples illustrating that broadband S-parameter models in Touchstone format would be supported, as well as diverse subsets of models for on-die and package interconnect, for signal nets and for power nets. Model makers would not be constrained to produce a single model for the whole device and could directly use the various circuits they already have on hand.

BOARD DESIGN AND IBIS SIMULATION IN CONSIDERATION OF THE DELAY CONTROL

Makoto Matsumuro (IB-Electronics, Japan)

Makoto Matsumuro showed a method for calculating pin delays using existing package models and using these to de-skew bus signals by altering PCB routing. The calculations are simple for IBIS [Pin] RLC and [Define Package Model]. Delay calculations are more complicated when S-parameter package models are used. He concluded by suggesting that EDA tools implement delay extraction from S-parameter models, and alternatively recommending that these models be enhanced to contain delay data.

A PRACTICAL DOE APPLICATION IN STATISTICAL SI ANALYSIS USING IBIS & HOW CAN WE MAKE IBIS WORK BEYOND BEST CASE/WORST CASE?

Feng Shi*, Anders Ekholm**, Zilwan Mahmod** and David Zhang* (Ericsson, *China, **Sweden)
[Presented by Zilwan Mahmod (Ericsson, Sweden)]

Zilwan Mahmod gave a brief overview of design of experiments (DOE) methodology in the context of a specific example of finding acceptable network topology and other settings using very fast response surface model technology. Step by step elimination of settings that did not matter much and settings that produced unacceptable results led to eye diagrams that were reasonably open in best and worst cases. She concluded by saying that engineers should increasingly use statistical/probability methods and that IBIS should allow for parameters that are expressed with confidence interval ranges and not only as “100% confidence” values.

IBIS SIMULATION CASE STUDY: UNEXPECTED GLITCH AND USING C_FIXTURE

Lance Wang (IO Methodology, USA)

Lance Wang presented simulation results showing artifacts that were dependent on the simulation time step used. The possible causes were explored, and it was found that not using C_fixture for SPICE extraction or making certain modifications to extracted IBIS V/T curves could lessen the artifacts. Lance reported that it appears some IBIS simulators completely ignore C_fixture values in IBIS files.

IBIS-AMI: CONCERN FOR PAM4 SIMULATION

Shinichi Maeda (KEI Systems, Japan)

Shinichi Maeda showed that in addition to faster NRZ signaling, PAM4 signaling has become a viable option for achieving 56Gbps speeds. He gave an overview of PAM4 and its simulation using IBIS 6.1 IBIS-AMI models. He noted that the IBIS-AMI methodology assumes linear buffers, but if a completely ideal step is used the result may be a model with a faster edge than the actual buffer. He also suggested that with PAM4 it is important to simulate all process corners since with PAM4 it is not as clear which process corner would be worst case, as it is with NRZ. However, some IBIS-AMI models do not have slow and fast corners, making an accurate worst case determination difficult.

DDR4 SI/PI ANALYSIS USING IBIS5.0

Yumiko Sugaya (Socionext, Japan)

Yumiko Sugaya said that overclocking had been an issue using IBIS models, but EDA tools have solved the issue, making IBIS 5.0 power aware models fairly accurate and fast for DDR4 analysis with SSO. She gave a thorough overview of the overclocking issue and the use of initial delay compensation to solve the problem. Some waveform and eye diagram results with good correlation were shown. IBIS was able to simulate in 3 hours a circuit that took 9.2 days in SPICE. She suggested that IBIS should support modeling of the pre-buffer delay penalty to resolve the overclocking issue in a portable manner.

CONCLUDING ITEMS

Issues of available IBIS model quality were discussed, as well as advancements in package modeling. Mike LaBonte noted that the IBIS Open Forum provides a free Model Review Service,

encouraging IC vendors to submit models for review. Mike also encouraged participants to submit BIRDs detailing suggested IBIS improvements.

Toru Watanabe thanked the presenters and IBIS Open Forum for making the meeting a success.

Mike LaBonte thanked the co-sponsors, presenters and attendees for their participation and support. The meeting adjourned at 5:30 PM.

NEXT MEETING

The next IBIS Open Forum teleconference meeting will be held November 20, 2015. The following IBIS Open Forum teleconference meeting will be held December 18, 2015.

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NOTES

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This meeting was conducted in accordance with ANSI guidance.

All inquiries may be sent to ibis-info@freelists.org. Examples of inquiries are:

- To obtain general information about IBIS.
- To ask specific questions for individual response.
- To subscribe to the official ibis@freelists.org and/or ibis-users@freelists.org email lists (formerly ibis@eda.org and ibis-users@eda.org).
- To subscribe to one of the task group email lists: ibis-macro@freelists.org, ibis-interconn@freelists.org, or ibis-quality@freelists.org.
- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.
- To report bugs or request enhancements to the free software tools: ibischk6, tschk2, icmchk1, s2ibis, s2ibis2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.ibis.org/bugs/ibischk/
http://www.ibis.org/ bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.ibis.org/bugs/tschk/
http://www.ibis.org/bugs/tschk/bugform.txt

The BUG Report Form for icmchk resides along with reported BUGs at:

http://www.ibis.org/bugs/icmchk/
http://www.ibis.org/bugs/icmchk/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.ibis.org/bugs/s2ibis/bugs2i.txt
http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt

http://www.ibis.org/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.ibis.org/

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

http://www.ibis.org/directory.html

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IBIS – SAE STANDARDS BALLOT VOTING STATUS

Organization	Interest Category	Standards Ballot Voting Status	October 28, 2015	November 9, 2015	November 13, 2015	November 16, 2015
Altera	Producer	Inactive	X	X	-	-
ANSYS	User	Inactive	-	-	-	X
Applied Simulation Technology	User	Inactive	-	-	-	-
Avago Technologies	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Active	-	X	X	X
Cisco Systems	User	Inactive	-	X	-	-
CST	User	Inactive	-	-	-	-
Ericsson	Producer	Active	-	X	X	X
Huawei Technologies	Producer	Inactive	-	X	-	-
IBM	Producer	Inactive	X	-	-	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Inactive	X	-	X	-
IO Methodology	User	Active	-	X	X	X
Keysight Technologies	User	Active	X	X	X	X
Maxim Integrated Products	Producer	Inactive	-	-	-	-
Mentor Graphics	User	Inactive	X	-	-	X
Micron Technology	Producer	Inactive	-	-	-	X
Signal Integrity Software	User	Active	X	X	X	X
Synopsys	User	Inactive	X	X	-	-
Teraspeed Labs	General Interest	Inactive	X	-	-	-
Toshiba	Producer	Inactive	-	-	-	X
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	X	-	-
Zuken	User	Inactive	-	-	-	X

I/O Buffer Information Specification Committee (IBIS)

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH SAE BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
- PRODUCERS - MEMBERS THAT SUPPLY ELECTRONIC EQUIPMENT.
- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.