

IBIS Open Forum Minutes

Meeting Date: May 13, 2015 Meeting Location: SPI-E IBIS Summit, Berlin, Germany

VOTING MEMBERS AND 2015 PARTICIPANTS

Altera ANSYS Applied Simulation Technology Avago Technologies Cadence Design Systems Cisco Systems Ericsson Huawei Technologies IBM Infineon Technologies AG Intel Corporation

IO Methodology Keysight Technologies

Maxim Integrated Products Mentor Graphics Micron Technology Qualcomm Signal Integrity Software

Synopsys

Teraspeed Labs Toshiba Xilinx ZTE Corporation Zuken

[David Banas], Masashi Shimanouchi, Hsinho Wu (Steve Pytel), Curtis Clark Fred Balistreri, Norio Matsui Minh Quach, Leif Zweidinger Brad Brim, Joshua Luo, Ken Willis, Joy Li, Ambrish Varma David Siadat, Rockwell Hsu, Bidyut Sen Anders Ekholm* Xiaoging Dong Adge Hawes, Luis Armenta **Christian Sporrer*** Michael Mirmak, Todd Bermensolo, Nhan Phan Gianni Signorini* Lance Wang Radek Biernacki, Pegah Alavi, Colin Warwick Jian Yang, Nicholas Tzou, Heidi Barnes, Dave Larson **Kyla Thomas** Mahbubul Bari, Don Greer, Joe Engert Arpad Muranyi, Ed Bartlett, Vladimir Dmitriev-Zdorov Randy Wolff* Senthil Nagarathinam, Kevin Roselle Mike LaBonte, Walter Katz, Todd Westerhoff Mike Steinberger Ted Mido, Rita Horner, William Lau, Scott Wedge Michael Zieglmeier, Joerg Schweden* Bob Ross, Tom Dagostino (Yasumasa Kondo) (Raymond Anderson) (Min Huang), Tao Guo Michael Schaeder*, Markus Buecker, Griff Derryberry **Ralf Bruening***

OTHER PARTICIPANTS IN 2015

Bayside Design Continental Automotive

CST Freescale Galbi Research Elliot Nahas Felix Goelden, Markus Bebendorf, Sebastian Groener* Stefanie Schatt* Stefan Paret*, Matthias Troescher* Jon Burnett Dave Galbi

| Tim Wang Lee |
|------------------------------|
| Wael Dghais* |
| Shinichi Maeda |
| Xu Jiang |
| Pietro Vergine* |
| Stefano Grivet-Talocia* |
| Joseph Aday |
| Chris Denham |
| Boris Kogan*, Michael Flint* |
| Yuriy Shlepnev |
| Jan Preibisch* |
| Siris Tsang |
| Iliya Zamek |
| |

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

| Date | Meeting Number | Meeting Password |
|--------------|----------------|------------------|
| May 22, 2015 | 205 475 958 | IBIS |

For teleconference dial-in information, use the password at the following website:

https://ciscosales.webex.com/ciscosales/j.php?J=205475958

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The IBIS Open Forum Summit was held in Berlin, Germany at the Seminaris CampusHotel Berlin following the 2015 SPI conference. About 17 people representing 13 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda.org/ibis/summits/may15/

Randy Wolff welcomed all the participants and thanked the sponsors ANSYS, CST, Mentor Graphics, Synopsys and Zuken. He asked all the participants to introduce themselves. There were a wide variety of people from many countries and organizations including academia and industry.

PHYSICS AND MODELING OF VIAS IN PRINTED CIRCUIT BOARDS

Jan Preibisch and Christian Schuster, Technische Universitat Hamburg-Harburg, Germany

Jan Preibisch presented. Vias cause signal integrity problems such as attenuation, reflections, dispersion, interference and crosstalk. PI problems caused by vias include voltage drop, switching noise and crosstalk. EMC problems include near field coupling and radiated emissions. Currents on the via structure include signal current, conduction return current and displacement return current. Ground vias have a significant effect on the signal via. Adding two vias makes the situation better. Increasing more ground vias shields the signal via better and better.

Jan presented a model for vias. A physics based model includes coupling from the via to the planes and a complex impedance between the parallel plates. Three methods for determining the parallel plate impedance are the cavity resonator method, radial waveguide method and the contour integral method. CIM is a two dimensional method of moments solution that works with arbitrary boundaries and also models the via itself. Including striplines in the model involves modeling the parallel plate impedance as well as the stripline mode. Complete models for one cavity can be combined to model the full PCB. The models compared very well to full-wave 3D simulator models. The via model can be created in a few seconds of computer time versus 3-4 hours with the 3D EM solver.

Limitations exist such as coupling from one via to another directly when they are very close. The technique models via pitches down to 20 mils currently.

Anders Ekholm asked if Jan had looked at differential vias. Jan replied that yes, he modeled those as well. Anders asked if 3D effects of the trace coming into the via are modeled. Jan responded that most effects are taken care of by mode conversion. Traces on the top layer are not modeled as well. Christian Sporrer asked if this technique was only for modeling of a PCB or if it can be used for via optimization. Jan noted that it is fast to create the models, but the models are not implemented in an optimizer currently.

CHAIR'S STATUS REPORT

Michael Mirmak, Intel Corporation, USA

Randy Wolff presented. He began by describing IBIS' parent organization change from

TechAmerica to SAE Industry Technical Consortia. He noted that IBIS 6.1 is in editorial review now, with many changes related to AMI. The Interconnect task group is also close to completing a BIRD to improve package and on-die interconnect modeling capabilities. The following version of IBIS will include this BIRD as well as backchannel equalization support, redriver AMI flow clarifications and PAM-4 signaling support.

Randy discussed proposals to establish a 1-year IBIS release schedule and use a new numbering scheme. These changes could affect parser development and membership dues.

IBIS MODEL FORMULATION AND EXTRACTION FOR SPI EVALUATION

Wael Dghais, Kevin F.G. Pinto and Jonathan Rodriguez, Universidade de Aveiro, Instituto de Telecomunicações, Portugal

Wael Dghais presented work done to improve the underlying equations used to simulate IBIS models used for both signal and power integrity. He proposed that linear interpolation of the non-linear [ISSO PU] and [ISSO PD] data was accurate enough and could improve simulator convergence and speed. Randy Wolff commented that this seemed reasonable given the limited practical change in gate voltage seen in real device operation.

Wael then showed details of modeling the [Composite Current] data in IBIS. He proposed the need for modeling a buffer's ground current as well as the power supply current already modeled by [Composite Current] data. The resulting model compared very well to the transistor-level model. Wael also noted that model for his paper assumes different VDD rails for the pre-driver and the driver.

Randy Wolff asked what changes in IBIS are needed. Wael commented that he'd like to see [Composite Current] extended to include ground current. Manfred Maurer asked what measurement point is shown in correlations. Wael responded that it is the output of the first driver only in the three driver SSO simulation. Randy commented that when the pre-driver shares the power supply with the driver, then the pre-driver timing is also affected by power supply changes. He is interested in trying to model this effect. Anders Ekholm commented that this might be difficult, because pre-driver timing is not modelled in IBIS algorithms currently.

AD HOC DISCUSSION

Stefano Grivet-Talocia led an ad-hoc discussion on improving interaction between the SPI workshop and the IBIS Summit meeting.

Michael Schaeder commented that SPI is organized without considering the IBIS Summit. He would like to have the IBIS Summit on the agenda from the beginning. Stefano noted that IBIS is a side event that is not part of the conference. There will be concerns from IEEE about putting IBIS in the program. Since Stefano will have control over the SPI website, it will be ok to have IBIS on the website.

Stefano commented that there is a shared objective of more participation in both SPI and IBIS meetings. Randy Wolff commented that conferences like DesignCon attract people to both DesignCon and IBIS by offering presentations on practical applications and problem solving.

Stefano commented that an IEEE conference expects to have papers on new topics and research.

Matthias Troescher commented that for Europe, there is a need to attract automotive industry participants. Like Randy mentioned, there are many users of IBIS models that want to see content on practical usage of models.

Randy proposed more discussion by email to look for ways to encourage participation in both meetings.

[DEFINE PACKAGE MODEL] PROPOSED EXTENSION

Randy Wolff*, Radek Biernacki** and Bob Ross***, *Micron Technology, **Keysight Technology and ***Teraspeed Labs, USA

Randy Wolff presented. He described how it is common in package modeling to reduce the number of power and ground terminals by merging multiple pins connected to the same plane or fill structure into a single terminal. When using this data in an IBIS RLC matrix format, [Pin Mapping] data will not be consistent with the [Pin Numbers] list under [Define Package Model], as power and ground pins may be missing. BIRD176 was written to explain this situation and propose default methods for EDA software to handle the missing pins. Pins without model data due to merging are connected with implicit shorts. A new keyword [Merged Pins] is also introduced to explicitly define merged pin groups.

Randy showed an example of [Merged Pins] syntax, then described several situations to explain the hierarchy of [Define Package Model], [Pin] RLC and [Package] RLC data. The cases described showed legal and illegal cases for use of [Pin Numbers], [Pin Mapping], and [Merged Pins] data. Randy encouraged people to read the BIRD and provide comments before the upcoming vote.

INTERCONNECT TASK GROUP UPDATE – PACKAGE MODELING

Randy Wolff, Micron Technology, USA

Randy Wolff presented an overview of recent work done by the Interconnect task group for advancing package and on-die interconnect modeling in IBIS. He described how a new BIRD in development adds support for using IBIS-ISS and Touchstone data to describe on-die and package interconnect models. Christian Sporrer asked if the BIRD improved stacked-die package modeling. Randy commented that an update to EBD will address stacked-die modeling.

Randy noted that new and legacy package models will be able to co-exist in IBIS, but this assumes the models are uncoupled with no interactions. Pre- and post-layout package models will be supported. Randy showed some examples of the proposed syntax and described in detail the Terminal subparameter. He also described new keywords that replace [Pin Mapping] with modified functionality. Corners for interconnect modeling do not easily fit the IBIS definitions for typ, min and max. Corner cases will be handled in the BIRD through selection from multiple interconnect models.

The Interconnect task group will be working on the Electrical Module Description proposal, Touchstone specification updates, and expansions of parameters to support statistical Design of Experiment simulations in the future. Randy encouraged more participation from European members in the Interconnect task group.

SSO EXPERIENCE WITH IBIS

Manfred Maurer, IT-Beratung-Maurer, Germany

Manfred Maurer began by describing simultaneous switching outputs (SSO). He showed an SSO simulation setup including one transistor level model with current multipliers for 'm' buffers switching in parallel and one model held in a quiet state. SSO is not an issue for serial signaling using differential buffers. He showed results of simulating various loads as well as when sweeping package inductance values. When simulating an IBIS model without power-aware keyword tables, the results vary greatly from the Spice syntax. Manfred noted that IBIS models with power aware keyword data are very rare.

Pietro Vergine commented that there is not enough support for IBIS models with power-aware information. Randy Wolff added that he has been able to obtain these models from vendors, but he had to provide assistance to some vendors to ensure they were generating quality models.

TIME RESPONSE UTILITY

Bob Ross, Teraspeed Labs, USA

Anders Ekholm presented. He showed a spreadsheet utility created by Bob Ross that provides a fast way of seeing the time representation of a Laplace transform. The presentation detailed several examples of Laplace transform coefficients entered into the spreadsheet and converted to time-domain waveforms. The spreadsheet utility is available for download from the IBIS website.

Manfred Maurer asked Anders to describe a useful situation for the utility. Anders noted that in IBIS-AMI, the channel is described in Touchstone format. You can take the Laplace transform of your channel to see what the step response will look like, for instance to show if you have ringing problems.

CLOSING REMARKS

Randy Wolff closed the meeting by thanking the co-sponsors and the presenters. He also thanked all the attendees for making the meeting a success. The meeting concluded at approximately 5:30 PM.

NEXT MEETING

The next IBIS Open Forum teleconference meeting will be held May 22, 2015. The following IBIS Open Forum teleconference meeting will be held June 12, 2015.

NOTES

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This meeting was conducted in accordance with ANSI guidance.

The following e-mail addresses are used:

ibis-request@eda.org

To join, change, or drop from either or both: IBIS Open Forum Reflector (<u>ibis@eda.org</u>) IBIS Users' Group Reflector (<u>ibis-users@eda.org</u>) State your request.

ibis-info@eda.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the IBIS Open Forum as a full Member.

ibis@freelists.org (changed from ibis@eda.org, which has been deactivated)

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@freelists.org (changed from ibis-users@eda.org, which has been deactivated)

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/ http://www.eda.org/ibis/bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/ http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/ http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available

on the IBIS Home page:

http://www.eda.org/ibis

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

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IBIS – SAE STANDARDS BALLOT VOTING STATUS

| | | Standards | | | | |
|-------------------------------|----------------------|------------------|-------------------|-------------------|----------------|-----------------|
| Organization | Interest Category | Voting Status | March 20, 2015 | April 10, 2015 | May 1, 2015 | May 13, 2015 |
| Altera | Producer | Active | Х | Х | Х | - |
| ANSYS | User | Active | Х | Х | Х | - |
| Applied Simulation Technology | User | Inactive | - | - | - | - |
| Avago Technologies | Producer | Inactive | - | - | - | - |
| Cadence Design Systems | User | Active | Х | - | Х | - |
| Cisco Systems | User | Inactive | - | - | - | - |
| Ericsson | Producer | Inactive | - | - | - | Х |
| Huawei Technologies | Producer | Inactive | - | - | - | - |
| IBM | Producer | Active | - | Х | Х | - |
| Infineon Technologies AG | Producer | Inactive | - | - | - | Х |
| Intel Corp. | Producer | Active | Х | Х | Х | Х |
| IO Methodology | User | Active | Х | Х | Х | - |
| Keysight Technologies | User | Active | Х | Х | Х | - |
| Maxim Integrated Products | Producer | Active | Х | - | Х | - |
| Mentor Graphics | User | Active | Х | Х | Х | - |
| Micron Technology | Producer | Active | - | Х | - | Х |
| Qualcomm | Producer | Inactive | - | - | - | - |
| Signal Integrity Software | User | Active | Х | Х | Х | - |
| Synopsys | User | Active | Х | Х | - | Х |
| Teraspeed Labs | General Interest | Active | Х | Х | Х | - |
| Toshiba | Producer | Inactive | - | - | - | - |
| Xilinx | Producer | Inactive | - | - | - | - |
| ZTE | User | Inactive | - | - | Х | - |
| Zuken | User | Inactive | - | - | - | Х |

I/O Buffer Information Specification Committee (IBIS)

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH SAE BALLOT VOTING ARE:

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- PRODUCERS MEMBERS THAT SUPPLY ELECTRONIC EQUIPMENT.
- GENERAL INTEREST MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.