IBIS Open Forum Minutes

Meeting Date: **January 30, 2015**
Meeting Location: **DesignCon IBIS Summit, Santa Clara, CA, USA**

VOTING MEMBERS AND 2015 PARTICIPANTS

Altera	David Banas*
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Applied Simulation Technology	Fred Balistreri*, Norio Matsui*
Cadence Design Systems	Brad Brim*, Joshua Luo*, Ken Willis*, Joy Li*
Ericsson	Anders Ekholm*
Huawei Technologies	Xiaoqing Dong*
IBM	Adge Hawes*, Luis Armenta*
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Michael Mirmak*, Todd Bermensolo*, Nhan Phan*
IO Methodology	Lance Wang*
Keysight Technologies	Radek Biernacki*, Pegah Alavi*, Colin Warwick*
	Jian Yang*, Nicholas Tzou*, Heidi Barnes*, Dave Larson*
	Kyla Thomas*
Maxim Integrated Products	Mahbubul Bari*, Don Greer*, Joe Engert*
Mentor Graphics	Arpad Muranyi, Ed Bartlett*, Vladimir Dmitriev-Zdorov*
Micron Technology	Randy Wolff*
Qualcomm	Senthil Nagarathinam, Kevin Roselle*
Signal Integrity Software	Mike LaBonte*, Walter Katz*, Todd Westerhoff*
	Mike Steinberger*
Synopsys	Ted Mido*, Rita Horner*, William Lau*, Scott Wedge*
	Michael Zieglmeier*
Teraspeed Labs	Bob Ross*, Tom Dagostino*
Toshiba	(Yasumasa Kondo)
Xilinx	(Raymond Anderson)
ZTE Corporation	(Min Huang)
Zuken	Michael Schaeder*, Markus Buecker*, Griff Derryberry*

OTHER PARTICIPANTS IN 2015

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Bayside Design	Elliot Nahas*
Cisco	David Siadat*, Rockwell Hsu*, Bidyut Sen*
Continental Automotive	Felix Goelden*, Markus Bebendorf*
CST	Stefan Paret*
Freescale	Jon Burnett*
Galbi Research	Dave Galbi*
Independent	Tim Wang Lee*
KEI Systems	Shinichi Maeda*
Lattice Semiconductor	Xu Jiang*

Raytheon	Joseph Aday*
SAE International	Chris Denham*
Simberian	Yuriy Shlepnev*
Vitesse	Siris Tsang*
ZI Consulting	Iliya Zamek*

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
February 6, 2015	205 475 958	IBIS

For teleconference dial-in information, use the password at the following website:

https://ciscosales.webex.com/ciscosales/j.php?J=205475958

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The IBIS Open Forum Summit was held in Santa Clara, California at the Santa Clara Convention Center during the 2015 DesignCon conference. About 63 people representing 32 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda.org/ibis/summits/jan15/

Michael Mirmak welcomed everyone to the Summit, opening the meeting at 8:30 a.m. He thanked the sponsors including Keysight Technologies for providing the food as well as

DesignCon (UBM). Michael asked all the participants to introduce themselves. There was a large cross section of model users and developers.

CHAIR'S STATUS REPORT
Michael Mirmak, Intel

Michael Mirmak began by giving an overview of IBIS version lifetimes, noting that we are working towards a one year release schedule for new IBIS versions. 11 BIRDs are open currently, mostly on packages and related areas. The chief objectives for IBIS activities are to finalize a new, comprehensive interconnect solution and to finalize backchannel treatment. The IBIS charter is also outdated, last updated in 1999. A new Policies and Procedures document is needed, and one has been drafted by the board. It can be viewed at:

http://www.eda.org/ibis/docs/policies

Comments on the document are encouraged. Major changes include updated elections procedures, quorum definitions, the addition of a Treasurer position, and clarifications of membership rules and dues. The document will be reviewed at the next two IBIS Open Forum teleconferences, followed by a vote. Emailed votes will be accepted.

Bob Ross noted that some open BIRDs are ones that are intended to be replaced by BIRDs in progress, so that inflates the number of BIRDs that are actually intended for the next specification release.

SAE INDUSTRIES TECHNOLOGY CONSORTIA: A BRIEFING
Chris Denham, SAE International

Chris Denham began by noting that the home for IBIS within the SAE organization will be SAE ITC (Industries Technology Consortia). ITC leverages the assets of the SAE Enterprise. IBIS is one of four programs within ITC.

Michael Mirmak asked how international standardization is different from past organizations such as GEIA. Chris commented that SAE does have a link to ANSI, but SAE is an international organization, so standardizing in SAE automatically provides international recognition.

SINK OR SWIM AT 28GBPS: HOW TO VALIDATE INTERCONNECT ANALYSIS SOFTWARE FOR 28GBPS DATA LINKS
Yuriy Shlepnev, Simberian

Yuriy Shlepnev began by noting that he sees IBIS-AMI models for 28Gbps systems, but before using those models it is important to validate the system models first. The design of PCB and packaging interconnects for data links running at bitrates of 28-32 Gbps and beyond is a challenging problem. Analysis can correlate with measurements if models are validated with measurements. Yuriy highlighted an analysis to measurement correlation procedure. A test board was used for gathering measurement data. Validation of the S-parameter quality is the first step. Step two involves understanding the actual as-built board geometries.   The third step is to create material models with Generalized Modal S-parameters. The fourth step is to simulate all the structure models and compare with measurement data. Yuriy showed good

correlation for several structures on the test board. He pointed out that backdrilling for strip line vias was a source of mismatch due to inconsistency with the depth of the back drill. He concluded that a process such as the one presented should be standardized.

Michael Steinberger commented that a test board might be good for validating certain aspects of a model but not all. Some geometries aren't covered. Yuriy agreed, commenting that he sees companies developing their own test boards, but none are available publicly. Michael asked how we could come to agreement on a standardized test board. Yuriy commented that you could start with one board just for transmission lines. Then a board dedicated to vias is the next most important thing to validate. Walter Katz commented that IBIS contains data to describe a model, a standardized data format. We have stayed away from defining exact quality of the data. He asked what IBIS could do for standardizing the interconnect model quality. Yuriy commented that standardizing structures that could be built on test boards could be a start. Michael suggested that we'd need to involve system designers to make sure the board contains structures that are used in practice. Yuriy noted that many test boards are out there, and those efforts could be combined.

Mahbubul Bari asked about the TDR measurements with 20ps rise time. Yuriy responded that the TDR measurements were created from S-parameter data, so the 20ps rise time related to the bandwidth of the original measurement.

IBIS-ATM TASK GROUP REPORT
Arpad Muranyi, Mentor Graphics

Michael Mirmak presented. Michael began by noting that no new capabilities from new BIRDs are in the IBIS specification since the last DesignCon. Several BIRDs have been approved since the IBIS 6.0 release. Michael noted that discussions on package and on-die interconnect modeling proposals have moved to the Interconnect task group. Two AMI-related BIRDs need to be considered. A new proposal is being discussed on backchannel communication that may supersede BIRDs 128 and 147. New discussion has started on C_comp model improvements.

IBIS QUALITY TASK GROUP REPORT
Mike LaBonte*, Bob Ross**, SiSoft*, Teraspeed Labs**

Mike LaBonte began by describing what the Quality task group does. The task group created an IBIS quality scoring system. Ongoing work is to address IBISCHK issues. Bob Ross leads most IBISCHK activities. An IBISCHK6 user guide has been in development for the last year. The document helps explain the 1,258 unique messages in IBISCHK. Help is needed on the user guide, and other topics could be discussed if more people join the group.

Michael Mirmak asked if the group discusses AMI model quality. Mike noted that the IBIS checking service has been extended to reviewing AMI models. A question was asked about updating the IBIS Quality Checklist. Mike noted that a QUAIL could be submitted to add items to the checklist.

A question was asked if there was a way to check the K-T curves created within EDA software. Mike noted that this data is not exposed to the user. Michael Mirmak commented that there are published equations about generating this data. Arpad Muranyi has also published how to

generate this data in a circuit simulator. David Banas asked if anyone was using the public Python code for AMI model debug and development. He will send a link to the code to the IBIS reflector.

IBIS INTERCONNECT BIRD
Walter Katz, SiSoft

Walter Katz began by saying that there has been a large effort to allow the use of IBIS-ISS circuits in IBIS for package and on-die interconnect modeling. The Interconnect task group's major contributors include EDA vendors, IC vendors and model providers. Model types supported include IBIS-ISS and Touchstone directly. Terminals are brought out for pins, pads, buffer signals and buffer supplies. There will be a 1:1 correspondence between signal pins and signal pads. Package models and on-die interconnect models can be combined or separate. Updating EBD with similar capabilities is planned for future work. Walter noted that there was much discussion on the use of ideal ground (node 0) in interconnect models. It will be allowed but is discouraged. There will be language supporting pre-layout and post-layout type models, allowing a terminal to connect to a pin name or a model name. Corner definitions for interconnect models are not well defined and need to be resolved. Other open issues include resolving the connection of the external reference node in [External Model]s, reconciling [External Circuit] with new interconnect models and reconciling use of the global ground reference. The goal is to complete the new BIRD for submittal to the Open Forum by mid Q2 2015. Follow on work will update EBD.

Lance Wang asked if IBISCHK will check for errors in the new syntax. Walter commented that it will, but is not defined fully yet. There will even be a way to terminate unused terminals of subcircuits.

Michael Mirmak asked if Walter saw a way for an AMI model to make use of the on-die interconnect model. Walter noted that there is an assumed high impedance connection between the AMI model and the analog buffer signal node in the IBIS model. He thought that since the AMI model only looks at the differential voltage between the positive and negative signal terminals of two models, it doesn't care about the voltage noise on power and ground terminals of the buffers. He also commented that using a GetWave flow, one could do a power aware simulation to generate a waveform at the die node that includes power effects and process that waveform with the RX AMI model. Walter did not think anything further should be standardized, since it should be up to the EDA software to determine how to use the data in the AMI flow. In response to discussion on where the waveform is at for the AMI flow, Michael responded that it is at the buffer, but this proposal adds an explicit die pad that can be a separate terminal from a buffer terminal. Walter noted that the addition of a C_comp model could actually complicate AMI by adding another node.

Mike LaBonte asked if [Pin Mapping] was used with the new proposal. Walter commented that we'd like to refer to pins with low impedance connections by their signal name, but this isn't well defined in Pin Mapping. A new keyword is being used to clarify this.

CORNER CONSIDERATIONS
Bob Ross, Teraspeed Labs

Bob Ross began by noting that the presentation was previously given at the Asian IBIS Summits last November. Corners come in many flavors and uses in IBIS. [Model] corners typically describe PVT conditions. [External Model]s align with [Model]s. [External Circuit]s could be a buffer or an interconnect model, so corners mean different things depending on the application. Package model corners could have many definitions. For IBIS-AMI corners, slow and fast entries are not clear as to their meaning. The user or EDA tool makes the corner selection. Bob detailed how the term "parameter" has many meanings in IBIS too. Bob showed an example of passing parameters into an AMI file. Since it is not clear in all cases, parameters could be assigned directly within subcircuits, or parameter names could be made more descriptive. Bob noted that the interconnect modeling proposal currently defines a "Param" that could pass in many uncorrelated parameters into a subcircuit. However, the task group is considering removing parameter passing and using interconnect model selectors instead.

Bob showed an example of how the use of L and C values for a package corresponding to desired Zo and Td values could end up with different, undesired Zo and Td corners. Bob recommended minimizing the use of parameter passing with corners because of different possible interpretations.

Walter Katz commented that for IBIS-AMI, the use of Corner was meant to relate to the process corner as in traditional IBIS. Min was meant to correlate to slow/weak and max to fast/strong. Usage of List, Range, etc. for parameters were not meant to correlate to anything in legacy IBIS. Michael Mirmak asked if we might need dependency tables or fixed limits put into the models for interconnect to ensure parameters didn't go outside acceptable ranges. Bob commented this could solve the problem in a complicated way.

IMPROVED C_COMP MODEL CASE STUDY
Randy Wolff, Micron Technology

Randy Wolff began by noting he would talk about improvements to C_comp models, showing a lossy C_comp model created from measurements and a test case demonstrating the difference between using the legacy C_comp model and using an improved lossy C_comp model. He stated that a proposal is under development to allow IBIS-ISS subcircuits to replace the legacy C_comp model.

Measurements using a VNA to capture S11 data were taken on several 8Gb DDR4 SDRAM devices. Due to JEDEC requirements, three flavors of packages were available for measurement. The first package included no die and allowed direct measurement of the package capacitance. The second package included a shorted metal die that allowed direct measurement of package inductance. The third package included a live die that allowed measurement including the die capacitance. Randy modeled several address signal inputs and showed the process for determining the ESR value of the die capacitance.

Randy used the lossy RC model of the die to compare in simulation to the original C-only C_comp model. He simulated a DDR4 LRDIMM post-register address net with DDP devices and 40 loads in total. The simulation showed an improved DC voltage margin using the lossy C_comp model. He concluded that improving the C_comp model is needed for improving the accuracy and usefulness of IBIS models.

A question was asked about how measurements were done with an active die. Randy clarified that the die was powered through a test board and the VNA probe was also biased. Bob Ross asked about the C_comp model, and Randy clarified that it is a capacitor with an ESR, so there is no series resistance.

Walter noted that there was a lot of "noise" in the measurements and some mismatch between simulation and measurement. Which is correct? Randy commented that the simulations aren't an exact match to the measurements, but they match well in the frequencies of interest up to about 3 GHz. He did not spend the time to make a more complicated model that might match to higher frequencies. Bob noted that one of the measurement lines appears to go above 0. Randy commented that this is just an artifact of the plotting software.

A question was asked about if the lossy C_comp model works in our favor. Randy commented that the lossy C_comp model provides low pass filtering that is improving the simulation results. This might not always be a good thing, but it is at least showing the correct behavior.

A question was asked about whether the C_comp model needed to be more complex. Randy commented that for the address inputs, the simple RC model looks to be good enough. A more complex model might be needed for power, but that would be better as an interconnect model. He deliberately looked at only inputs, as modeling outputs could be more complex. The RC model captured frequency dependence. Michael Mirmak commented that there can be voltage and state dependence on an output buffer's C_comp model too. Randy added that a different C_comp model might be desired for input and output states of an I/O. Michael asked if a terminator model could be used for the address input signal that Randy modeled. Randy responded that a terminator model would not be used properly in a simulator, since it would not be recognized as an input buffer.

GENERAL K-TABLE EXTRACTION PROPOSAL USING SPICE
Bob Ross, Teraspeed Labs

Bob Ross noted the need for a more detailed, generalized C_comp model. C_comp can vary with voltage, temperature, input versus output mode of the buffer, frequency, state dependence, etc. Bob described how V-T and I-T waveforms can be generated that remove the effect of C_comp from the V-T waveforms given in the IBIS model. He also showed how K tables can be generated that are used in this process. He applied this process to the case of using a C_comp subcircuit, showing how to generate the K tables needed for simulation of the IBIS buffer. He commented that he has simulated and successfully compensated for a C_comp subcircuit that included a parallel C and RC. EDA tools will need to add de-embedding of the general C_comp model subcircuit for V-T data given at the A_signal node. Also, any series resistance must be de-embedded from the I-V tables.

Mike LaBonte asked how Bob determined the correct value to use in the feedback element. Bob responded that the value did not work for all cases and might need to be decreased, potentially due to some time step issues. Radek Biernacki commented that it is currently up to the EDA tool to calculate the K tables, but questioned if it should be up to the model maker to include a K-T table that replaces the V-T table in the model. Walter Katz commented that IBIS was originally a measurement based modeling approach, so C_comp de-embedding was

needed from the beginning. Walter commented that K-T tables could be generated by model makers, but a tool would need to be put in the public domain to do it.

IBIS-AMI AND CO-OPTIMIZATION
Todd Westerhoff, Walter Katz and Mike LaBonte, SiSoft

Todd Westerhoff began by saying that the purpose of his presentation was to make sure the backchannel modeling problem was defined and the user needs (solutions) were defined before any details were talked about. He observed that optimizing TX/RX settings together provides more margin than optimizing settings individually. Three user scenarios are hardware backchannel emulation, model-based co-optimization and simulator-based co-optimization. Scenario one must emulate exactly how hardware actually works, and there are many requirements. Scenario two allows co-optimization when the actual hardware might not allow it. Scenario three allows optimization using legacy IBIS models. In scenarios one and two, the TX exploration algorithm exists in the RX model, and the TX "configurator" exists in the TX code. The EDA software only needs to allow the two models to talk to each other. Scenario three involves stepping in for the TX, RX or both models when they don't include the support for co-optimization. Todd asked for feedback about which scenarios need to be supported.

Adge Hawes asked how many systems use an open backchannel protocol. Todd responded that PCI Gen. 3 and others are common protocols that have defined communication methods. Others are considered private. Anders Ekholm asked if the goal was to support both statistical and time domain flows. Todd responded yes.

BACKCHANNEL REVISITED
Ken Willis and Ambrish Varma, Cadence

Ken Willis began by noting that he originally developed a proprietary solution to do backchannel optimization and decided to bring that solution to IBIS for standardization. Being in the IP space requires delivering lots of models, and the backchannel capability is a must-have. He noted that IBIS is a device modeling specification, and it should not become an EDA tool specification. Ken noted that scenario one and two described in Todd Westerhoff's presentation are currently covered in BIRD147. This BIRD defined a file (BCI) detailing what parameters could be passed between the RX and the TX. He felt that developing BCI files for standard protocols would be a good service for the industry and would get posted on the IBIS website. BCI files could also be developed for private protocols. Ken did not agree with support of scenario three, saying he thought it was a tool-specific capability that requires some new model development for legacy TX models. Ken concluded that he'd like to see BIRD147 completed quickly to get support for scenarios one and two in the specification quickly.

OPEN DISCUSSION
Todd Westerhoff commented that TX models could be abstracted because most follow similar modeling methods. He thought that scenario three was needed based on comments from users. Michael Steinberger commented that it looked like a BCI file would be one implementation of a TX "configurator". He was wondering what would prevent someone from creating a BCI file for their own TX. Walter summarized that he thought a BIRD could be written

to support all three scenarios that would not lock all vendors into using the flow defined by BIRD147 for scenarios one and two and a different flow later on to support scenario three. Walter commented that a metafile could be created that maps coefficients to standard information such as tap settings. This would allow legacy models with a metadata file to be used in co-optimization.

CONCLUDING ITEMS

Michael Mirmak thanked the sponsors Keysight Technologies and UBM, the presenters, organizers and attendees.

The meeting concluded at approximately 5:00 PM.

NEXT MEETING

The next IBIS Open Forum teleconference meeting will be held February 6, 2015. The following IBIS Open Forum teleconference meeting will be held February 27, 2015.

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NOTES

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This meeting was conducted in accordance with ANSI guidance.

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     subscribe ibis <your e-mail address>

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ibis-info@eda.org
     To obtain general information about IBIS, to ask specific questions for individual
     response, and to inquire about joining the IBIS Open Forum as a full Member.

ibis@eda.org
     To send a message to the general IBIS Open Forum Reflector. This is used mostly for
     IBIS Standardization business and future IBIS technical enhancements. Job posting
     information is not permitted.

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     To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS
     clarification, current modeling issues, and general user concerns. Job posting
     information is not permitted.

ibis-bug@eda.org

       To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

       http://www.eda.org/ibis/bugs/ibischk/
       http://www.eda.org/ibis/bugs/ibischk/bugform.txt

       The BUG Report Form for tschk2 resides along with reported BUGs at:

       http://www.eda.org/ibis/tschk_bugs/
       http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

       To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

       http://www.eda.org/ibis/icm_bugs/
       http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

       http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
       http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt
       http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

       http://www.eda.org/ibis

Check the IBIS file directory on eda.org for more information on previous discussions and results:

       http://www.eda.org/ibis/directory.html

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IBIS – SAE STANDARDS BALLOT VOTING STATUS

Organization	Interest Category	Standards Ballot Voting Status	November 20, 2014	December 5, 2014	January 9, 2015	January 30, 2015
Altera	Producer	Active	-	-	X	X
ANSYS	User	Inactive	X	X	-	-
Applied Simulation Technology	User	Inactive	-	-	-	X
Cadence Design Systems	User	Active	X	X	X	X
Ericsson	Producer	Inactive	X	-	-	X
Huawei Technologies	Producer	Inactive	-	-	-	X
IBM	Producer	Inactive	-	-	-	X
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	-	X	X	X
IO Methodology	User	Active	X	X	X	X
Keysight Technologies	User	Active	-	X	X	X
Maxim Integrated Products	Producer	Inactive	-	-	-	X
Mentor Graphics	User	Active	X	X	X	X
Micron Technology	Producer	Active	X	X	X	X
Qualcomm	Producer	Active	-	-	X	X
Signal Integrity Software	User	Active	-	X	X	X
Synopsys	User	Active	-	X	X	X
Teraspeed Labs	General Interest	Active	-	X	X	X
Toshiba	Producer	Inactive	X	X	-	-
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	-	-	-
Zuken	User	Inactive	X	-	-	X

I/O Buffer Information Specification Committee (IBIS)

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH SAE BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
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- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.