

IBIS Open Forum Minutes

Meeting Date: **November 14, 2014** Meeting Location: **Shanghai, China**

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Huawei Technologies	Jinjun Li*, Xiaoging Dong, Zanglin Yuan, Han Li
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In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Meeting Number	Meeting Password
Asian IBIS Summit - Taipei -	- no teleconference
Asian IBIS Summit – Yokoha	ma – no teleconference
205 475 958	IBIS
	Meeting Number Asian IBIS Summit – Taipei – Asian IBIS Summit – Yokoha 205 475 958

For teleconference dial-in information, use the password at the following website:

https://ciscosales.webex.com/ciscosales/j.php?J=205475958

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

WELCOME AND KEYNOTE COMMENTS

The Asian IBIS Summit took place on Friday, November 14, 2014 at the Parkyard Hotel in Shanghai. Approximately 98 people from 28 organizations attended.

The statements below summarize the material presented. More details are available through the summit presentations posted online at:

http://www.eda.org/ibis/summits/nov14a/

Anders Ekholm convened the meeting and introduced Jinjun Li of Huawei Technologies for his comments. Jinjun welcomed the attendees and thanked the IBIS Open Forum for their ongoing support of the IBIS Summit series in the People's Republic of China.

Anders continued by thanking the co-sponsors: the major sponsor Huawei Technologies, ANSYS, Intel Corporation, IO Methodology, Keysight Technologies, Synopsys, Teledyne LeCroy and ZTE Corporation.

ACTIVITIES AND DIRECTION OF IBIS

Michael Mirmak (Intel Corporation, USA) [Presented by Anders Ekholm (Ericsson, Sweden)]

Anders Ekholm began by noting that the current version of IBIS is IBIS 6.0, and a parser, IBISCHK6, was released in June 2014. A user's guide for IBISCHK6 is in development from the IBIS Quality task group and a work-in-progress document is available for review. An IBIS model review service is also available. As of today, three approved BIRDs propose major changes to IBIS 6.0, while five other approved BIRDs make clarifications or corrections. Eleven other BIRDs are proposed but not approved, and these cover areas including backchannel adaptation for equalization, expanded package modeling capabilities, Touchstone support for AMI analog buffer models and parameter passing for External Circuits. A major revision of the IBIS Open Forum basic policies and procedures is also underway. Changes to the IBIS Open Forum charter will allow for greater involvement in votes and officer elections by membership companies worldwide.

HANDLING OF OVERCLOCKING CAUSED BY DELAY IN WAVEFORM TABLES

Radek Biernacki*, Ming Yang*, Randy Wolff** and Justin Butterfield** (*Keysight Technologies and **Micron Technology, USA)

[Presented by Tao Zhang (Keysight Technologies, China)]

Tao Zhang began by defining overclocking of IBIS models. He then described how power aware IBIS models can suffer from fictitious overclocking. This overclocking is imposed by EDA tools improperly handling the added delay in V-T waveforms inherent in models that include both V-T and I-T data tables. BIRD168.1 was introduced (and approved) to allow model makers to describe the intrinsic delays between pre-driver switching current and driver voltage switching. The delays can be used to define unique triggering events in the EDA software for I-T and V-T data tables.

AN EFFECTIVE SOLUTION TO SIMULATE COMPOSITE CURRENT WHEN OVERCLOCKING

Xuefeng Chen (Synopsys, China)

Xuefeng Chen began by defining [Composite Current] and describing overclocking issues with IBIS power aware models. To fix overclocking issues, he showed a modified buffer model that used superposition of [Composite Current] data tables. For instance, the model combined rising I-T and falling I-T or falling I-T and rising I-T for different R_fixture and V_fixture values. The modified I-T waveforms were used to simulate the current I(VDDQ). The new model matched well to the transistor-level model for I(VDDQ) as well as the voltage at the die pad.

TRUE DIFFERENTIAL IBIS MODEL FOR SERDES ANALOG BUFFER

Shivani Sharma, Tushar Malik and Taranjit Kukal (Cadence Design Systems, India) [Presented by Yitong Wen, (Cadence Design Systems, China)]

Yitong Wen gave an overview of current differential buffer modeling techniques in IBIS. An alternative approach to S-parameter characterization was shown using standard IBIS tabular data formats along with series elements to model differential current. This extended the approach suggested in the IBIS cookbook suggesting modeling of differential current using series resistance. A modeling flow was shown for extraction of common and differential mode impedances. From the impedance at a specific frequency one can calculate series and common mode reactances and resistances. Depending on the sign the reactance could be inductive or capacitive. A parallel RL network is then modeled using the series model type. A parallel RC network is modeled using C_comp and clamp I-V tables. The true differential model provides much better accuracy than a pseudo differential IBIS model for channel simulation in terms of jitter, eye opening and reflection losses.

BEST PRACTICES FOR HIGH-SPEED SERIAL LINK SIMULATION

Minggang Hou (ANSYS, China)

Minggang Hou presented methods for improving accuracy of serial link simulations. He began by showing how to determine the maximum bandwidth needed in a channel model based on the rise time of the signals into the model. He then emphasized the need for enough low frequency data points in a channel S-parameter model and described how to determine the minimum frequency step needed in the S-parameter model. Minggang then described passivity and causality issues with S-parameters. He concluded by saying that S-parameter data integrity is key for good signal integrity simulations.

CONNECTOR VIA FOOTPRINT OPTIMIZATION FOR 25GBPS CHANNEL DESIGN

Wenliang Dai and Zhouxiang Su (Xpeedic Technology, China) [Presented by Wenliang Dai (Xpeedic Technology, China)]

Wenliang Dai described how via discontinuities have a significant impact on channel SI. Accurate and fast via modeling using 3D full-wave EM solvers is a must for high speed channel design with IBIS-AMI. Wenliang showed how various via parameters such as antipad size, trace entry/exit layer and backdrill depth affect the channel performance. He summarized that optimal channel design requires via optimization.

USING IBIS-AMI MODEL FOR 25GBPS RETIMER SIMULATION

Maoxiang Wei, Changgang Yin and ShunLin Zhu (ZTE Corporation, China) [Presented by Changgang Yin (ZTE Corporation, China)]

Changgang Yin began by introducing IBIS-AMI models. He described the use of repeaters in long channels with too much insertion loss and how repeater models are created in IBIS-AMI. For higher data rates, retimers are used instead of repeaters. He described modeling of retimers with IBIS-AMI models. Correlation to lab measurements of a retimer AMI model was shown. Simulation results of a retimer in a 25Gbps channel were shown. He summarized how a retimer AMI model helps one estimate channel margin, pre-emphasis and equalization parameters in a serial link simulation.

IBIS AMI VALIDATION

Zilwan Mahmod and Anders Ekholm (Ericsson, Sweden) [Presented by Zilwan Mahmod (Ericsson, Sweden)]

Zilwan Mahmod began by describing design goals he has with IBIS AMI analysis. IBIS AMI models must be validated, as correct and validated models are needed. Certification is the first step a model must go through to check that the model behavior is reasonable. Zilwan presented a long checklist of items to verify. To do active correlation, the PCB model in simulation must be adjusted to match the real channel characteristics as seen in measurements. S-parameters from measurement can be used in the correlation exercise, but the PCB models need to be adjusted for later use in post-layout simulation. TX active validation is feasible, but RX active validation is not, because measurements at the decision point are not possible.

Zilwan's experience shows that many models fail certification for various reasons such as syntax errors, run time errors, simulated DC levels that don't match measured DC levels, idealized analog models, etc.

SIGNING IBIS MODEL AGAINST DDR4 SPEC

Tushar Malik and Taranjit Kukal (Cadence Design Systems, India) [Presented by Zhangmin Zhong (Cadence Design Systems, China)]

Zhangmin Zhong noted that one should certify controller IBIS models before performing system simulations. If the models do not adhere to the JEDEC DDR4 standard, a designer may wrongly associate performance issues with interconnect elements. DDR4 compliance checks can include output impedance, single-ended slew rate, differential slew rate and pulse width. A methodology was shown for testing a model against these compliance checks. Zhangmin concluded that IBIS verification against JEDEC requirements can help in quickly verifying PHY netlists for compliance and ensuring that IBIS models have been correctly make with proper netlist settings.

INTER-PAIR SKEW EFFECT ANALYSIS USING IBIS-AMI SIMULATION

Jianhua Wang, Xiaoqing Dong (Huawei Technologies, China) [Presented by Jianhua Wang (Huawei Technologies, China)]

Jianhua Wang described how intra-pair skew can come from many sources in a high speed serial link. Skew can cause resonance and degradation to differential loss SDD21 as well as DCD and common mode noise. Jianhua showed that in 20Gps+ high speed link systems, intrapair skew has more predominant impact on link BER performance, due to decreased system link margin compared to the lower speed generations. Skewed channel pulse response has the same feature as ISI induced pulse distortion, and UI-spaced equalization (particularly DFE) can help to a certain extent reduce the harm induced by channel skew. Experiments show that even when skew is approaching one UI, the link can still work under certain conditions but with much less loss compensation capability or much less margin. He concluded that AMI model based simulation is an effective approach for system evaluation in terms of skew impact analysis.

CORNER CONSIDERATIONS

Bob Ross (Teraspeed Labs, USA) [Presented by Anders Ekholm (Ericsson, Sweden)]

Anders Ekholm stated that corners mean the assignment of typ, min or max entries in IBIS models. Different areas of IBIS have different corner definitions. Anders reviewed the selection of corners for [Model]s, [External Model]s, [External Circuit]s, [Package]s and IBIS-AMI models. He noted that IBIS contains several methods to describe corners and to assign and pass parameters. Model makers should minimize parameter passing with corners because of different possible interpretations. EDA tools should be capable of mixing or matching typ, min and max conditions. He also described how L and C corner values derived from Td and Zo corners can give different "effective" ranges than desired.

CONCLUDING ITEMS

Anders Ekholm thanked the co-sponsors, presenters and attendees for their participation and support. The meeting adjourned at 5:30 PM.

NEXT MEETING

The Asian IBIS Summit in Taipei will be held November 17, 2014. The Asian IBIS Summit in Yokohama will be held November 20, 2014. No teleconferences will be available for the Summit meetings. The next IBIS Open Forum teleconference meeting will be held December 5, 2014.

NOTES

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This meeting was conducted in accordance with ANSI guidance.

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To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/ http://www.eda.org/ibis/bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/ http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/ http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eda.org/ibis

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

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IBIS – SAE STANDARDS BALLOT VOTING STATUS

		Standards Ballot				
Organization	Interest Category	Voting Status	September 12, 2014	October 3, 2014	October 24, 2014	November 14, 2014
Altera	Producer	Inactive	-	-	Х	-
ANSYS	User	Inactive	-	-	-	Х
Applied Simulation Technology	User	Inactive	-	-	-	-
Cadence Design Systems	User	Active	Х	Х	Х	Х
Ericsson	Producer	Inactive	-	-	-	Х
Huawei Technologies	Producer	Inactive	-	-	-	Х
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Inactive	Х	Х	-	-
IO Methodology	User	Active	Х	Х	Х	-
Keysight Technologies (Agilent)	User	Active	Х	Х	Х	Х
LSI (Avago)	Producer	Inactive	-	-	-	-
Maxim Integrated Products	Producer	Inactive	-	-	-	-
Mentor Graphics	User	Active	Х	Х	Х	Х
Micron Technology	Producer	Active	Х	Х	Х	-
Qualcomm	Producer	Inactive	Х	-	-	-
Signal Integrity Software	User	Active	Х	Х	Х	-
Synopsys	User	Active	-	Х	Х	Х
Teraspeed Labs	General Interest	Active	Х	Х	Х	-
Toshiba	Producer	Inactive	Х	Х	-	-
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	-	-	Х
Zuken	User	Inactive	-	-	-	-

I/O Buffer Information Specification Committee (IBIS)

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

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