IBIS Open Forum Minutes

Meeting Date: **November 19, 2013**
Meeting Location: **Taipei, Taiwan**

VOTING MEMBERS AND 2013 PARTICIPANTS

Agilent Technologies	Radek Biernacki, Pegah Alavi, Heidi Barnes, Fangyi Rao, Colin Warwick, Tarun Kalwani, Ming Yan, Xingdong Xue, Zaokai Yuan, Xianzhi Zhao, Ming-Chih Lin*, Peter Lin*
Altera	David Banas, Hsinho Wu
ANSYS	[Luis Armenta], Ben Franklin, Dan Dvorscak, Steve Pytel, Lan Chen, Timothy (Gang) Chen, Minggang Hou, Jianbo Liu, Roger Luo, Peng Wang, Shulong Wu, Guoli Yi, Daniel Chang*, Richard Chen*, Naijen Hsuan*, Charlotte Wang*, Jean Wang*, Jerry Wang*, Benson Wei*
Applied Simulation Technology	Fred Balistreri, Norio Matsui
Cadence Design Systems	[Terry Jernberg], Joy Li, Yingxin Sun, Ambrish Varma, Kevin Yao, Brad Brim, Aileen Chen, Lanbing Chen, Raymond Y. Chen, Heiko Dudek, Jiayuan Fang, Zhiqiang (Johnny) Fang, Henry He, Jinsong Hu, Li Li, Maofeng Li, Ping Liu, Yubao Meng, Zuli Qin, Aaron Tang, Haisan Wang, Yun Wang, Yitong Wen, Janie Wu, Yanrui (Clark) Wu, Dingru Xiao, Benny Yan, Wenjian Zhang, Zhangmin Zhong, *Tric Chiang, Thunder Lay*, Jack (Wei-Chang) Lin*, Paddy Wu*, Candy Yu*
Ericsson	Anders Ekholm*, Martina Fiammengo, Markus Janis*
Foxconn Technology Group	Leo Cheng*, Po-Chuan (Eric) Hsieh*, Alex Tang*
Huawei Technologies	Yu Chen, Xiaoqing Dong, Jing Fu, Chen Han, Peng Huang, Jinjun Li, Lingfei Li, Luya Ma, Xiao Peng, Xinlu Peng, Haili Wang, Shengli (Victory) Wang, Zhengrong Xu, Hongxian Yi, Gezi Zhang, Zhengyi Zhu
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Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Michael Mirmak, Mohammad Bapi, Stewart Gilbert, Ravindra Rudraraju, Kang Nan, Weifeng Shu, Ming Wei, Jimmy Hsu*, Thomas (YiRen) Su*
IO Methodology	Lance Wang*
LSI	Brian Burdick, Sarika Jain, Xingdong Dai, Anaam Ansari, Min Huang
Maxim Integrated Products	Hassan Rafat, Mahbubul Bari, Ron Olisar
Mentor Graphics	Arpad Muranyi, Ed Bartlett, Vladimir Dmitriev-Zdorov

Micron Technology	Randy Wolff
Signal Integrity Software	Walter Katz, Mike LaBonte, Mike Steinberger, Todd Westerhoff
Synopsys	John Ellis, Ted Mido, Scott Wedge, Rinsha Reghunath, Xuefeng Chen, Jinghua Huang, Yu Wang
Teraspeed Consulting Group	Bob Ross, Tom Dagostino
Toshiba	(Yasumasa Kondo)
Xilinx	(Raymond Anderson)
Zuken	Masaud Raeisi, Reinhard Remmert, Michael Schaeder, Alfonso Gambuzza

OTHER PARTICIPANTS IN 2013

Accton Technology Group	Ching-Hwei Tsend*, Xian-Wei Wang*
ASE Group	Hink Chung*, Jarris Kuo*
ASUSTek Computer	Vincent Lu*
AU Optronics Corp	Jason Kuo*, Joe Shih*
Avant Technology	Elvis Li, Linda Sun, Jyam Huang*, Enson Lee*
Bayside Design	Elliot Nahas
Celestica	Lei Liu, Fei Xue
Chinese Electronics Technology Company Institute #52 (CETC52)	Shujun Wei, Tianjiao Wu
Cisco Systems	Biao Chen, Feng Wu, Iris Zhao
Computer Simulation Technology	Heiko Grubrich
Compal Electronics	Scott C.H. Li*
Contech	Zheng Tang
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Delta Networks	Skipper Liang*
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Etrain China	Weichun Lu
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Freescale	Jon Burnett
Granite River Labs	Vamshi Kandalla, Miki Takahashi
H3C	Lichen Li, Xiaoxiang Li
Hewlett-Packard	Yongjin Choi, Ting Zhu
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Hisense	Aofeng Qian
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Inventec	Zhong Peng
KEI Systems	Shinichi Maeda
Lenovo	John Lin*, Alan Sun*
Marvell Technology Group	Weizhe Li, Fang Lv, Banglong Qian, Yuyang Wang
Mediatek	Gerald Hsu*, Fandy Huang*
Micro-Star International	Ethan Huang*, Anthony Liang*, PeterTsai*, Cloud Tseng*

Molex	Davi Correia, Greg Fu, Satish
National Instruments	Lee Mohrmann
Nokia Siemens Networks	Xuhui (Helen) Chen, Gino Guo, Gang Zheng
Novatek Microelectronics Corp	Jasper Cheng*, Willy Lin*, Frank Pai*
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Open Silicon	Norman Chang*
Pegatron Corp	Lawrence Ting*
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SAE	(Chris Denham)
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Shanghai United-Imaging	Xi Huang, Yuan Liu, Jirui Lu, Chun Yuan, Yi Zhao
Spreadtrum Communications Shanghai	Lily Dai, Steven Guo
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TechAmerica	[(Chris Denham)]
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Teradyne	Raymond Yakura
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VIA Telecom	Jen-Hung (Eddie) Lin*, Jacky Liu*
Vitesse Semiconductor	Sirius Tsang
Winbond Electronics Corp	Albert (Cheng-Han) Lee*, Marko (Chien-Cheng) Lin*
Zhejiang Uniview Technologies	Huanyang Chen, Fei Ye
ZTE Corporation	Huifeng Chen, Fengling Gao, Tao Guo, Hui Jiang, Zhi Zhou, Shunlin Zhu

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
November 22, 2013	Asian IBIS Summit - Yokohama – no telephone bridge	
December 6, 2013	205 475 958	IBIS

For teleconference dial-in information, use the password at the following website:

https://ciscosales.webex.com/ciscosales/j.php?J=205475958

All teleconference meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

WELCOME AND KEYNOTE COMMENTS
The Asian IBIS Summit took place on Tuesday, November 19, 2013 at the Sherwood Hotel in Taipei. Approximately 64 people from 28 organizations attended.

The statements below summarize the material presented. More details are available through the summit presentations posted online at:

http://www.eda.org/ibis/summits/nov13b/

Lance Wang convened the meeting and introduced Daniel Chang of ANSYS for his comments. Daniel welcomed the attendees and thanked the IBIS Open Forum for their ongoing support of the IBIS Summit series in the Republic of China.

Lance continued by thanking the co-sponsors: the major sponsor ANSYS and also the co-sponsors Cadence Design Systems, Intel Corporation, IO Methodology, and Synopsys.

INTRODUCING IBIS 6.0
Michael Mirmak (Intel Corporation, USA)
[Presented by Lance Wang (IO Methodology, USA)]

Lance Wang noted that IBIS 6.0 was released September 20, 2013. Major additions focus on IBIS-AMI including added support for redrivers and retimers and IBIS-ISS and Touchstone. The document is now easier to read and use. Lance gave detailed examples of modeling a mid-bus repeater. In IBIS 6.0, IBIS-ISS can be used to represent the complex analog buffer behavior of an AMI model. Multiple files in different locations is now supported for AMI models. Use of IBIS 6.0 improved analog modeling can help ensure model portability. Among issues to resolve is improving IBIS package modeling. Package modeling formats are being discussed with a target to include an update in the next major IBIS release. Developing an IBISCHK6 syntax parser is a focus now.

IBIS SUMMARY DOCUMENTS
Bob Ross (Teraspeed Consulting Group, USA)
[Presented by Anders Ekholm (Ericsson, Sweden)]

Anders Elkholm presented information about several documents created by Bob Ross to accompany the IBIS 6.0 specification release. IBIS 6.0 contains a keyword hierarchy tree in section 3.1. Bob updated an unofficial hierarchy document from 2007 with information from IBIS versions 5.1 and 6.0. Extra information in this document includes when items were added at major versions. Bob also created an unofficial evolution document featuring updated columns showing major version evolution, rules and changes evolution and significant subparameter selections such as the *_type subparameter choices.

Anders also noted that Bob helped create four new summary tables in section 10.7 of the IBIS 6.0 specification. These tables include Usages, Types and Formats for Reserved Parameters and Types for Format values. The summary information provides quick references for IBIS and IBIS-AMI syntax. The documents are found on the IBIS website along with the IBIS 6.0 specification.

A comment was made that we hope the IBIS committee can provide some real examples, not only the specification. Anders responded that this was a good idea. We now have some AMI models as examples. We could add others as well. We hope the chip vendors can help as well.

MODELING, EXTRACTION AND VERIFICATION OF VCSEL MODEL FOR IBIS AMI
Zhaokai Yuan (Agilent Technologies, PRC)
[Presented by Ming-Chih Lin (Agilent Technologies, ROC)]

Ming-Chih Lin began by introducing the various components of an optical Rx/Tx module. To simulate an optical link, IBIS-AMI can be extended to model the optical channel. The entire optical module is treated as a mid-channel repeater, and all optical behaviors are encapsulated inside the optical model. Ming-Chih then described the basics of the Vertical Cavity Emitting Laser (VCSEL). Ming-Chih went on to describe the principles of modeling the VCSEL's performance versus thermal behavior. Measured curves of LI, VI and frequency response were modeled using curve fitting algorithms. VCSEL model verification was then performed on two different devices and a full optical link.

A question was asked about how to use this method for long distance transmission cases. Ming-Chih responded that this method is for short distance clock transfer. Long distance transfer will need to include more effects.

ANISOTROPIC SUBSTRATES VARIANCE FOR IBIS-AMI SIMULATION
Naijen Hsuan (ANSYS, ROC)

Naijen Hsuan presented that anisotropic substrate variance is a real physical issue that leads to variation in channel characteristics for high speed SerDes channels. FR4 fiber weave creates local dielectric constant variation leading to insertion loss variation and differential pair skews. Varying the angle of the weave relative to the channel layout leads to variation in differential insertion loss, phase and return loss. Naijen setup a Design of Experiments (DOE) to look at optimizing an Rx CTLE while looking at sensitivities to anisotropic substrate

variance. Response surface modeling helped to look at a huge number of possible combinations in order to find optimal solutions. A High Performance Computing (HPC) solution also helped reduce the analysis time.

MORE ON IBIS MODELING FOR LOAD-DEPENDENT CURRENT-MODE DIFFERENTIAL DRIVERS

Lance Wang (IO Methodology, USA)

Lance Wang presented a methodology for modeling load-dependent current-mode differential pair buffers. These buffers are found increasingly often in GHz serial link designs, and traditional IBIS buffer extraction methods are not accurate enough for modeling them. Lance detailed an enhanced I-V and V-T extraction method. Correlation shows matched results between IBIS and Spice. Lance summarized that two enhancements to IBIS would be useful for these buffers. One enhancement would be to include Rref_diff/Cref_diff loads for regular IBIS differential pair models. A second enhancement when modeling dynamic PLL current mode buffers would be to include various I-V tables for different differential loads and a current dependent C_comp value table.

A comment was made that these kinds of buffers use one side with pullup and one side with pulldown for rising and falling transitions. Will this method give inaccurate results of P and N pins that are not balanced? Lance responded that this is true. However, luckily, most of these buffers are balanced.

AN ADVANCED BEHAVIORAL BUFFER MODEL WITH OVER-CLOCKING SOLUTION

Yingxin Sun and Raymond Y. Chen (Cadence Design Systems, USA)
[Presented by Thunder Lay (Cadence Design Systems, ROC)]

Thunder Lay began by describing the mechanisms related to overclocking of IBIS models. A simulator that does not properly window V-T data will give incorrect results, sometimes showing missing bits. V-T windowing works well for IBIS 4.2 models. However, for IBIS 5.0 models that include I-T data, using the same V-T windowing algorithm will cut off the pre-driver current seen in the composite current I-T data. Thunder proposed an advanced over-clocking solution, where a pre-driver stage was added to the driver stage. With this model, the composite current could be broken into two portions, the contribution from the driver and the contribution from the pre-driver. The proposed over-clocking solution could be implemented into an advanced IBIS simulator to automatically handle the windowing of both V-T and I-T data. With this solution, very good correlation was seen between IBIS and the original transistor model for real SSO simulation, even under over-clocking scenarios.

COMBINED I-V TABLE CHECKING PROBLEM

Bob Ross*, Yingxin Sun** and Joy Li** (*Teraspeed Consulting Group, **Cadence Design Systems, USA)
[Presented by Anders Ekholm (Ericsson, Sweden)]

Anders Ekholm began by describing BUG140, where unexpected non-monotonic warnings are issued for combined I-V tables. There is no specification requirement that individual or combined I-V tables be monotonic. Combined table checks were added to the IBIS parser following BUG94. Non-monotonicity often occurs outside of normal simulation regions (clamp

regions) and is not a problem for simulation software. Anders walked through a simple example to demonstrate how piecewise linear interpolation methods can cause non-monotonicities when combining two data sets. Anders then showed two test case examples from BUG140. The Quality task group discussed several options for fixes including using more complicated SPLINE fitting algorithms. The final resolution was to change the warning to a note.

IBIS MODEL FOR IO-SSO ANALYSIS

Thunder Lay and Jack W.C. Lin (Cadence Design Systems, ROC)
[Presented by Jack W.C. Lin (Cadence Design Systems, ROC)]

Jack W.C. Lin began by defining Simultaneous Switching outputs Noise (SSN). SSN impacts timing and noise margin and becomes a bigger problem as voltages decrease and data rates increase. Traditional SSN simulations can be pessimistic when the analysis excludes an on-die decoupling model or includes an estimated on-die decoupling model. An accurate RC or distributed chip PDN model is needed for realistic power/ground noise analysis. Jack showed a method of using [External Circuit] in IBIS 5.1 to incorporate on-die and package models into the buffer. Jack then showed a case study of a DDR data byte lane including a power-aware IBIS model, on-chip decoupling model and PCB and package S-parameters converted to broadband-Spice models. Without a chip PDN model, SSN is overestimated. With an on-die RC PDN model, the noise is underestimated. Using a distributed broadband model of the on-die PDN gave the most realistic results. Jack summarized that for tighter timing and noise budgets in LPDDR3 or DDR4, system level SSN analysis is helpful for design margin assessment.

CONCLUDING ITEMS

Lance Wang thanked the co-sponsors, presenters and attendees for their participation and support. The meeting adjourned at 4:30 p.m.

NEXT MEETING

The Asian IBIS Summit – Yokohama will be held November 22, 2013. The next IBIS Open Forum teleconference will be held December 6, 2013 from 8:00 to 10:00 a.m. US Pacific Time.

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NOTES

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This meeting was conducted in accordance with ANSI guidance.

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To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the IBIS Open Forum as a full Member.

ibis@eda.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/
http://www.eda.org/ibis/bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/
http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eda.org/ibis

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

IBIS – SAE STANDARDS BALLOT VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	October 11, 2013	November 1, 2013	November 15, 2013	November 19, 2013
Agilent Technologies	User	Active	X	X	X	X
Altera	Producer	Inactive	X	X	-	-
ANSYS	User	Active	-	-	X	X
Applied Simulation Technology	User	Inactive	-	-	-	-
Cadence Design Systems	User	Active	X	X	X	X
Ericsson	Producer	Active	-	-	X	X
Foxconn Technology Group	Producer	Inactive	-	-	-	X
Huawei Technologies	Producer	Inactive	-	-	X	-
IBM	Producer	Inactive	-	X	-	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	X	X	X
IO Methodology	User	Active	X	-	X	X
LSI	Producer	Inactive	X	X	-	-
Maxim Integrated Products	Producer	Inactive	-	-	-	-
Mentor Graphics	User	Inactive	X	X	-	-
Micron Technology	Producer	Inactive	X	X	-	-
Signal Integrity Software	User	Inactive	X	X	-	-
Synopsys	User	Inactive	-	-	X	-
Teraspeed Consulting	General Interest	Inactive	X	X	-	-
Toshiba	Producer	Inactive	-	-	-	-
Xilinx	Producer	Inactive	-	-	-	-
Zuken	User	Inactive	-	-	-	-

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH SAE BALLOT VOTING ARE:

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