IBIS Open Forum Minutes

Meeting Date: **November 15, 2013**
Meeting Location: **Shanghai, China**

VOTING MEMBERS AND 2013 PARTICIPANTS

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Foxconn Technology Group	(Sogo Hsu)
Huawei Technologies	Yu Chen*, Xiaoqing Dong*, Jing Fu*, Chen Han*, Peng Huang*, Jinjun Li*, Lingfei Li*, Luya Ma*, Xiao Peng*, Xinlu Peng*, Haili Wang*, Shengli (Victory) Wang*, Zhengrong Xu*, Hongxian Yi*, Gezi Zhang*, Zhengyi Zhu*
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Infineon Technologies AG	(Christian Sporrer)
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IO Methodology	Lance Wang*
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Mentor Graphics	Arpad Muranyi, Ed Bartlett, Vladimir Dmitriev-Zdorov
Micron Technology	Randy Wolff
Signal Integrity Software	Walter Katz, Mike LaBonte, Mike Steinberger, Todd Westerhoff
Synopsys	John Ellis, Ted Mido, Scott Wedge, Rinsha Reghunath,

	Xuefeng Chen*, Jinghua Huang*, Yu Wang*
Teraspeed Consulting Group	Bob Ross, Tom Dagostino
Toshiba	(Yasumasa Kondo)
Xilinx	(Raymond Anderson)
Zuken	Masaud Raeisi, Reinhard Remmert, Michael Schaeder, Alfonso Gambuzza

OTHER PARTICIPANTS IN 2013

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Bayside Design	Elliot Nahas
Celestica	Lei Liu*, Fei Xue*
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QLogic	James Zhou
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Vitesse Semiconductor	Sirius Tsang
Zhejiang Uniview Technologies	Huanyang Chen*, Fei Ye*
ZTE Corporation	Huifeng Chen*, Fengling Gao*, Tao Guo*, Hui Jiang*, Zhi Zhou*, Shunlin Zhu*

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
November 19, 2013	Asian IBIS Summit - Taipei – no telephone bridge	
November 22, 2013	Asian IBIS Summit - Yokohama – no telephone bridge	
December 6, 2013	205 475 958	IBIS

For teleconference dial-in information, use the password at the following website:

https://ciscosales.webex.com/ciscosales/j.php?J=205475958

All teleconference meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

WELCOME AND KEYNOTE COMMENTS

The Asian IBIS Summit took place on Friday, November 15, 2013 at the Parkyard Hotel in Shanghai. Approximately 109 people from 32 organizations attended.

The statements below summarize the material presented. More details are available through the summit presentations posted online at:

http://www.eda.org/ibis/summits/nov13a/

Lance Wang convened the meeting and introduced Jinjun Li of Huawei Technologies for his comments. Jinjun welcomed the attendees and thanked the IBIS Open Forum for their ongoing support of the IBIS Summit series in the People's Republic of China.

Lance continued by thanking the co-sponsors: the major sponsor Huawei Technologies, Agilent Technologies, ANSYS, Cadence Design Systems, Intel Corporation, IO Methodology, Synopsys, and Teledyne LeCroy.

INTRODUCING IBIS 6.0
Michael Mirmak (Intel Corporation, USA)
[Presented by Lance Wang (IO Methodology, USA)]

Lance Wang noted that IBIS 6.0 was released September 20, 2013. Major additions focus on IBIS-AMI including added support for redrivers and retimers and IBIS-ISS and Touchstone. The document is now easier to read and use. Lance gave detailed examples of modeling a mid-bus repeater. In IBIS 6.0, IBIS-ISS can be used to represent the complex analog buffer behavior of an AMI model. Multiple files in different locations is now supported for AMI models. Use of IBIS 6.0 improved analog modeling can help ensure model portability. Among issues to resolve is improving IBIS package modeling. Package modeling formats are being discussed with a target to include an update in the next major IBIS release. Developing an IBISCHK6 syntax parser is a focus now.

IBIS SUMMARY DOCUMENTS
Bob Ross (Teraspeed Consulting Group, USA)
[Presented by Anders Ekholm (Ericsson, Sweden)

Anders Elkholm presented information about several documents created by Bob Ross to accompany the IBIS 6.0 specification release. IBIS 6.0 contains a keyword hierarchy tree in section 3.1. Bob updated an unofficial hierarchy document from 2007 with information from IBIS versions 5.1 and 6.0. Extra information in this document includes when items were added at major versions. Bob also created an unofficial evolution document featuring updated columns showing major version evolution, rules and changes evolution and significant subparameter selections such as the *_type subparameter choices.

Anders also noted that Bob helped create four new summary tables in section 10.7 of the IBIS 6.0 specification. These tables include Usages, Types and Formats for Reserved Parameters and Types for Format values. The summary information provides quick references for IBIS and IBIS-AMI syntax. The documents are found on the IBIS website along with the IBIS 6.0 specification.

MORE ON IBIS MODELING FOR LOAD-DEPENDENT CURRENT-MODE DIFFERENTIAL DRIVERS
Lance Wang (IO Methodology, USA)

Lance Wang presented a methodology for modeling load-dependent current-mode differential pair buffers. These buffers are found increasingly often in GHz serial link designs, and traditional IBIS buffer extraction methods are not accurate enough for modeling them. Lance detailed an enhanced I-V and V-T extraction method. Correlation shows matched results between IBIS and Spice. Lance summarized that two enhancements to IBIS would be useful for these buffers. One enhancement would be to include Rref_diff/Cref_diff loads for regular IBIS differential pair models. A second enhancement when modeling dynamic PLL current mode buffers would be to include various I-V tables for different differential loads and a current dependent C_comp value table.

Someone asked in which situations this method should be used. Lance responded that this enhanced method needs to be used if the differential pair buffer has the load-dependent requirement. Otherwise, the extracted I-V and V-T curves will not be accurate.

Another question was asked if this method could be used for other kinds of differential pair buffer extractions. Lance responded that it depends. Some voltage mode differential pair buffers uses differential loads too. They could use this method as well.

COMBINED I-V TABLE CHECKING PROBLEM

Bob Ross*, Yingxin Sun** and Joy Li** (*Teraspeed Consulting Group, **Cadence Design Systems, USA)
[Presented by Anders Ekholm (Ericsson, Sweden)

Anders Ekholm began by describing BUG140, where unexpected non-monotonic warnings are issued for combined I-V tables. There is no specification requirement that individual or combined I-V tables be monotonic. Combined table checks were added to the IBIS parser following BUG94. Non-monotonicity often occurs outside of normal simulation regions (clamp regions) and is not a problem for simulation software. Anders walked through a simple example to demonstrate how piecewise linear interpolation methods can cause non-monotonicities when combining two data sets. Anders then showed two test case examples from BUG140. The Quality task group discussed several options for fixes including using more complicated SPLINE fitting algorithms. The final resolution was to change the warning to a note.

IBIS MODEL FOR IO-SSO ANALYSIS

Thunder Lay and Jack W.C. Lin (Cadence Design Systems, China)
[Presented by Zuli Qin (Cadence Design Systems, China)]

Lance Wang noted the Agenda change that this presentation is switched with the “An Advanced Behavioral Buffer Model with Over-Clocking Solution” presentation discussed below.

Zuli Qin began by defining Simultaneous Switching outputs Noise (SSN). SSN impacts timing and noise margin and becomes a bigger problem as voltages decrease and data rates increase. Traditional SSN simulations can be pessimistic when the analysis excludes an on-die decoupling model or includes an estimated on-die decoupling model. An accurate RC or distributed chip PDN model is needed for realistic power/ground noise analysis. Zuli showed a method of using [External Circuit] in IBIS 5.1 to incorporate on-die and package models into

the buffer. Zuli then showed a case study of a DDR data byte lane including a power-aware IBIS model, on-chip decoupling model and PCB and package S-parameters converted to broadband-Spice models. Without a chip PDN model, SSN is overestimated. With an on-die RC PDN model, the noise is underestimated. Using a distributed broadband model of the on-die PDN gave the most realistic results. Zuli summarized that for tighter timing and noise budgets in LPDDR3 or DDR4, system level SSN analysis is helpful for design margin assessment.

WHEN COULD PCB AND PKG PDN LUMPED LOOP INDUCTANCE BE EXTRACTED SEPARATELY?

Zhengrong Xu (Huawei Technologies, China)

Zhengrong Xu began by noting that die-package-PCB mid-frequency resonance is the crucial factor in chip self-generated power supply noise. Without an on-package-decap (OPD), the PDN mid-frequency resonance can be approximated as the simple parallel resonance of lumped Rdie-pkg-pcb, Lpkg-pcb and Cdie. The package and PCB usually come from different people, so Lpkg and Lpcb are usually extracted from S-parameters separately. Zhengrong showed a methodology for extracting inductance from the package and PCB S-parameters. He showed that for a simple package, the total PDN inductance is the summation of the package and PCB inductances. However, for a package that includes an OPD, a simple summation is not correct. In this case, the PDN inductance must be extracted from the cascaded package and PCB S-parameters.

Zhengrong concluded by noting that the IBIS package RLC model is not suitable for PDN simulation when OPDs are present. IBIS must be updated to allow use of S-parameter or Spice package models.

A question was asked how one knows the target impedance and frequency for the calculations. Zhengrong responded that normally it is provided by the IC vendors.

DDRN INTERFACE SIGNOFF ANALYSIS WITH DISTRIBUTED CHIP IO INTERCONNECT MODEL

Steven Guo*, Qin Zuli**, and Zhangmin Zhong** (*Spreadtrum, and **Cadence Design Systems, China)
[Presented by Steven Guo (Cadence Design Systems, China)]

Steven Guo began by introducing chip IO interconnection structures for a Smartphone memory subsystem, expanding upon timing budgets. He then detailed types of interconnect models for the buffer transistors, the ASIC PDN and signal interconnect, the package and the PCB. Steven then showed a case study looking at the LPDDR memory system SSO and ASIC IO power decoupling cap optimization. Analysis was done to look at noise coupled to address and clock signals from the data and strobe signals. A power integrity analysis was performed to determine the optimal value for MOS decoupling caps on the ASIC. Steven concluded that with a chip IO interconnection model, chip vendors can do more accurate DDRn signoff analysis to predict system electrical performance before ASIC tapeout.

A question was asked about how to define the worst case pattern stimulus for simulations. Steven responded that it will depend on real applications.

AN ADVANCED BEHAVIORAL BUFFER MODEL WITH OVER-CLOCKING SOLUTION
Yingxin Sun and Raymond Y. Chen (Cadence Design Systems, USA)
[Presented by Raymond Y. Chen (Cadence Design Systems, USA)]

Raymond Chen began by describing the mechanisms related to overclocking of IBIS models. A simulator that does not properly window V-T data will give incorrect results, sometimes showing missing bits. V-T windowing works well for IBIS 4.2 models. However, for IBIS 5.0 models that include I-T data, using the same V-T windowing algorithm will cut off the pre-driver current seen in the composite current I-T data. Raymond proposed an advanced over-clocking solution, where a pre-driver stage was added to the driver stage. With this model, the composite current could be broken into two portions, the contribution from the driver and the contribution from the pre-driver. The proposed over-clocking solution could be implemented into an advanced IBIS simulator to automatically handle the windowing of both V-T and I-T data. With this solution, very good correlation was seen between IBIS and the original transistor model for real SSO simulation, even under over-clocking scenarios.

A comment was made that from the presentation, one needs to treat IBIS V-T/I-T data differently from the standard way it is treated now. Is the recent IBIS model data enough for simulators to do it correctly? Raymond responded that yes, it is enough.

Xuefeng Chen of Synopsys suggested that it would be better to present a detailed solution to help everyone implement the new method in their simulators.

MODELING, EXTRACTION AND VERIFICATION OF VCSEL MODEL FOR IBIS AMI
Zhaokai Yuan (Agilent Technologies, China)

Zhaokai Yuan began by introducing the various components of an optical Rx/Tx module. To simulate an optical link, IBIS-AMI can be extended to model the optical channel. The entire optical module is treated as a mid-channel repeater, and all optical behaviors are encapsulated inside the optical model. Zhaokai then described the basics of the Vertical Cavity Emitting Laser (VCSEL). He went on to describe the principles of modeling the VCSEL's performance versus thermal behavior. Measured curves of LI, VI and frequency response were modeled using curve fitting algorithms. VCSEL model verification was then performed on two different devices and a full optical link.

ADAPTIVE CROSSTALK CANCELLATION BLOCK FOR SERDES AND ITS AMI IMPLEMENTATION
Taranjit Kukal#, Shivani Sharma#, and Zhangmin Zhong## (Cadence Design Systems, #India, ##China)
[Presented by Zhangmin Zhong (Cadence Design Systems, China)]

Zhangmin Zhong began by describing how crosstalk from neighboring channels at high frequencies causes Crosstalk-Induced Jitter (CIJ). CIJ causes FEXT and NEXT. FEXT is more dominant for PCB traces. Zhangmin showed a crosstalk cancellation block for an Rx modeled using Multiple Input Multiple Output (MIMO) modeling. There is a need for adaptive crosstalk cancellation, where the crosstalk coupling coefficient is determined on the fly based on crosstalk activity, and if the coupling coefficient is too small the cancellation scheme can be switched off to save power. Zhangmin then described adaptive CIJ cancellation using an AMI

implementation. Simulation results showed improvements to BER. He concluded that since CIJ is pattern dependent, it is important that crosstalk cancellation adapt itself based on data-induced jitter.

A question was asked if this noise cancelling methodology has been used in a real application. Zhangmin responded that it has not yet, but it just passed validation and will be implemented soon.

ANISOTROPIC SUBSTRATES VARIANCE FOR IBIS-AMI SIMULATION
Naijen Hsuan (ANSYS, China)
[Presented by Minggang Hou (ANSYS, China)]

Minggang Hou presented that anisotropic substrate variance is a real physical issue that leads to variation in channel characteristics for high speed SerDes channels. FR4 fiber weave creates local dielectric constant variation leading to insertion loss variation and differential pair skews. Varying the angle of the weave relative to the channel layout leads to variation in differential insertion loss, phase and return loss. Minggang setup a Design of Experiments (DOE) to look at optimizing an Rx CTLE while looking at sensitivities to anisotropic substrate variance. Response surface modeling helped to look at a huge number of possible combinations in order to find optimal solutions. A High Performance Computing (HPC) solution also helped reduce the analysis time.

A question was asked referring to slide 9. How dense does one need to model the substrate weave? It appears to be very coarsely modeled in the picture shown. Minggang responded that the picture has been enlarged a lot. It should be modeled as the real substrate, since it is a very fine structure.

CONCLUDING ITEMS
Lance Wang thanked the co-sponsors, presenters and attendees for their participation and support. The meeting adjourned at 5:30 PM.

NEXT MEETING
The Asian IBIS Summit – Taipei will be held November 19, 2013. The Asian IBIS Summit – Yokohama will be held November 22, 2013. The next IBIS Open Forum teleconference will be held December 6, 2013 from 8:00 to 10:00 AM US Pacific Time.

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NOTES

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This meeting was conducted in accordance with ANSI guidance.

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In the body, for the IBIS Open Forum Reflector:
subscribe ibis <your e-mail address>

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Help and other commands:

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ibis-request@eda.org

To join, change, or drop from either or both:
IBIS Open Forum Reflector (ibis@eda.org)
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State your request.

ibis-info@eda.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the IBIS Open Forum as a full Member.

ibis@eda.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/
http://www.eda.org/ibis/bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/
http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eda.org/ibis

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

IBIS – SAE STANDARDS BALLOT VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	September 20, 2013	October 11, 2013	November 1, 2013	November 15, 2013
Agilent Technologies	User	Active	X	X	X	X
Altera	Producer	Active	-	X	X	-
ANSYS	User	Inactive	-	-	-	X
Applied Simulation Technology	User	Inactive	-	-	-	-
Cadence Design Systems	User	Active	X	X	X	X
Ericsson	Producer	Inactive	-	-	-	X
Foxconn Technology Group	Producer	Inactive	-	-	-	-
Huawei Technologies	Producer	Inactive	-	-	-	X
IBM	Producer	Inactive	-	-	X	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	X	X	X
IO Methodology	User	Active	X	X	-	X
LSI	Producer	Active	X	X	X	-
Maxim Integrated Products	Producer	Inactive	-	-	-	-
Mentor Graphics	User	Active	X	X	X	-
Micron Technology	Producer	Active	X	X	X	-
Signal Integrity Software	User	Active	X	X	X	-
Synopsys	User	Inactive	-	-	-	X
Teraspeed Consulting	General Interest	Active	X	X	X	X
Toshiba	Producer	Inactive	-	-	-	-
Xilinx	Producer	Inactive	-	-	-	-
Zuken	User	Inactive	-	-	-	-

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

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