IBIS Open Forum Minutes

Meeting Date: **November 16, 2012**
Meeting Location: **Yokohama, Japan**

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Yamaha	Masahiro Tsukuda*
Yamaichi Electronics Co.	Masahi Iwata*
Yazaki	Kazuki Hattron*
YDC	Yoshiaki Manabe*
YDK Co.	Yoshio Takemura*
Zhejiang United Electronic Industry	Gang Xu
Zhejiang Uniview Technologies	Sunny (Huanyang) Chen, Phil (Fei) Ye

Zuiki Seikoh Go*

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
November 30, 2012	205 475 958	IBIS

For teleconference dial-in information, use the password at the following website:

https://ciscosales.webex.com/ciscosales/j.php?J=205475958

All teleconference meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

WELCOME AND KEYNOTE COMMENTS

The IBIS Open Forum summit was held in Yokohama, Japan, co-located with the Electronics Design Solutions Fair (EDS Fair) at the Pacifico Yokohama Conference Center. About 156 people representing 86 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda.org/pub/ibis/summits/nov12c/

Lance Wang opened the seventh Asian IBIS Summit in Yokohama, Japan. Haruhiko Saitoh (JEITA EC Working Group Chair and Sony Corporation) welcomed everyone and looked forward to a productive meeting. Lance Wang provided some brief remarks, thanked JEITA for their support and providing excellent facilities.

IBIS 5.1: AN OVERVIEW

Michael Mirmak (Intel Corporation, USA)
[Presented by Lance Wang (IO Methodology, USA)]

Lance Wang announced that IBIS 5.1 was approved on August 24, 2012. It has been reformatted based on Microsoft Word for ease of editing, changes (BIRDs), readability, and cross-referencing with hyperlinks. ASCII figures and tables are replaced with graphics and actual tables. The terminology has been made more consistent. Lance showed a list of 25 BIRDs that have been incorporated to support new features and changes. The AMI parameter discussion that was in Section 6C has been moved to a new section 10A. While old AMI files will still work, there are some flow changes to support non-LTI models in TX AMI_GetWave. Use_Init_Output is deprecated for AMI_Ver 5.1 files depicted by using the AMI_Version parameter.

Lance showed some of the format changes and also announced the ibischk5 parser, Version 5.1.2 was released October 6, 2012 to support checking IBIS Version 5.1 and .ami files. The next steps for specification updates include renumbering the sections and incorporating new BIRDs written in the new format. The next major Version is 6.0, but Version 5.2 might be issued for standardization only.

IBIS PARSER UPDATE
Bob Ross (Teraspeed Consulting Group, USA)
[Presented by Anders Ekholm, Ericsson Sweden)]

Anders Ekholm showed the valid IBIS Version numbers through 5.1 and also the latest ibischk versions through Version 5.1.2. Specifications are upgraded to the last major version. Downward compatibility is maintained for features and syntax so that existing models remain valid.

IBIS-AMI started supporting sub-version distinctions in the .ami format. AMI_Version is required for “5.1” files and Use_Init_Output is not legal.

Anders gave a brief overview of ibischk5 Version 5.1.2 and showed its flags. There are over 1150 unique numbered error message strings. The source code package has 44 new test case files since Version 5.0.7. Ibischk Version 5.1.2 checks many more errors than the older Version 5.0.7 as a result of 23 BIRDs and 13 BUG reports that impact the parser.

Anders described briefly the tschk2 parser that checks both Touchstone Version 1.0 and Touchstone Version 2.0 files.

Anders concluded that the parsers officially check files for specification compliance and are critical to IBIS success.

S-PARAMETER: WHAT YOU CAN READ, WHAT YOU HAVE TO READ
Shinichi Maeda (KEI Systems, Japan)

Shinichi Maeda presented an overview of S-parameter models including their definition and examples of gain and phase information. He showed gain and phase plots for a capacitor, and inductor, and two different length transmission lines. He noted that phase information is important because two networks could have very similar gain but very different phase. S-parameters can be n-Port models to represent large systems. Shinichi showed an example of a 4-port model of two single ended lines and defined forward and backwards crosstalk. S-

parameters can also be in a differential format that shows the common mode, differential mode and common-to-differential mode characteristics. Common problems of S-parameter data include not defining the DC point and dealing with extrapolation when a higher frequency range is needed for simulation.

CHIP PDN MODEL FOR POWER AWARE SIGNAL INTEGRITY ANALYSIS
Jack W.C. Lin#, and Raymond Y. Chen## (Cadence Design Systems, #China, ##USA)
[Presented by Yukio Masuko (Cadence Design Systems, Japan)]

Yukio Masuko described traditional SSO analysis with traditional IBIS and showed artificially large power/ground fluctuations. On die RC decoupling capacitors reduce the fluctuations. A chip PDN helps identify mid-frequency resonance. This could add to larger power ground noise and worse digital quality. IBIS Version 5.0 is currently limited because it lacks a direct RC decoupling network.

Some chip PDN capacitance comes from the driver transistors and another part comes from outside of the transistors. For example, MIMCAPs on an interposer can contribute sizable capacitance. Yukio showed how to generate a chip PDN model (as proposed earlier by Sigrity) for the driver transistors. Outside the transistors, the PDN capacitance can be extracted by I/O circuit bus groups. This can be modeled as an RC model or a distributed Spice model. Yukio showed a case study using PDN in SSO analysis (with an RC model and distributed Spice model) that showed realistic power/ground noise versus artificially high noise for the case without a PDN.

Yukio also illustrated a BIRD proposal that uses the [Pin Mapping] busses to map bus name to subcircuit nodes through a [Define Chip PDN Model] keyword and [External Model].

THE VOICE FROM PRACTICAL DESIGNING WITH SI SIMULATION
Hironari Kibe (Zuken, Japan)

Hironari Kibe noted that it is more common for layout designers to consider Signal Integrity and to increase their usage of IBIS models. His presentation introduced frequently asked questions of an EDA vendor support center related to IBIS models. The first question defined flight time and when it begins and ends. The second question he answered was why flight time can be negative. The third question clarified the relationship between [Package], [Pin] and [Package Model] keyword data. The fourth question answered how a simulator uses more than one set of [Rising Waveform] and [Falling Waveform] data. The fifth question clarified what to do when two simulators show different results. Hironari noted that the problems come from different options settings between the simulators about 60% of the time. There is also an “IBIS Quality Framework” provided by the JEITA/EC Center that is helpful to follow before calling a support center. Hironari concluded that we need to create for “frameworks” to educate users and to enhance IBIS models.

IBIS VALIDATION METHOD REVIEW
Lance Wang (IO Methodology, USA)

Lance Wang described how system design engineers need validated IBIS models to analyze high speed designs. The IBIS Accuracy Specification was originally released in 1998. In 2007,

the IBIS Quality task group was formed. This group has released IBIS Quality specifications and a Quality checklist. In recent years, many system companies started to ask their device vendors to supply quality control documents for their IBIS models.

The goal of IBIS validation is to correlate IBIS model simulation results with golden sources (measurements and simulations) for specific test loads. Commonly used correlation/comparison methods include the quality checklist, curve overlay or envelope metrics, threshold based metrics and differential index based metrics. Lance detailed pros and cons of each of the methods and presented several common mistakes in the validation process.

Lance concluded that validation is best done by IBIS model vendors. Comparison methods vary and must be used wisely to fit buffer model needs. IBIS users should ask their vendors for reasonable validation reports.

OVER-CLOCKING MODEL VALIDATION
Yasuki Torigoshi (Toshiba Corporation, Japan)

Yasuki Torigoshi defined overclocking of an IBIS model as a simulation where the bit length is shorter in time duration than the [Rising Waveform] and/or [Falling Waveform] data. Overclocking of models can create waveform problems, and the IBIS Cookbook recommends avoiding the situation. Yasuki showed simulation results comparing many model variations with different length V-t curves. Removing initial delays and cutting the V-t waveform tails showed varying results comparing IBIS simulations to Spice simulations. Yasuki concluded that we need to improve the IBIS specification as it relates to waveform overclocking. This is especially true since IBIS 5.0 models that include [Composite Current] data will have long waveforms. He recommended leaving waveform cutting up to simulators.

DESIGNING DDR3 SYSTEM USING STATIC TIMING ANALYSIS IN CONJUNCTION WITH IBIS SIMULATION
Taranjit Kukal#, Zhangmin Zhong##, and Heiko Dudek### (Cadence Design Systems, #India, ##China, and ###Germany)
[Presented by Hirotsugu Ueno (Cadence Design Systems, Japan)]

Hirotsugu Ueno described how DDR3 board design requires exploration of a large solution space including timing budgets, signal quality, component selection and stack-up and layout constraints. There are multiple constraints across timing and signal integrity. Timing closure across reads, writes and address is challenging. Signal integrity (SI) also affects timing. Ad-hoc analysis and verification leads to non-optimal designs. A unified static timing analysis and SI flow produces better designs. SI simulations feedback into the static timing analysis. Hirotsugu presented several use cases. Hirotsugu concluded that DDR3 compliance requires multiple specifications to be met covering timing and SI measurements. Timing models should be able to handshake data with IBIS simulations at pre-route exploration and post-route verification stages to ensure that both SI and timing constraints are met.

THE APPLICATION OF SIMULATION KIT USING USB3.0 IBIS-AMI MODEL
Motoaki Matsumura (Fujitsu Semiconductor, Japan)

Motoaki Matsumura detailed the process used to design, build and verify a USB3.0 interface. His conclusion was that using IBIS-AMI models enabled high accuracy and short turnaround time. Using IBIS-AMI models allowed for simulation of one million bits in ½ hour. This compares to only 1000 bits of simulation using Spice models. Using a simulation test kit with his EDA software also improved the process. He noted that model makers should verify the quality of their own IBIS-AMI models (on different OS's and EDA tools), since users can not correct or modify IBIS-AMI black-box models. He also had an issue with some EDA tools when the Continuous Time Linear Equalizer (CTLE) circuit characteristics were represented with an S-parameter model instead of inside of the IBIS-AMI model. Tool dependences with Samples Per Bit also caused problems. Sometimes the recommended value is not the default value in the model.

Motoaki showed good correlation between simulation and measurement results. He also was able to examine cost reduction of the product by using the simulation kit and IBIS-AMI models due to the short simulation times. Motoaki concluded that IBIS-AMI is a key technology for USB3.0 analysis at 5Gbps. IBIS-AMI model makers need to solve various problems between the models and the EDA tool before model release. He also expects to see more information about IBIS-AMI including documents such as a cookbook and troubleshooting guide, more samples of simulation results accompanying models, and visualization of EQ characteristics.

CONCLUDING ITEMS

Lance Wang thanked the attendees and co-sponsors and JEITA for sponsoring and arranging the meeting. The meeting adjourned at approximately 6:00 PM.

NEXT MEETING

The next IBIS Open Forum teleconference will be held November 30, 2012 from 8:00 to 10:00 AM US Pacific Time.

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NOTES

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This meeting was conducted in accordance with the TechAmerica Legal Guides and TechAmerica Manual of Organization and Procedure.

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In the body, for the IBIS Open Forum Reflector:
subscribe ibis <your e-mail address>

In the body, for the IBIS Users' Group Reflector:
subscribe ibis-users <your e-mail address>

Help and other commands:
help

ibis-request@eda.org

To join, change, or drop from either or both:
IBIS Open Forum Reflector (ibis@eda.org)
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State your request.

ibis-info@eda.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the IBIS Open Forum as a full Member.

ibis@eda.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/
http://www.eda.org/ibis/bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/
http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eda.org/ibis

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

To create an account on the TechAmerica KAVI workspace, check out:

http://workspace.techamerica.org/kwspub/join/

IBIS CURRENT MEMBER VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	October 26, 2012	Novembe r 9, 2012	November 13, 2012	November 16, 2012
Agilent Technologies	User	Active	X	X	X	X
Altera	Producer	Inactive	-	-	-	-
ANSYS	User	Active	-	X	X	X
Applied Simulation Technology	User	Inactive	-	-	-	-
ARM	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Active	X	X	X	X
Ericsson	Producer	Active	X	X	X	X
Foxconn Technology Group	Producer	Inactive	-	-	X	-
Freescale	Producer	Inactive	-	-	-	X
Huawei Technologies	Producer	Inactive	-	X	-	-
IBM	Producer	Inactive	X	-	-	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	X	X	-
IO Methodology	User	Active	X	X	X	X
LSI	Producer	Inactive	-	-	-	-
Maxim Integrated Products	Producer	Inactive	-	-	-	-
Mentor Graphics	User	Inactive	X	-	-	X
Micron Technology	Producer	Inactive	X	-	-	-
Nokia Siemens Networks	Producer	Inactive	-	X	-	-
QLogic	Producer	Inactive	-	-	-	-
Signal Integrity Software	User	Inactive	X	-	-	-
Sigrity	User	Inactive	-	-	-	-
Synopsys	User	Inactive	-	X	-	-
Teraspeed Consulting	General Interest	Inactive	X	-	-	-
Texas Instruments	Producer	Inactive	-	-	-	-
Toshiba	Producer	Inactive	-	-	-	X
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	X	-	-
Zuken	User	Inactive	-	-	-	X

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH TECHAMERICA BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
- PRODUCERS - MEMBERS THAT SUPPLY ELECTRONIC EQUIPMENT.
- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.