IBIS Open Forum Minutes

Meeting Date: **November 9, 2012**
Meeting Location: **Shanghai, China**

VOTING MEMBERS AND 2012 PARTICIPANTS

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ARM	(Nirav Patel)
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Foxconn Technology Group	(Sogo Hsu)
Freescale	(Jon Burnett)
Huawei Technologies	Xiaoqing Dong*, Chunxing Huang*, Peng Huang* Hongxin Jiang*, Wenjin Luo*, Longfang Lv*, Luya Ma*, Xiao Peng*, Huichao Weng*, Zhengrong Xu*, Juhua Yu*, Fangfang Zhang*
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IO Methodology	Lance Wang*
LSI	Brian Burdick
Maxim Integrated Products	Hassan Rafat, Mahbubul Bari
Mentor Graphics	Arpad Muranyi, Vladimir Dmitriev-Zdorov
Micron Technology	Randy Wolff, Aniello Viscardi, Francesco Madonna Antonio Prisco, Justin Butterfield
Nokia Siemens Networks GmbH	Eckhard Lenski, Evis Minga, Bruce (Zhenshui) Qin*, Feiqin Shen*, Yuanzhi Xu*, Jieping Zhang*, XiuYing (Echo) Zhou*
QLogic	(James Zhou)

Signal Integrity Software	Walter Katz, Mike LaBonte, Todd Westerhoff Akalu Lentiro
Sigrity	[Raymond Chen], Yingxin Sun, Sam Chitwood Ben Franklin, Srdjen Djordjevic
Synopsys	Andy Tai, Scott Wedge, Hany Elhak, Ted Mido, Xuefeng Chen*, Jinhua Huang*, Huihuang Li*
Teraspeed Consulting Group	Bob Ross, Tom Dagostino
Texas Instruments	Casey Morrison, Pegah Alavi, Valerie Chang Modesto Garcia, Karl Muth
Toshiba	Masatoshi Abe
Xilinx	Harry Fu
ZTE	Huifeng Chen*, Xiaolin Chen*, Fengling Gao*, Hui Jiang*, Wan Ming*, Qi Ni*, Anbing Sun*, Lili Wei*, Shunlin Zhu*
Zuken	Michael Schaeder

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Aruba Networks	Amir Motamedi
Avago Technologies	Sanjeev Gupta, Amolak Badesha
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Cavium	Johann Nittmann
Celestica	Lily Dai*, Jason Liu*, Ivan (Yunqiang) Meng*, Harrison Xue*, Lobo Zhang*, Van Zhu*
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Enea Group	Xiaoliang Gao*
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SWIEE Electronics	Chen Gao*
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Université de Brest	Mihai Telescu, Cherif Diouf
University of Illinois	Thomas Comberiate, José Schutt-Ainé
Vitesse Semiconductor	Sirius Tsang
Zhejiang United Electronic Industry	Gang Xu*
Zhejiang Uniview Technologies	Sunny (Huanyang) Chen*, Phil (Fei) Ye*

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
November 13, 2012	Asian IBIS Summit - Hsinchu – no telephone bridge	
November 16, 2012	Asian IBIS Summit - Yokohama – no telephone bridge	
November 30, 2012	205 475 958	IBIS

For teleconference dial-in information, use the password at the following website:

https://ciscosales.webex.com/ciscosales/j.php?J=205475958

All teleconference meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

WELCOME AND KEYNOTE COMMENTS
The Asian IBIS Summit took place on Friday, November 9, 2012 at the Parkyard Hotel in Shanghai. Approximately 109 people from 32 organizations attended.

The statements below summarize the material presented. More details are available through the summit presentations posted online at:

http://www.eda.org/ibis/summits/nov12a/

Lance Wang convened the meeting and introduced Chunxing Huang of Huawei Technologies for his comments. Chunxing welcomed the attendees and thanked the IBIS Open Forum for their ongoing support of the IBIS Summit series in the People's Republic.

Lance continued by thanking the co-sponsors: the major sponsor Huawei Technologies, Agilent Technologies, ANSYS, Cadence Design Systems, Intel Corporation, IO Methodology, Synopsys, Teledyne LeCroy, and ZTE Corporation.

IBIS 5.1: AN OVERVIEW
Michael Mirmak (Intel Corporation, USA)
[Presented by Lance Wang (IO Methodology, USA)]

Lance announced that IBIS 5.1 was approved on August 24, 2012. It has been reformatted based on Microsoft Word for ease of editing, changes (BIRDs), readability, and cross-referencing with hyperlinks. ASCII figures and tables are replaced with graphics and actual tables. The terminology has been made more consistent. Lance showed a list of 25 BIRDs that have been incorporated to support new features and changes. The AMI parameter discussion that was in Section 6C has been moved to a new section 10A. While old AMI files will still work, there are some flow changes to support non-LTI models in TX AMI_GetWave. Use_Init_Output is deprecated for AMI_Ver 5.1 files depicted by using the AMI_Version parameter.

Lance showed some of the format changes and also announced the ibischk5 parser, Version 5.1.2 was released October 6, 2012 to support checking IBIS Version 5.1 and .ami files. The next steps for specification updates include renumbering the sections and incorporating new BIRDs written in the new format. The next major Version is 6.0, but Version 5.2 might be issued for standardization only.

In response to a question, ibischk5 does not check .dlls. It does check .ami files. Another person asked if timing will be put in IBIS. Lance responded that no proposal exists for timing, but several presentations discuss the topic.

USING LATENCY INSERTION METHOD TO HANDLE IBIS MODELS

Ping Liu*#, Jilin Tan*##, Jose Schutt-Aine** (*Cadence Design Systems, #China, ##USA; **University of Illinois, USA)

Ping Liu indicated that the traditional way of setting up IBIS simulations is to apply Newton-Raphson techniques combined with modified nodal analysis. However, the results may be unpredictable and not even converge. A Latency Insertion Method introduced here has many advantages including no convergence issues, linear numerical complexity, speed, and no ill-conditioning problems. For large-scaled networks, a “leapfrog” scheme (current to voltage to current to voltage, etc.) is used to solve for node voltages and branch currents. Nodes must have a shunt capacitor, and branches must have a series inductor.

Ping showed how this can be extended to the IBIS buffer simulation based on two equations, two unknowns, and Ku and Kd calculations can be reformulated using an explicit leapfrog method. The IBIS simulation converges in cases where the Newton Raphson method does not. Ping also showed how this formulation can be extended to handle [ISSO_PU] and [ISSO_PD] tables per BIRD98. The formulation can also be used for handling composite currents described in BIRD95.

Someone commented that Latency Insertion Method requires a ground capacitance even if none is given and then asked how the value is determined. Ping responded that in practice a value of 1/10,000 of the smallest capacitor is used when initializing.

CHANNEL SIMULATION PLATFORM CREATION IN MATLAB AND IBIS-AMI SIMULATION VERIFICATION

Jason Liu*, Harrison Xue*, Benny Yan** (*Celestica, **Cadence Design Systems, China)

Harrison Xue indicated that equalization (FFE, CTLE and DFE) can improve the quality of the eye for 10+ Gbps signal rates. The key to choosing an equalizer is not to just evaluate the characteristics of a lossy channel, but also to evaluate the characteristics of the equalizers. Harrison introduced the channel simulation platform flow and also showed an example of a Feed-Forward Equalizer (FFE) and a Decision Feedback Equalizer (DFE). He also showed an expression for Continuous Time Linear Equalizer (CTLE).

The Channel Pulse Response (CPR) is used to evaluate the channel and also to determine which equalization should be used in the channel. Harrison showed a plot with several equalization methods and gave a formula to evaluate CPR. An eye may be improved by combining equalization methods instead of by using just one. Total Jitter (TJ) can be modeled as Random Jitter (RJ) convolved with Deterministic Jitter (DJ). DJ can be modeled as a Dual-Dirac model. Harrison showed good eye correlations with an EDA tool and a MatLab reference simulation for both the vertical voltages and horizontal Unit Intervals for six cases. The best results were with emphasis and CTLE. He also stated that the capability of an equalizer can be determined.

In response to a question, Harrison referred to the formula on slide 7 to narrow the values for quick optimization.

EFFECT ANALYSIS OF IL REASONANCE BETWEEN 0.5~1 NORMALIZED FREQUENCY BANDWIDTH

Chunxing Huang, Xiaoqing Dong, Lan Yu (Huawei Technologies, China)

Chunxing Huang stated that when data rates move to 25 Gbps, it is difficult to control stub length. Resonance is likely to appear in insertion loss (IL) between half Baud-rate and Baud-rate frequencies. He showed channels A without resonances and channels B with resonances between 16 GHz and 25 GHz. For a system operating at 25 Gbps, most of the IL characteristics should be determined by the frequency characteristics from 0 to 0.5 normalized baud rate. So the resonances for the two channels should have little effect.

However, Chunxing analyzed and compared the two channels with IL resonance at 0.5 to 1 normalized frequencies and without such resonances with pulse response analysis and full channel simulation.

Pulse response analysis showed more resonances at post-cursors (2, 3, 4, 5), and ISI would be hard to compensate by equalization. SerDes RX would see a relatively blurred eye and clock data recovery (CDR) would show increased jitter. Chunxing showed actual full channel simulation results for constructed S-parameter ILs measured at 12.5 GHz in 2 dB increments. The eye height degraded significantly. The driving capability degraded from 38 dB to 25 dB. So, resonances between 0.5 and 1 normalized frequency should be removed because of their effect on the system performance.

One person asked about experiences with CFE at 10 GHz. The answer is that 10 GHz CFE is different than 30 GHz CFE.

EFFICIENT END-TO-END SIMULATIONS OF 25G OPTICAL LINKS

Jing-Tao Liu*#, Fangyi Rao*##, Sanjeev Gupta**, Amolak Badesha** (*Agilent Technologies, # China, ##USA; **Avago Technologies, USA)

Jing-Tao Liu indicated that above 25G (25 Gbps), the traditional electrical link is limited by channel losses. Optical channels have advantages including smaller loss and superior bandwidth, flawless connectivity between digital boards and backplanes, smaller footprints, and reduced EMI. Jing-Tao showed an optical link system and gave some of the challenges to model the electrical and optical portions of the link with IBIS-AMI simulation methodology. He illustrated the IBIS-AMI flow and gave advantages and disadvantages. One concern is that channels are assumed to be linear, but optical channels are strongly non-linear and noisy.

The solution is to treat the entire optical module as a mid-channel repeater and extend IBIS-AMI simulation to include the repeater. Jing-Tao showed the full channel optical link simulation flow and then gave some electrical details of the VCSEL optical model and corresponding equations. He then showed 25G optical channel simulation results (eye diagrams, bathtub curves, and optical noise effects, temperature effects, and non-linear effects, and fiber effects). Jing-Tao concluded that IBIS-AMI methodology is applied to model and simulate the optical channels and provides many advantages for end-to-end optical link analysis.

ANALYSIS OF THE IMPACT OF CROSSTALK IN HIGH-SPEED SERIAL LINKS
Anbing Sun, Changgang Yin, Wei Jia (ZTE Corporation, China)

Anbing Sun stated that crosstalk at 10 Gbps and above is inevitable because of smaller risetimes and impedance mismatches. In a SerDes system crosstalk is described in IEEE802.3ap as far-end crosstalk (FEXT), near-end crosstalk (NEXT) and an insertion loss to crosstalk ratio (ICR).

BGA fanout area, connectors, parallel traces, and other vias in the channel all can contribute to crosstalk in a high-speed system. Often the focus is on connectors, but the BGA fanout area is becoming an important contributor.

Anbing described modeling crosstalk analysis for three BGA patterns. They had different fanout patterns, distance between pairs, and via lengths. S4p S-parameters are extracted by measurement or by an EM field solver as part of the flow. Anbing described the setup and showed simulation results for the three patterns and compared them with 0 crosstalk, 1-times crosstalk and 2-times crosstalk. This comparison showed that the BGA fanout area is not negligible.

In response to a question, the best fanout structure needs to be determined based on your specific design.

VERIFICATION OF ICN USABILITY IN CHARACTERIZING SYSTEM CROSTALK
Xiaoqing Dong, Chunxiang Huang (Huawei Technologies, China)

Xiaoqing Dong defined ICN as Integrated Crosstalk Noise, and this was defined in early cable standard and is currently in 802.3bj. She gave equations for some terms to determine if ICN is usable in characterizing link crosstalk noise through test comparisons for 25G (25 Gbps) applications. Total ICN is the RMS sum of ICN-next and ICN-fext. She then posed several ICN usability questions and verification tests.

Xiaoqing showed the setup and results of three experiments for single crosstalk ICN usability. Based on these experiments she summarized that ICN data correlates well when crosstalk noise is not near the scope noise floor. Test accuracy is degraded when the crosstalk noise is near the scope noise floor, but ICN calculation is still valid.

Xiaoqing also showed results for multi-cross talk RMS sum verification and ICN RMS sum verification. She also concluded that the ICN RMS algorithm is valid.

She gave three overall findings. The PRBS31 pattern should be used for the aggressor data for the ICN metric. The RMS value of crosstalk noise should be measured instead of peak-to-peak noise. In cases where the scope noise floor is significant, the ICN calculation can be used to get crosstalk noise data. Furthermore, it is recommended to use ICN as an input parameter for stress channel simulation in high speed links and to help users generate ICN masks of their links for different SerDes models. ICN noise can be represented by Gaussian white noise.

Several questions were asked regarding the measurement setup.

CHIP PDN MODEL FOR POWER AWARE SIGNAL INTEGRITY ANALYSIS
Jack W.C. Lin#, Raymond Y. Chen## (Cadence Design Systems, #China, ##USA)
[Presented by Haisan Wang (Cadence Design Systems, China)

Haisan Wang described traditional SSO analysis with traditional IBIS and showed artificially large power/ground fluctuations. On die RC decoupling capacitors reduce the fluctuations. A chip PDN helps identify mid-frequency resonance. This could add to larger power ground noise and worse digital quality. IBIS Version 5.0 is currently limited because it lacks a direct RC decoupling network.

Some chip PDN capacitance comes from the driver transistors and another part comes from outside of the transistors. For example, MIMCAPs on an interposer can contribute sizable capacitance. Haisan showed how to generate a chip PDN model (as proposed earlier by Sigrity) for the driver transistors. Outside the transistors, the PDN capacitance can be extracted by I/O circuit bus groups. This can be modeled as an RC model or a distributed Spice model. Haisan showed a case study using PDN in SSO analysis (with an RC model and distributed Spice model) that showed realistic power/ground noise versus artificially high noise for the case without a PDN.

Haisan also illustrated a BIRD proposal that uses the [Pin Mapping] busses to map bus name to subcircuit nodes through a [Define Chip PDN Model] keyword and [External Model].

IBIS PARSER UPDATE
Bob Ross (Teraspeed Consulting Group, USA)
[Presented by Anders Ekholm (Ericsson, Sweden)]

Anders Ekholm showed the valid IBIS Version numbers through 5.1 and also the latest ibischk versions through Version 5.1.2. Specifications are upgraded to the last major version. Downward compatibility is maintained for features and syntax so that existing models remain valid.

IBIS-AMI started supporting sub-version distinctions in the .ami format. AMI_Version is required for “5.1” files and Use_Init_Output is not legal.

Anders gave a brief overview of ibischk5 Version 5.1.2 and showed its flags. There are over 1150 unique numbered error message strings. The source code package has 44 new test case files since Version 5.0.7. Ibischk Version 5.1.2 checks many more errors than the older Version 5.0.7 as a result of 23 BIRDs and 13 BUG reports that impact the parser.

Anders described briefly the tschk2 parser that checks both Touchstone Version 1.0 and Touchstone Version 2.0 files.

Anders concluded that the parsers officially check files for specification compliance and are critical to IBIS success.

IBIS VALIDATION METHOD REVIEW
Lance Wang (IO Methodology, USA)

Lance Wang described how system design engineers need validated IBIS models to analyze high speed designs. The IBIS Accuracy Specification was originally released in 1998. In 2007, the IBIS Quality task group was formed. This group has released IBIS Quality specifications and a Quality checklist. In recent years, many system companies started to ask their device vendors to supply quality control documents for their IBIS models.

The goal of IBIS validation is to correlate IBIS model simulation results with golden sources (measurements and simulations) for specific test loads. Commonly used correlation/comparison methods include the quality checklist, curve overlay or envelope metrics, threshold based metrics and differential index based metrics. Lance detailed pros and cons of each of the methods and presented several common mistakes in the validation process.

Lance concluded that validation is best done by IBIS model vendors. Comparison methods vary and must be used wisely to fit buffer model needs. IBIS users should ask their vendors for reasonable validation reports.

A question was asked about how to validate IBIS models without a Spice circuit. Lance responded that IBIS I-V and V-t curves should be consistent. This is one thing you can check without a Spice circuit.

THE EVOLUTION OF DDR MEMORY AND OVERCOMING CHALLENGES OF DDR3/4 DESIGN

Steven Pytel (ANSYS, USA)
[Presented by Baolong Li, (ANSYS, China)

Baolong Li showed a chart detailing the changes in operating voltages and memory speeds for SDR SDRAM through the most recent DDR4 SDRAM technologies. The DDR4 standard was announced in September 2012. DDR4 uses a 1.2V supply voltage and has significant changes to the operation of the data signals as compared to DDR3.

The analysis of DDRX technologies involves significant complexity including large amounts of output data in reports. Accurate system level analysis of performance must include accurate package, PCB and connector extractions. Accurate die models are needed including IBIS models plus current modeling and chip PDN modeling.

A question was asked about slide 17, if the result contains the PCB as well. Baolong responded that the result is with the package only.

DESIGNING DDR3 SYSTEM USING STATIC TIMING ANALYSIS IN CONJUNCTION WITH IBIS SIMULATIONS

Taranjit Kukal#, Zhangmin Zhong##, Heiko Dudek### (Cadence Design Systems, #India, ##China, ###Germany)

Zhangmin Zhong described how DDR3 board design requires exploration of a large solution space including timing budgets, signal quality, component selection and stack-up and layout constraints. There are multiple constraints across timing and signal integrity. Timing closure across reads, writes and address is challenging. Signal integrity (SI) also affects timing. Ad-

hoc analysis and verification leads to non-optimal designs. A unified static timing analysis and SI flow produces better designs. SI simulations feedback into the static timing analysis. Zhangmin presented several use cases. Zhangmin concluded that DDR3 compliance requires multiple specifications to be met covering timing and SI measurements. Timing models should be able to handshake data with IBIS simulations at pre-route exploration and post-route verification stages to ensure that both SI and timing constraints are met.

CONCLUDING ITEMS

Lance Wang thanked the co-sponsors, presenters and attendees for their participation and support. The meeting adjourned at 5:30 PM.

NEXT MEETING

The Asian IBIS Summit – Hsinchu will be held November 13, 2012. The Asian IBIS Summit – Yokohama will be held November 16, 2012. The next IBIS Open Forum teleconference will be held November 30, 2012 from 8:00 to 10:00 AM US Pacific Time.

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NOTES

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This meeting was conducted in accordance with the TechAmerica Legal Guides and TechAmerica Manual of Organization and Procedure.

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To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS

clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/
http://www.eda.org/ibis/bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/
http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eda.org/ibis

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

To create an account on the TechAmerica KAVI workspace, check out:

http://workspace.techamerica.org/kwspub/join/

IBIS CURRENT MEMBER VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	September 14, 2012	October 5, 2012	October 26, 2012	November 9, 2012
Agilent Technologies	User	Active	X	X	X	X
Altera	Producer	Inactive	X	-	-	-
ANSYS	User	Inactive	X	-	-	X
Applied Simulation Technology	User	Inactive	-	-	-	-
ARM	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Active	-	X	X	X
Ericsson	Producer	Active	-	-	X	X
Foxconn Technology Group	Producer	Inactive	-	-	-	-
Freescale	Producer	Inactive	-	-	-	-
Huawei Technologies	Producer	Inactive	-	-	-	X
IBM	Producer	Active	X	X	X	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	X	X	X
IO Methodology	User	Active	X	X	X	X
LSI	Producer	Inactive	-	X	-	-
Maxim Integrated Products	Producer	Inactive	X	-	-	-
Mentor Graphics	User	Active	X	X	X	-
Micron Technology	Producer	Active	X	X	X	-
Nokia Siemens Networks	Producer	Inactive	-	-	-	X
QLogic	Producer	Inactive	-	-	-	-
Signal Integrity Software	User	Active	X	X	X	-
Sigrity	User	Inactive	-	-	-	-
Synopsys	User	Inactive	-	-	-	X
Teraspeed Consulting	General Interest	Active	X	X	X	-
Texas Instruments	Producer	Inactive	-	-	-	-
Toshiba	Producer	Inactive	-	-	-	-
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	-	-	X
Zuken	User	Inactive	-	-	-	-

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

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