

New Approach for Implementing IBIS-ISS for Package, Module, Connector, Cable, and External Model

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Overview

- Goals of Presentation
- IBIS-ISS in .ibs files
 - On-Die Model
 - Package A
 - Package B
 - Package C
 - Package D
- IBIS-ISS Interconnect in .ebd file
 - Legacy EBD
 - EBD with ISS subckt
 - What it buys you
 - EBD with Touchstone file
- Electronic Module Description (EMD)
- Buffer SPICE Subckts (IBIS-BSS)
- Motion

Goals of Presentation

- To explain the range of functionality proposed
 - Will require some supporting documentation.
- Syntax in examples is self documenting. Just studying examples:
 - User can understand the capability of the interconnect models delivered.
 - IC Vendor can understand how to create interconnect models.
 - EDA Vendors can understand how to generate simulations using these interconnect models.
- Propose a specific course of action.

IBIS-ISS in .ibs files

- Minimal changes to legacy IBIS
- Support both package and on-die models
- Satisfies needs today and in the future

package.ibs

[Component]

[IBIS-ISS Package] Package_<A:Z>.pkg

[IBIS-ISS On-Die] On-Die.die

[Pin]

Pin_Name	Signal_name	Model
A1	DQ1	DQ
A2	DQ2	DQ
A3	DQ3	DQ
V1	VDD	Power
G1	VSS	GND

[Die_Name]

Die_name	Signal_name
----------	-------------

D.VDD1	VDD
--------	-----

D.VDD2	VDD
--------	-----

D.VSS1	VSS
--------	-----

D.VSS2	VSS
--------	-----

[Model] DQ

A_puref	VDD
---------	-----

A_pdref	VSS
---------	-----

[End]

On-Die.die

```
(On-Die_models
  (DQ_die
    (Tstonefile    die_DQ.s2p)
    (Model_Ports
      (1 (Type Pad)  (Model_Name DQ))
      (2 (Type Buffer) (Model_Name DQ))
    )
  )
  (POWER
    (Tstonefile    die_POWER.s6p)
    (Model_Ports
      (1 (Type Pad) (Pad_Name  D.VDD1))
      (2 (Type Pad) (Pad_Name  D.VDD2))
      (3 (Type Pad) (Pad_Name  D.VSS1))
      (4 (Type Pad) (Pad_Name  D.VSS2))
      (5 (Type Buffer) (Supply VDD))
      (6 (Type Buffer) (Supply VSS))
    )
  )
)
```

Package_A.pkg

```
(Package_Models
  (DQ_pkg
    (File          pkg_DQ.mod)
    (Subckt        (Corner pkg_DQ_typ pkg_DQ_min pkg_DQ_max))
    (Length        (Range 15 11 21))
    (Parameters    Length)
    (Model_Ports
      (1 (Type Pad) (Model_Name DQ))
      (2 (Type Pin) (Model_Name DQ))))
  (POWER
    (Tstonefile    pkg_POWER.s6p)
    (Model_Ports
      (1 (Type Pad) (Pad_Name  D.VDD1))
      (2 (Type Pad) (Pad_Name  D.VDD2))
      (3 (Type Pad) (Pad_Name  D.VSS1))
      (4 (Type Pad) (Pad_Name  D.VSS2))
      (5 (Type Pin) (Pin_Name   V1))
      (6 (Type Pin) (Pin_Name   G1))
    )
  )
)
```

Package_B.pkg

(Package_Models

(DQ_pkg

(File pkg_DQ.mod)

(Subckt (Corner pkg_DQ_typ pkg_DQ_min pkg_DQ_max))

(Pin_Name (List A1 A2 A3))

(Length (Range 15 11 21))

(Parameters Length)

(Dependency_Table

(ParameterNames Pin_Name Length)

(ColumnTypes In Out_Match)

(A1 11)

(A2 15)

(A3 21))

(Model_Ports

(1 (Type Pin) (Pin_Name {Pin_Name}))

(2 (Type Pad) (Pad_Name D.{Pin_Name}))))

(POWER

(Tstonefile pkg_POWER.s6p)

(Model_Ports

(1 (Type Pad) (Pad_Name D.VDD1))

(2 (Type Pad) (Pad_Name D.VDD2))

(3 (Type Pad) (Pad_Name D.VSS1))

(4 (Type Pad) (Pad_Name D.VSS2))

(5 (Type Pin) (Pin_Name V1))

(6 (Type Pin) (Pin_Name G1))))

Package_C.pkg

(Package_Models

(DQ_pkg

(Tstonefile cpl_DQ.s6p)

(Model_Ports

(1 (Type Pin) (Channel 1) (Victim True) (Model_Name DQ))

(2 (Type Pad)(Channel 1) (Victim True) (Model_Name DQ))

(3 (Type Pin) (Channel 2) (Victim False) (Model_Name DQ))

(4 (Type Pad)(Channel 2) (Victim False) (Model_Name DQ))

(5 (Type Pin) (Channel 3) (Victim False) (Model_Name DQ))

(6 (Type Pad)(Channel 3) (Victim False) (Model_Name DQ))))

(POWER

(Tstonefile pkg_POWER.s6p)

(Model_Ports

(1 (Type Pad) (Pad_Name D.VDD1))

(2 (Type Pad) (Pad_Name D.VDD2))

(3 (Type Pad) (Pad_Name D.VSS1))

(4 (Type Pad) (Pad_Name D.VSS2))

(5 (Type Pin) (Pin_Name V1))

(6 (Type Pin) (Pin_Name G1))))

)

Package_D.pkg

```
(Package_Models
  (DQ_pkg
    (Tstonefile cpl_DQ.s6p)
    (Model_Ports
      (1 (Type Pin) (Pin_Name A1))
      (2 (Type Pad) (Pad_Name D.A1))
      (3 (Type Pin) (Pin_Name A2))
      (4 (Type Pad) (Pad_Name D.A2))
      (5 (Type Pin) (Pin_Name A3))
      (6 (Type Pad) (Pad_Name D.A3)) ))
  (POWER
    (Tstonefile pkg_POWER.s6p)
    (Model_Ports
      (1 (Type Pad) (Pad_Name D.VDD1))
      (2 (Type Pad) (Pad_Name D.VDD2))
      (3 (Type Pad) (Pad_Name D.VSS1))
      (4 (Type Pad) (Pad_Name D.VSS2))
      (5 (Type Pin) (Pin_Name V1))
      (6 (Type Pin) (Pin_Name G1)) )))
```

```
(On-Die_models
  (DQ_die
    (Tstonefile die_DQ.s6p)
    (Model_Ports
      (1 (Type Pad) (Pad_Name D.A1))
      (2 (Type Buffer) (Buffer_Name B.A1))
      (3 (Type Pad) (Pad_Name D.A2))
      (4 (Type Buffer) (Buffer_Name B.A2))
      (5 (Type Pad) (Pad_Name D.A3))
      (6 (Type Buffer) (Buffer_Name B.A4)) ))
  (POWER
    (Tstonefile die_POWER.s10p)
    (Model_Ports
      (1 (Type Pad) (Pad_Name D.VDD1))
      (2 (Type Pad) (Pad_Name D.VDD2))
      (3 (Type Pad) (Pad_Name D.VSS1))
      (4 (Type Pad) (Pad_Name D.VSS2))
      (5 (Type Buffer) (Buffer_Name Pu.A1))
      (6 (Type Buffer) (Buffer_Name Pd.A1))
      (7 (Type Buffer) (Buffer_Name Pu.A2))
      (8 (Type Buffer) (Buffer_Name Pd.A2))
      (9 (Type Buffer) (Buffer_Name Pu.A3))
      (10 (Type Buffer) (Buffer_Name Pd.A3)) )))
```

IBIS-ISS Interconnect in .ebd file

- Legacy.ebd example
- [Path Description] can be converted to IBIS-ISS programmatically
- Simulation shows the importance of using lossy transmission lines
- Extensions to EBD to interface to IBIS-ISS essentially the same as used in .ibs files

Legacy EBD

[IBIS Ver] 4.0

[File name] Legacy.ebd

[Begin Board Description]

Example

[Number Of Pins] 12

[Pin List] signal_name

A2 GND

A3 POWER

A4 DQ26

A5 POWER

A6 DQ25

A8 DQ7

A12 GND

C7 DK0#

D7 DK0

F5 A1

F11 POWER

G1 GND

[Reference Designator Map]

| Ref Des File name

Component name

U0 memory.ibs memory

U1 memory.ibs memory

[End Board Description]

[End]

[Path Description] DQ26

Pin A4

Len = 0 C = 0.194p / | solder ball C

Len = 0 L = 0.185n / | solder ball L

Len = 1 R = 1.799 L = 3.720e-09 C = 1.247e-12 / | substrate RLC

Len = 0 C = 0.010p / | bondwire bond pad C

Len = 0 L = 0.226n / | bondwire L

Len = 0 C = 0.060p / | bondwire C

Len = 0 R = 128.7m / | bondwire R

Len = 0 C = 0.010p / | bondwire bond pad C

Len = 5.022 R = 1.666 L = 4.62e-10 C = 1.58e-13 / Go=0, Rs=2.1e-05 Gd=2.1e-13

Fork

Len = 5.022 R = 1.666 L = 4.62e-10 C = 1.58e-13 / Go=0, Rs=2.1e-05 Gd=2.1e-13

Len = 0 C = 0.010p / | pad C

Endfork

Len = 0.451 R = 1.666 L = 4.62e-10 C = 1.58e-13 / Go=0, Rs=2.1e-05 Gd=2.1e-13

Len = 0 C = 0.010p / | pad C

Fork

Len = 0.595 R = 0.926 L = 2.22e-10 C = 3.22e-13 / Go=0, Rs=2.1e-05 Gd=2.1e-13

Len = 0 C = 0.010p / | pad C

Endfork

Node U1.230

[Path Description] DQ25

[Path Description] DQ7

[Path Description] DK0#

[Path Description] DK0

[Path Description] A1

IBIS-ISS EBD

[IBIS Ver] 6.0

[File name] IBIS-ISS.ebd

[IBIS-ISS] EBD_IBIS-ISS.pkg

[Begin Board Description] Example

[Number Of Pins] 12

[Pin List] signal_name

A2 GND

A3 POWER

A4 DQ26

A5 POWER

A6 DQ25

A8 DQ7

A12 GND

C7 DK0#

D7 DK0

F5 A1

F11 POWER

G1 GND

[Reference Designator Map]

Ref Des	File name	Component name
---------	-----------	----------------

U0	memory.ibs	memory
----	------------	--------

U1	memory.ibs	memory
----	------------	--------

[End Board Description]

[End]

EBD_IBIS-ISS.mod

```
.subckt DQ26 J.A4 U1.230
C1 J.A4 0 194f
L2 J.A4 len1 185p
W3 len1 0 tee4 0 rlgcmodel=wline_1 N=1 L=+9.61E-03
C4 tee4 0 10f
L5 tee4 len2 226p
C6 len2 0 60f
R7 len2 len3 .129
C8 len3 0 10f
W9 len3 0 len4 0 rlgcmodel=wline_2 N=1 L=+5.02E-03
W10 len4 0 len5 0 rlgcmodel=wline_2 N=1 L=+5.02E-03
C11 len5 0 10f
W12 len4 0 len6 0 rlgcmodel=wline_3 N=1 L=+4.5E-04
C13 len6 0 10f
W14 len6 0 U1.230 0 rlgcmodel=wline_14 N=1
L=+5.95122E-04
C15 U1.230 0 10f
.model wline_1 W ModelType=RLGC N=1
+ Lo = +3.86929E-07
+ Co = +1.29791E-10
+ Rs=2.1e-05 Gd=2.1e-13 Ro = +1.87E+02
```

```
.model wline_2 W ModelType=RLGC N=1
+ Lo = +4.62193E-07
+ Co = +1.57917E-10
+ Rs=2.1e-05 Gd=2.1e-13 Ro = +1.66E+03
.model wline_3 W ModelType=RLGC N=1
+ Lo = +4.62193E-07
+ Co = +1.57917E-10
+ Rs=2.1e-05 Gd=2.1e-13 Ro = +1.66E+03
.model wline_14 W ModelType=RLGC N=1
+ Lo = +2.22411E-07
+ Co = +3.21547E-10
+ Rs=2.1e-05 Gd=2.1e-13 Ro = +9.24E+02
.ends DQ26
```

```
.subckt DQ25 J.A6 U1.228
.ends DQ25
.subckt DQ7 J.A8 U0.228
.ends DQ7
.subckt DK0# J.C7 U1.22
.ends DK0#
.subckt DK0 J.D7 U1.24
.ends DK0
.subckt A1 J.A1 U1.55
.ends A1
```

Loss is Important

Blue: Legacy EBD

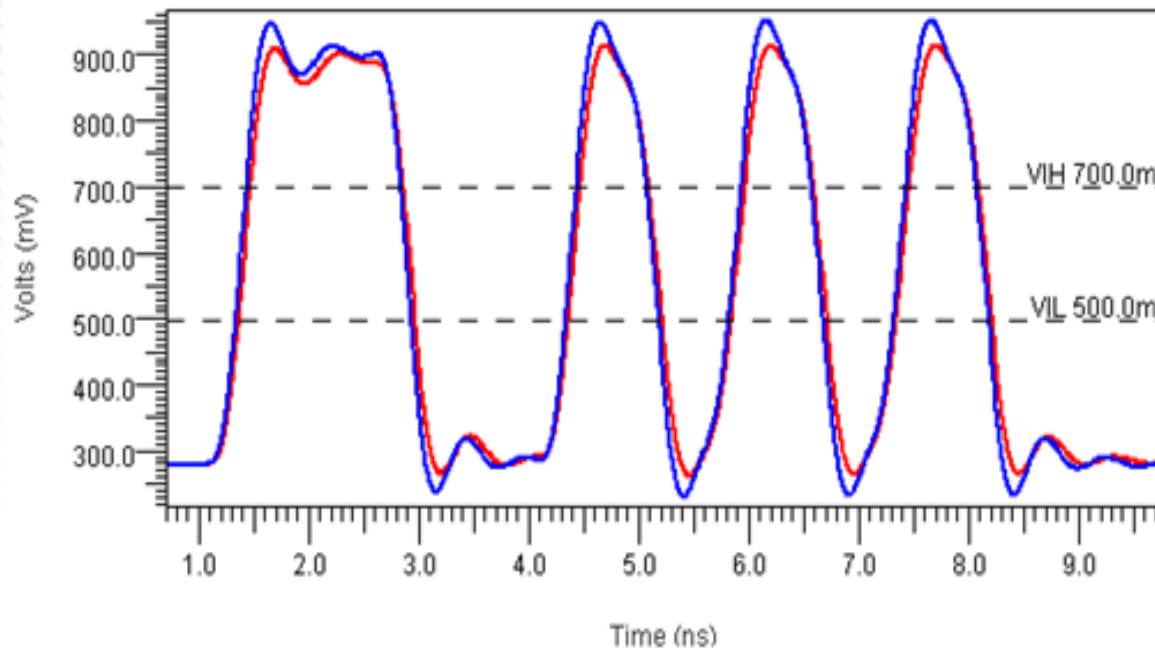
Red: Gd and Rs included

1 GBps .5dB ~ 5%

28 GBps 3dB ~ 40%

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EBD Hspice Subckts



EBD_IBIS-ISS.pkg using Touchstone files

```
(DQ26
  (Tstonefile DQ26.s2p)
  (Model_Ports
    (1 (Pin_Name A4))
    (2 (Pin_Name U1.230)) ))
(DK0
  (Tstonefile DK0.s6p)
  (Model_Ports
    (1 (Pin_Name C7))
    (2 (Pin_Name U0.22))
    (3 (Pin_Name U1.22))
    (4 (Pin_Name D7))
    (5 (Pin_Name U0.24))
    (6 (Pin_Name U1.24)) ))
(DQ25_Coupled
  (Tstonefile DQ25_Coupled.s6p)
  (Model_Ports
    (1 (Pin_Name A4)      (Channel 1) (Victim False))
    (2 (Pin_Name U1.230) (Channel 1) (Victim False))
    (3 (Pin_Name A6)      (Channel 2) (Victim True))
    (4 (Pin_Name U1.228) (Channel 2) (Victim True))
    (5 (Pin_Name A8)      (Channel 3) (Victim False))
    (6 (Pin_Name U0.228) (Channel 3) (Victim False)) ))
```


Electronic Module Description (EMD)

- Modifying EBD is not the right thing to do
- We should plan on a new EMD section in IBIS 6.0
- This is nothing new. I gave presentation in 2008 to IBIS-ATM, which was the driving force behind IBIS-ISS
 - http://www.eda.org/ibis/macromodel_wip/archive/20080624/walterkatz/Electrical%20Module%20Description%20EMD%20Review/EMD_Review_080624.pdf
 - http://www.eda.org/ibis/macromodel_wip/archive/20080916/walterkatz/Block%20Diagram%20View%20of%20EMD/EMD_Block.pdf
- EMD examples
 - Legacy.ebd file shown in slides 10 and 11 converted to EMD
 - Connector in EMD
- EMD supersedes EBD and ICM, with the added functionality of supporting MCM, Connectors and Cables

Legacy EBD converted to EMD

(My_EMD (IBIS_Ver 6.0) (Description "...")

(File_Rev "...") (Copyright "...") (Notes "...") (Date "...") (Disclaimer "...") (Manufacturer "...")

(File_Name My_EMD.emd)

(IBIS-ISS_File My_EMD.iss))

(Module_Name Example)

(Number_Of_Pins 12)

(Pin List

(A2 (Signal_Name GND))

(A3 (Signal_Name POWER))

(A4 (Signal_Name DQ26))

(A5 (Signal_Name POWER))

(A6 (Signal_Name DQ25))

(A8 (Signal_Name DQ7))

(A12 (Signal_Name GND))

(C7 (Signal_Name DK0#))

(D7 (Signal_Name DK0))

(F5 (Signal_Name A1))

(F11 (Signal_Name POWER))

(G1 (Signal_Name GND)))

(Diff_Pins (D7 C7))

(Extended_Nets

(DQ26 A4 U1.230) (DQ25 A6 U1.228) (DQ7 A8 U0.228) (DK0 C7 D7 U1.22 U1.24) (A1 A1 U1.55)

(POWER A3 A5 F11 U0.41 U0.125 U1.41 U1.125) (GND A2 A12 G1 U0.10 U0.235 U1.10 U1.235))

(Reference_Designator_Map

(U0 (IBIS_File memory.ibs) (Component memory))

(U1 (IBIS_File memory.ibs) (Component memory)))

Connector EMD

(Connector (IBIS_Ver 6.0)

(File_Name Connector.emd)

(IBIS-ISS_File Connector.iss))

(Module_Name Connector)

(Number_Of_Pins 12)

(Connectors

(A (Side Aside))

(B (Side Bside)))

(Extended_Nets

(1 A.1 B.1)

(2 A.4 B.4)

(POWER A.2 A.5 B.2 B.5)

(GND A.3 A.6 B.3 B.6))

(Pin List

(A.1 (Signal_Name 1))

(A.2 (Signal_Name POWER))

(A.3 (Signal_Name GND))

(A.4 (Signal_Name 2))

(A.5 (Signal_Name POWER))

(A.6 (Signal_Name GND))

(B.1 (Signal_Name 1))

(B.2 (Signal_Name POWER))

(B.3 (Signal_Name GND))

(B.4 (Signal_Name 2))

(B.5 (Signal_Name POWER))

(B.6 (Signal_Name GND))))

File Connector.iss

(Package_full

(Tstonefile Package_full.s12p)

(Model_Ports

(1 (Pin_Name A.1)) (7 (Pin_Name B.1))

(2 (Pin_Name A.2)) (8 (Pin_Name B.2))

(3 (Pin_Name A.3)) (9 (Pin_Name B.3))

(4 (Pin_Name A.4)) (10 (Pin_Name B.4))

(5 (Pin_Name A.5)) (11 (Pin_Name B.5))

(6 (Pin_Name A.6)) (12 (Pin_Name B.6))))

(Package_coupled_A

(Tstonefile Package_coupled_A.s4p)

(Model_Ports

(1 (Pin_Name A.1)) (3 (Pin_Name B.1))

(2 (Pin_Name A.4)) (4 (Pin_Name B.4))))

(Package_coupled_B

(Tstonefile Package_full.s12p)

(Model_Ports

(1 (Pin_Name A.1)) (7 (Pin_Name B.1))

(4 (Pin_Name A.4)) (12 (Pin_Name B.4))))

Buffer SPICE Subckts (IBIS-BSS)

- BIRDS 116, 117, 118, 122, 125, 129, 144, 145, 152 and 153 are gobbledygook to address the simple problem of defining SPICE subckts for [Model]s
- <http://en.wikipedia.org/wiki/Gobbledygook>
 - **Gobbledygook** or **gobbledegook** (sometimes **gobbledegoo**) is [jargon](#) or especially convoluted language (specifically, American English and British English) that results in it being excessively hard to understand or even [incomprehensible](#). "Bureaucratese" is one form of gobbledygook. There are two distinct and opposite cases. One is that incomprehensible material is actual [gibberish](#). In the other some abstruse material is either ineptly presented or is subjectively perceived to be gibberish due to a lack of preparation. The SMOG statistic for gobbledygook for example yields an index in terms of years of required education.
- Creating a new IBIS 6.0 section IBIS-BSS dedicated to defining SPICE subckts for [Model]s is a much simpler solution as demonstrated in the next slide.
 - No need for A_to_D or D_to_A
 - No need for [Circuit Call]
 - No need for [Node Declarations]
 - No need for [External Circuit]
- IBIS-BSS is IBIS-ISS enhanced to include “macros”
 - e.g. PWL voltage controlled sources
 - Enhancements not required for AMI analog models (AMI is LTI)
 - Enhancements required to represent non-LTI buffer models

IBIS-BSS Exemplars

[Model] IO

Model_type I/O

Vinl .6

Vinh .8

Vmeas .7

[Temperature Range] 25 100 0

[Voltage Range] 1.5 1.4 1.6

(IBIS-BSS

(IO

(File_Name IO.spi)

(Circuit_Name (Corner io_typ io_min io_max))

(Stimulus

(Trise (Corner 50ps 70ps 40ps))

(Tfall (Corner 50ps 70ps 40ps))

(Vlow 0)

(Vhigh (Corner 1.5 1.4 1.6))

(Enable 0 1.5)) | (Drive Enabled Disabled)

(Parameters

(Zon (Corner 50 60 40))

(Zoff 1K)

(C_comp (Corner 1pF 1.5pF .8pF))

(Model_Ports

(1 Drive) | Analog stimulus input to driver

(2 Signal) | Pad of buffer

(3 Core) | Analog output of receiver

(4 Enable)) | Analog Enable

[Model] tx

Model_type Differential_Output

Vmeas .7

[Algorithmic Model]

Executable Windows_VS5_32 tx.dll Tx.ami

[End Algorithmic Model]

[Temperature Range] 25 100 0

[Voltage Range] 1.5 1.4 1.6

(IBIS-BSS

(tx

(Tstonefile Tx.ami(Tstonefile))

(Stimulus

(Trise 1ps) (Tfall 1ps)

(Vlow Tx.ami(Vol))

(Vhigh Tx.ami(VoH))

(Rdrive Tx.ami(Rdrive)) | R between stimuli

| (ideal voltage sources) and s4p inputs

(Model_Ports

(1 Drive+) | Analog stimulus input high side

(2 Drive-) | Analog stimulus input low side

(3 Signal+) | Analog output high side

(4 Signal-)) | Analog output low side

Items in red are reserved branches/parameters

BIRDS 116, 117, 118, 122, 125, 129, 144, 145, 152 and 153

BIRD No.	BIRD Name
116	Add IBIS-ISS to [External Model] and [External Circuit] as a Supported Language
117.3	Parameterize A_to_D and D_to_A Converters
118.2	Analog Parameter Assignments
122	IBIS-AMI New Reserved Parameters for Analog Modeling
125.1	Make IBIS-ISS Available for IBIS Package Modeling
129	Add "polarity" Argument to D_to_A Converters
144.3	Add TOUCHSTONE to [External Model] and [External Circuit] as a Supported Language
145.2	Instantiation of IBIS I/O buffers in an [External Circuit] using the [Model Call] keyword
152	Analog Model Boundary Definition
153	Parameter Tree Keyword

Motion

Resolve, that that we

- Anticipate rejecting BIRDs 116, 117, 118, 122, 125, 129, 144, 145, 152 and 153.
- Generate BIRDs to be included in IBIS 6.0 to support IBIS-ISS subckts and Touchstone files for package and on-die interconnect modeling as described in this document.
- Generate BIRDs to be included in IBIS 6.0 to support IBIS-BSS subckts and Touchstone files for buffer models as described in this document.
- Create a new section in IBIS 6.0 called Electronic Module Design (EMD) to support Boards, MCM, Packages, Connectors and Cables and to support IBIS-ISS subckts and Touchstone files for interconnect as described in this document.
- IBIS 6.0 Editorial Committee consider putting the following IBIS 6.0 sections in separate documents
 - AMI, IBIS-BSS, IBIS-ISS Package Modeling, EMD
 - EMI Parameters, Test Load and Data Description, Notes on Data Derivation Method
 - EBD, Legacy Package Modeling, Pin Mapping, Multi-Lingual Model Extensions, Node Declarations, Circuit Call, External Circuit, External Model