IBIS Open Forum Minutes

Meeting Date: June 5, 2012
Meeting Location: DAC IBIS Summit, San Francisco, California

VOTING MEMBERS AND 2012 PARTICIPANTS

Agilent	Heidi Barnes*, Radek Biernacki*, Yoji Sekine, Fangyi Rao
Altera	David Banas*, Hsinho Wu, Masashi Shimanouchi
ANSYS (Ansoft)	Flavio Calvano, Luis Armenta*, Dan Dvorscak*
Applied Simulation Technology	Norio Matsui
ARM	(Nirav Patel)
Cadence Design Systems	Brad Griffin*, Terry Jernberg, Jilin Tan, Dennis Nagle Ambrish Varma
Ericsson	Anders Ekholm, Zilwan Mahmod, Mattias Lundquist
Foxconn Technology Group	(Sogo Hsu)
Freescale	(Jon Burnett)
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Michael Mirmak*, Subas Bastola*, Udy Shrivastava, Stewart Gilbert, Eddie Frie
IO Methodology	Lance Wang
LSI	Brian Burdick
Maxim Integrated Products	Hassan Rafat, Mahbubul Bari
Mentor Graphics	Arpad Muranyi*, Vladimir Dmitriev-Zdorov
Micron Technology	Randy Wolff, Aniello Viscardi, Francesco Madonna Antonio Prisco, Justin Butterfield*
Nokia Siemens Networks GmbH	Eckhard Lenski, Evis Minga
Signal Integrity Software	Walter Katz*, Mike LaBonte, Todd Westerhoff Akalu Lentiro
Sigrity	Raymond Chen, Yingxin Sun, Sam Chitwood Ben Franklin, Srdjen Djordjevic
Synopsys	Andy Tai, Scott Wedge, Hany Elhak, Ted Mido
Teraspeed Consulting Group	Bob Ross, Tom Dagostino
Toshiba	Masatoshi Abe*
Xilinx	Harry Fu
Zuken	Michael Schaeder

OTHER PARTICIPANTS IN 2012

AMD	(Nam Nguyen)
Apple Computer	(Matt Herndon)
Aruba Networks	Amir Motamedi
Avago Technologies	Sanjeev Gupta, Amolak Badesha
Bayside Design	Elliot Nahas
Cavium	Johann Nittmann
Ciena	Kaisheng (Klaus) Hu*

Cisco Systems	David Siadat, Mike Sapozhnikev
Enterasys	Robert Haller
Exar Corporation	Helen Nguyen
Granite River Labs	Jiang Xu, Johnson Tan
Hewlett-Packard	Ting Zhu*
High Speed Design Center	Ben Chia
Hitachi	Yutaka Uematsu
Huawei Technologies	Xiaoqing Dong
IBM	Adge Hawes, Greg Edlund
Instituto de Telecomunicações	Wael Dghais, Hugo Teixeira
JEITA	Atsushi Ishikawa*
KEI Systems	Shinichi Maeda
Luxshare-ICT	Alan Kinningham, Steven Wong
MK Resolutions	Olga Chervyakova
Nvidia	Eric Hsu
Politecnico di Torino	Stefano Grivet-Talocia
QLogic	(James Zhou)
Research In Motion	Yi Cao
Sony	Kenji Yasoda
ST Microelectronics	Davide Pandini
TechAmerica	(Chris Denham)
Texas Instruments	Casey Morrison, Pegah Alavi*, Valerie Chang Modesto Garcia, Karl Muth
Université de Brest	Mihai Telescu, Cherif Diouf
University of Illinois	Thomas Comberiate, José Schutt-Ainé
Vitesse Semiconductor	Sirius Tsang
ZTE	(Huang Min)

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
June 22, 2012	205 722 546	IBIS

For teleconference dial-in information, use the password at the following website:

   https://cisco.webex.com/cisco/j.php?J=205722546

All teleconference meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed

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> http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The IBIS Open Forum Summit at DAC was held in San Francisco, California at the Marriott Marquis Hotel. About 16 people representing 13 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

> http://www.eda.org/ibis/summits/jun12/

Michael Mirmak welcomed all the participants and thanked the co-sponsors Mentor Graphics and the IBIS Open Forum. He asked all the participants to introduce themselves.

Walter Katz requested adding an open discussion item: brainstorming on what IBIS is and what models are. IBIS would be treated as a container for models, with different languages for the data in the container. Packages, power delivery networks and device data have outgrown the IBIS structure. The topic was scheduled for open discussion after the formal presentations concluded.

IBIS IN REVIEW

Michael Mirmak, Intel Corp.

Michael Mirmak summarized the status of IBIS, as an organization, in terms of achievements and the goals for the coming months. He noted the BIRD progress since the DesignCon summit, and graded the "predictions" made during that summit for progress expected by mid-2012. The key upcoming challenges to IBIS as an organization include finding a new structure for the IBIS Model Review Committee, addressing TechAmerica organizational changes and moving to a faster, more regular schedule of specification updates. He also added that some charter changes would be necessary if the DAC meeting in 2013 were not used as an IBIS Summit location, due to its Texas venue.

Walter Katz suggested that the Model Review Committee be disbanded. Arpad Muranyi noted that individuals could still volunteer to be reviewers, with their availability posted to the IBIS website. Any NDAs that might be needed could be left to the discretion of submitters and individual reviewers to discuss.

Dan Dvorscak asked whether parser updates would follow a six-month update schedule. Arpad noted that a six-month update schedule would result in a significant change in arrangements for parser licensing and payment.

Walter asked whether an IBIS-ISS parser is truly needed, aside from financial impacts, if most EDA vendors have compatible formats. Michael Mirmak suggested that a standard parser would still be useful as a universal reference for the industry. Arpad added that IBIS-ISS has some definitions and interpretations that are different than those used in Berkeley SPICE and commercial SPICE flavors.

IBIS-ATM TASK GROUP REPORT
Arpad Muranyi, Mentor Graphics Corp.

Arpad Muranyi provided a very brief summary of ongoing work in the IBIS-ATM (Advanced Technology Modeling) Task Group. BIRD149.1 and BIRD151 have been included in IBIS 5.1. BIRD124 has been rejected in favor of BIRD150. It and BIRD152 and BIRD123.3 are targeted for IBIS 6.0, assuming IBIS 5.2 is intended only for standardization. Several important areas still require discussion and finalization of related BIRDs, including links to package models, improvements to analog and digital connections, plus new features such as backchannel equalization and repeater treatments.

David Banas asked about Arpad's thoughts on the rate of progress and the group's efficiency. Arpad answered that the group is moving very slowly, with decisions rehashed multiple times. "Ratholes" or minor topics sometimes dominate the discussion. Arpad also noted that others are welcome to stand as chair.

Radek Biernacki asked how Arpad felt about the pace relative to a six-month release schedule. Arpad answered that this is not just an ATM Task Group issue. Radek added that rushing can also cause issues.

Walter Katz noted that IBIS is a triangle, involving EDA vendors, IC vendors and system designers. If discussion is dominated by one group – EDA vendors, in some cases – progress becomes bogged down. IC vendors and system designers can drive issue closure and increased speed. Arpad suggested more active discussions between meetings, as waiting for the next meeting slows progress.

IBIS 5.1: AN OVERVIEW
Michael Mirmak, Intel Corp.

Michael Mirmak summarized the status of IBIS 5.1 as a document. 25 BIRDs have been included in IBIS 5.1, mostly covering clarifications to IBIS-AMI. The document also implements a completely new format of the entire document and some restructuring of the IBIS-AMI sections. The use of a non-ASCII format and editor allows tables and figures to be more complex but also makes the entire document readable. The document is expected to be released from the IBIS Editorial Task Group in time for introduction at the June 22 IBIS Open Forum teleconference. Challenges for continuing work include developing a new flow for submitting BIRDs, including potentially a template and updated tracking system (likely MANTIS). Michael concluded with a call to action for the attendees to review the document and provide feedback.

IBIS QUALITY CONTROL THROUGH SCRIPTING
Justin Butterfield, Micron Technology

Justin Butterfield summarized Micron's approach to generating traditional IBIS files through scripts. A basic template is used, which scripts combine with tables of data particular to individual devices. Mapping is used to combine the table data with IBIS keywords and individual features. The approach is also used for package model information and EBD modeling of stacked die devices. The entire flow is less prone to errors than traditional copy/paste methods, and permits generation of useful output reports.

Originally, the approach was change, copy and paste. Justin added that the scripts were created to prevent losing the connection between models and device parameters. The script builds IBIS files with a single [Model] in each. Lumped package models are used, as the packages themselves are short, making simple pin values still valid.

EBD structures are used for the packages (rather than DIMMs) on stacked-die designs. Michael Mirmak asked whether loss modeling was ever needed. Justin confirmed that, for DDR3, some W-elements are used in place of lumped parameters.

Arpad Muranyi asked whether [Model Selector] was used to combine models in final files. Justin confirmed this was true. Walter Katz clarified that "user" in many of the slides refers to a script user, not a model user.

Arpad asked whether the IBIS-ISS enhancements to IBIS as proposed in recent BIRDs would be useful for these applications. Justin replied that Micron was investigating this.

Subas Bastola asked whether I-V and V-t tables were contained in the spreadsheets used as input. Justin confirmed that they were. Michael asked whether IBIS could be modified to use dependency tables for basic or traditional parameters, as has been proposed for IBIS-AMI; would that make modeling easier? Arpad added that BIRD116 and BIRD117 already cover this approach. Walter noted that his presentation would cover this for IBIS "7.0" (after IBIS 5.2/6.0).

ELECTION OF OFFICERS

Michael Mirmak explained the nature of each of the IBIS board positions and asked for nominations for each. He added that the current serving officers would be willing to continue to serve if no other nominations were made.

Arpad Muranyi asked about elections for Task Groups. Walter Katz suggested that making procedures too fixed might derail technical development efforts.

Without objection or other nominees being proposed, the nominees below were elected to serve as the IBIS Board for 2012-2013.

Chair: Michael Mirmak, Intel Corp.
Vice-Chair: Lance Wang, IO Methodology Inc.

Secretary: Randy Wolff, Micron Technology
Model Librarian: Anders Ekholm, Ericsson
Postmaster: Mike LaBonte, Signal Integrity Software (SiSoft)
Webmaster: Mike LaBonte, Signal Integrity Software (SiSoft)

ADVENTURES IN HASKELL AMI MODELING – PART DEUX

David Banas, Altera

David Banas summarized the continuing work at Altera to use Haskell for IBIS-AMI modeling. Previous work showed that, for AMI_Init, Haskell can perform better than C for equivalent buffer descriptions, even with shorter code. AMI_GetWave work demonstrated that excellent correlation could be obtained with 20 lines of Haskell code, but at the penalty of 27x slower execution than C.

Pure impulse responses and frequency response curves were used for correlation. Haskell AMI_Init and AMI_GetWave match, with 40 gigasamples per second, with the same CSV file used as input. Walter Katz noted that the mismatches may be due to sampling.

The receiver design involves CTLE data and a non-linear compressor function, but testers were careful not to stimulate compressor. Further, the "spurs" evident in the correlation are understood as the result of coding errors and have been corrected. The "tail" difference in frequency domain correlation is "standard aliasing" and not disturbing, but the 27x worse performance than C is a disappointment. Using the optimize flag for the Haskell compiler reduced this to 10x. The list on slide 10 shows the top five "cost centers" or code segments and associated runtime burden. The second list contains the child processes associated with the cost centers. Cost centers can even be set at each line of code.

Michael Mirmak asked whether the optimize flag might be corrupting the correlation while improving runtime. David noted that this was under investigation.

Brad Griffin asked whether one can write routines in Haskell and link to C. David answered that translation and linking was possible in both directions. A Haskell convolution call was being used in the function which may be a source of slowdowns.

Walter Katz asked whether the compiler could be affecting the sampling. Additionally, David was asked why Haskell was being used instead of C, with its succinct libraries. David noted that using C++ with the "Boost" library suite was investigated as promising, as is C++ version 11. Overall, current C-based approaches are somewhat clunky and not as succinct or as elegant as the Haskell equivalents.

SURROGATE MODEL-BASED HIGH-SPEED IO MACROMODEL

Ting Zhu, Hewlett-Packard
Paul D. Franzon and Michael B. Steer, North Carolina State University

Ting Zhu provided a summary of recent work at NCSU on surrogate modeling. Surrogate modeling uses macromodeling approaches for individual parts of the traditional IBIS model

structure, with sampling used to capture behavioral trends with limited points.

Traditional IBIS is "unsuitable for statistical analysis" and "unable to simulate continuous variations" for distribution-based simulations, limitations that surrogate modeling addresses.

Each IBIS sub-element is modeled using surrogate methods to obtain numerical expressions. Surrogate methods include meta-models and response surface models (where polynomial equations can be used). Individual segments of the model may use different parameters and equation fits to the data. Correlation to transistor-level models is excellent.

The key is to limit samples, but also one needs to make the model data portable to today's simulators. Rational functions and polynomial functions are usable, with Verilog-A used to encapsulate the equations. The actual equation data was obtained using the SUMO package from the University of Ghent.

Surrogate models are similar to best-point fits. The specific modeling approach used also included Vth (shown as "P"). Arpad Muranyi asked whether frequency was included for C_comp. Ting noted that this was not included in this example set, but doing so is not difficult.

Timing error was significantly reduced with surrogate methods. IBIS-AMI representations are still being investigated at NCSU.

SHOULD IBIS SUPPORT EYE MASK DEFINITIONS?
Arpad Muranyi, Mentor Graphics

Arpad Muranyi summarized some key questions on the eye mask parameters needed in industry and available under IBIS 5.1 as proposed. While industry defines eye masks well, IBIS doesn't contain any timing information. IBIS-AMI defines receiver sensitivity, but only in terms of voltage. He observed that the center line in a receiver eye is the sampling time, with clock_times reported with respect to that decision point. No timing information or window is defined in IBIS, however. Arpad noted that in legacy IBIS there was no clock input for any of the receiver model types, so setup and hold was not needed for controlling their output state ('1', '0' or 'X'). But setup and hold parameters might still be useful even with legacy receiver models to tell the EDA tool how to evaluate the waveforms. Walter Katz noted that traditional IBIS indicates the first time that the signal is valid (versus the Vinh and Vinl levels). There's no UI or bit_time in traditional IBIS, and no hold time capability.

Arpad responded that the golden sampling time is versus clocks, not the waveform (the clock doesn't jitter but the data does). David Banas added that there is no Tco concept in traditional IBIS; it analyzes trace delays only and that Vmeas normalizes timings versus Tco loading. Walter added that traditional IBIS also does not include setup or hold concepts.

Walter and David both raised BER analysis as an example of where difficulties emerge from eye masks. Walter noted that specification-compliant designs may be analyzed using different BER data rates. David suggested that analysis is performed at or after the decision point and the evaluation criteria are tied to the design, not standards. Measurements at the pin or pad provide an envelope for individual devices to be evaluated versus specifications.

Michael Mirmak suggested providing a new set of keywords for the timing block or budget of a device. Walter replied that a full IBIS timing model must be developed and added.

PARAMETER TREES
Walter Katz, Signal Integrity Software (SiSoft)

Walter Katz summarized how parameter trees are used in industry and IBIS 5.0. Trees are defined in terms of roots, branches and leaves in IBIS, with nodes being part of industry definitions but not defined in IBIS. A root is a node without a parent, while a leaf is a node without a child. In 5.0, the "branch" is really a node. Traditional IBIS could be redefined in terms of parameter trees similarly to how IBIS-AMI parameters are structured. Walter also noted that tables and equations could be defined and used simultaneously in such a format.

Michael Mirmak observed that, in IBIS 5.1, branches are not named, while nodes and leaves are, which is confusing to casual users and readers. Further, there is an apparent parallel between SPICE netlists and parameter trees as defined. Walter corrected this, stating that SPICE netlists are not actually parameter trees but actually graphs. Radek Biernacki agreed with this approach.

Arpad Muranyi asked whether fixed parameter names and interpretations aren't the fundamental problem. Radek noted that branches can be identified by the "(" character. Subas Bastola inquired whether XML could be used for trees. Arpad noted that several previous attempts have been made to specify different IBIS parameters in terms of XML. Walter added that the specific format isn't as important as the structure.

OPEN DISCUSSION: IBIS 6.0
Michael Mirmak opened the floor for questions and discussion, beginning with IBIS 6.0. Arpad Muranyi suggested that while date codes might be useful for IBIS versioning, the question of parser licensing will have to be reviewed. Up to now, small "dot" revisions" were free, and major changes were for charge. Discussion should include how parser development is financed and how parser licensing is priced.

Radek Biernacki noted that the financial issues should be treated separately from the numbering scheme of IBIS. Maintenance fees in three annual installments might be a useful option.

Walter Katz stated that the numbering of the standard is not an immediate concern; IBIS 5.1 is only a reformat of the document. Instead, he suggested that older material be deprecated, and the document itself be split into separate documents to cover models, packages, EBD formats, AMI programming and the like, with independent revision control. Third, new modeling and package solutions can be developed and implemented.

Radek responded that standardizing sections could be difficult. One document can cover all options. Arpad added that the end of an individual model is not defined. The keyword-driven style of IBIS may still be a barrier; industry needs a new way of tackling modeling problems,

including inventing a language to describe any kind of behavior.

Walter responded that partitioning the document into sections and using a [Model] section for traditional IBIS could be maintained. Arpad added that this would require new parameter syntax.

Radek noted that we like to complain, but that IBIS is a near-hierarchical structure. We can put an equation within the existing structure and facilitate improvements, even with new keywords. Walter noted that BSS (buffer subcircuit specification) could be a solution. Michael noted that the ongoing problem appears to be freedom and flexibility versus reduced model development burdens; having keywords with interpretations recognized in common by industry allows model developers to avoid extra effort in writing evaluation code. Arpad suggested that libraries might be a suitable answer.

OPEN DISCUSSION: WHAT IS THE PURPOSE OF IBIS?

Walter Katz suggested that the purpose of IBIS is to set standards for models that are EDA tool-neutral and protect IP with sufficient accuracy to allow users to make engineering decisions. He outlined a few key areas for discussion:

Scope:
1. I/O buffers: interact with channel, DSP, power
2. On-die power and interconnect
3. Package power and interconnect
4. Socket
5. Board
6. Discretes
7. Connector
8. Optical cables

Languages:
- IBIS IV/VT/Ramp
- Berkeley SPICE
- IBIS-ISS
  VHDL[AMS]
- Verilog[AMS]
- Macromodel
- Equation-based

Issues:
- (MCP) Die pads vs. package pins: 1:1 assumption is not true
- Connector models
- Hierarchy: silicon, stacked silicon, EMD

Heidi Barnes noted that the real question for IBIS is where to define the reference plane that makes sense for defining the model. Package pins are not the ideal location. We would like the physical topology to be symmetrical. Smaller physical structures are better, as the fields will spread out otherwise.

David Banas suggested that the reference plane would be a trace in the middle of a topology, between and far away from vias.

Arpad Muranyi suggested that the biggest problems are due to pending BIRDs: we are more than six months out in terms of work. Walter suggested focusing on fundamentals, including die-to-pad connections. He suggested adding a "silicon only" model option, or similar keyword to identify individual pads. This would represent silicon, while EBD and EMD would describe packages, but no other changes would be made. Arpad responded that [Node Declarations] does part of this, and package definitions do part of this as well. Walter stated that pins, pads, nodes and packages are all separate concepts.

Dan Dvorscak asked whether IBIS was abandoning backwards compatibility in 5.1. Radek Biernacki replied that backwards compatibility in IBIS was "sort of extreme". Version 3.1 models should still be compatible if checked versus 3.1 rules, but a guarantee of forward compatibility with 4.0, etc. should not be made. Subas Bastola asked whether compatibility means 100% support of all keywords. Michael Mirmak responded that was not the assumption, citing transit time. Arpad reiterated that the keyword-driven approach of IBIS is a key problem. Walter added that, to change anything, model-maker support is critical. Power distribution is an example, where there's no buy-in for equation-based models.

Arpad noted that fixes to IBIS would not have to consist of a full language. Walter added that BSS supporting PWLs could get around non-LTI issues. An ISS-like language would be welcome.

Radek noted that IP protection is still critical. Arpad asked what would be the ideal behavioral modeling language for IC vendors to represent their SPICE models. Walter observed that encrypted models are still used, even when using behavioral data.

The June 22nd meeting will include discussion and brainstorming about creating a new Futures group to address IBIS simplification, including die pad, package and pin linking.

Ting Zhu asked about S2IBIS3 – is it up to date? She added that most users are familiar with the traditional IBIS format, but new features are not as familiar. Can the IBIS committee help with understanding these features with better, more complete cases? A new cookbook would be a good way of addressing the issue.

Walter asked how many companies create SerDes silicon to which IBIS-AMI can be applied.

CONCLUDING ITEMS

Michael Mirmak closed the meeting by thanking co-sponsor Mentor Graphics and the presenters. He also thanked all the attendees for making the meeting a success. He noted the time and date of the next IBIS meeting. The meeting concluded at approximately 5:00 PM.

NEXT MEETING

The next IBIS Open Forum teleconference will be held June 22, 2012 from 8:00 to 10:00 AM US Pacific Standard Time.

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NOTES

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This meeting was conducted in accordance with the GEIA Legal Guides and GEIA Manual of Organization and Procedure.

The following e-mail addresses are used:

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>   In the body, for the IBIS Open Forum Reflector:
>   subscribe ibis <your e-mail address>

>   In the body, for the IBIS Users' Group Reflector:
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ibis-info@eda.org
>   To obtain general information about IBIS, to ask specific questions for individual
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ibis@eda.org
>   To send a message to the general IBIS Open Forum Reflector. This is used mostly for
>   IBIS Standardization business and future IBIS technical enhancements. Job posting
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ibis-users@eda.org
>   To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS
>   clarification, current modeling issues, and general user concerns. Job posting
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ibis-bug@eda.org
>   To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form
>   for ibischk resides along with reported BUGs at:

>   http://www.eda.org/ibis/bugs/ibischk/
>   http://www.eda.org/ibis/bugs/ibischk/bugform.txt

>   The BUG Report Form for tschk2 resides along with reported BUGs at:

>   http://www.eda.org/ibis/tschk_bugs/
>   http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

> To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:
>
> http://www.eda.org/ibis/icm_bugs/
> http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

> http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
> http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt
> http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

> http://www.eda.org/ibis

Check the IBIS file directory on eda.org for more information on previous discussions and results:

> http://www.eda.org/ibis/directory.html

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IBIS CURRENT MEMBER VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	May 11, 2012	May 16, 2012	June 1, 2012	June 5, 2012
Agilent Technologies	User	Active	X	-	X	X
Altera	Producer	Inactive	X	-	-	X
ANSYS	User	Active	-	X	X	X
Applied Simulation Technology	User	Inactive	-	-	-	-
ARM	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Inactive	-	-	-	X
Ericsson	Producer	Active	X	-	X	-
Foxconn Technology Group	Producer	Inactive	-	-	-	-
Freescale	Producer	Inactive	-	-	-	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	-	X	X
IO Methodology	User	Active	X	X	X	-
LSI	Producer	Inactive	-	-	X	-
Maxim Integrated Products	Producer	Inactive	-	-	-	-
Mentor Graphics	User	Active	X	-	X	X
Micron Technology	Producer	Active	X	X	X	X
Nokia Siemens Networks	Producer	Active	-	X	X	-
Signal Integrity Software	User	Active	X	-	X	X
Sigrity	User	Active	-	X	X	-
Synopsys	User	Inactive	-	-	-	-
Teraspeed Consulting	General Interest	Inactive	X	-	-	-
Toshiba	Producer	Inactive	-	-	-	X
Xilinx	Producer	Inactive	-	-	-	-
Zuken	User	Inactive	-	-	-	-

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

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