IBIS Open Forum Minutes

Meeting Date: **November 15, 2011**
Meeting Location: **Shanghai, China**

VOTING MEMBERS AND 2011 PARTICIPANTS

Agilent	Radek Biernacki, Fangyi Rao, Amolak Badesha
Altera	Hui Fu, Zhuyuan Liu, Julia Nekrylova, David Banas
AMD	Nam Nguyen
ANSYS (Ansoft)	Samuel Mertens, YanJun (Yuki) Chen*, Minggang Hou*, Rui Li*
Apple Computer	(Matt Herndon)
Applied Simulation Technology	Norio Matsui
Cadence Design Systems	Terry Jernberg, Ambrish Varma, Dennis Nagle, Martin Biehl, Yukio Masuko, Aileen Chen*, Lanbing Chen*, Yubao Meng*, Liu Ping*, Yitong Wen*, Dingru Xiao*, Benny Yan*, Jinhui Zhang*, Rong Zhang*, Weijan Zhang*, Alex Zhao*, Zhangmin Zhong*, Zhongyoung Zhou*
Cisco Systems	[Syed Huq], [Mike LaBonte], Luis Boluna, Ashwin Vasudevan, Zhiping Yang, Greg (Guan) Fu*, Xinyi Hu*, Jiang Wang*, Zhongfu Gu*, Lihua Yuan*, Xinghai Tang*, Yang Wu*, Chunyuan Zhou*
Ericsson	Anders Ekholm*
Foxconn Technology Group	(Sogo Hsu)
Freescale	(Jon Burnett)
Green Streak Programs	Lynne Green
Huawei Technologies	Xiaoqing Dong*, Yu (Jeff) Chen*, ZhenXing Hu*, Chunxing Huang*, Peng Huang*, Randy Zhao*, Hongxing Jiang*, Qiang Lin*, Longfang Lv*, Zhengrong Xu*, Zhou Yi*, Hongcheng Yin*, Tinghou Chen*, Luyu Ma*, Gezi Zhang*, Iris Lou*, Tuhua Yu*, Ying Zhang*
IBM	Adge Hawes, Greg Edlund
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Michael Mirmak*, Udy Shrivastava, Heather Monigan, Jinsong Hu*, Y.L. Li*, Yinglei Zheng*, Long Yang*, Weifeng Shu*
IO Methodology	Lance Wang*
LSI	Brian Burdick
Mentor Graphics	Arpad Muranyi, Ed Bartlett, Vladimir Dmitriev-Zdorov, Steve Kaufer, Chuck Ferry
Micron Technology	Randy Wolff, Andrea Spiezia, Roberto Izzi, Aniello Viscardi, Giovanni Guerra, Francesco Madonna, Giuseppe Fusillo
Nokia Siemens Networks GmbH	Eckhard Lenski, Xiaoguang Cai*, Hongwei Fu*, Bruce (Zhenshui) Qin*, Xiaoping Yang*, Xiangpeng Yao*, Jieping Zhang*, Xianzhao Zhao*
QLogic	David Choe, James Zhou
Signal Integrity Software	Walter Katz, Todd Westerhoff, Mike Steinberger,

	Barry Katz, Mike LaBonte
Sigrity	Raymond Chen*, Kumar Keshavan, Yingxin Sun Li Li*, Kezhou Li*, Jing Wang*, Xingfeng Li*, Haisan Wang*, Zuli Qin*, Lily Luo*
Synopsys	Andy Tai*, Ted Mido, Scott Wedge, Xuefeng Chen*, Maggie Dai*, Zerui Fan*, Wenyun Gu*, Jianghua Huang*, Bo Liu*
Teraspeed Consulting Group	Bob Ross*, Kellee Crisafulli, Tom Dagostino, Scott McMorrow
Texas Instruments (National Semiconductor - merged with TI)	Casey Morrison, Alfred Chong [Hsinho Wu], Pegah Alavi, John Goldie
Toshiba	(Tetsuya Endo)
Xilinx	(Raymond Anderson)
ZTE	Bi Yi*, HuaZheng Cao*, Fenling Gao*, Xiaolin Ghen*, Mai Hu*, Wei Jia*, Hui Jiang*, Ganghui Li*, Wanming Mao*, Baofei Qian*, Anbing Sun*, Hao Tian*, Junfeng Wang*, Yingxin Wang*, Yunfeng Wang*, Meihua Xu*, Changgang Ying*, Qiang Zhang*, Wei Zhou*, Zhi Zhou*, Jiangrong Xiao*, Xiaobing Zhang*, Zhiwei Yang*, Shenghu Wang*, Dawei Sun*, Cheng Li*, Lu Li*, Li Wang*, Renjie Wang*, Jie Yu*, Shunlin Zhu*
Zuken	(Michael Schaeder)

OTHER PARTICIPANTS IN 2011

3M	Kylin Chen*, Shiang Yao*
AET	Mikio Kiyono
Anymid Group	Charles Zhou*
Apache Design Solutions	Shulong Wu*
Arrow Electronics	Ian Dodd
Avant Technology	Enson Lee*
Avago	Weiping He, Minh Quach, Sari Tocco
Bayside Design	Elliot Nahas
Broadcom	Mohammad Ali
Celestica	Sophia Feng*, Lily Dai*, Jason Liu*, Yunqiang Meng*, Junwei Zhang*, Harrison Xue*, Van Zhu*
CST	Martin Schauer
East China Normal University	Mengting Liao*
Eastwell	David Wu*
EDADOC Technology	Hansheng Ke*, Bruce Wu*
EMC Corporation	Abigail Jiang*, Peng (Tony) Liu*, Lynn Kong*, Chambers Yin*
E-Train Technology	Weiming (David) Lu*
Exar Corporation	Helen Nguyen
Flextronics	Golden Qiang*
Granite River Labs	Johnson Tan, Mike Engbretson, Quintin Anderson
H3C Technologies	Huanyang Chen*, Haitao Zhang*, Xiaoqun Li*
High Speed Design Center	Ben Chia
ICT-Lanto	Steven Wong
IMU	Runjong Zhou*

Inventec	Zhong Peng*
JEITA	Atsushi Ishikawa
KEI Systems	Shinichi Maeda
Lecroy	Derek Hu*
Marvell Semiconductor	Fang Lv*, Guobing Han*, Yuyang Wang*, Liang Wu*, Michael Wang*, Xike Liu*, Zhiqiang Li*
Maxim Integrated Products	Hassan Rafat
Mindspeed	Jeff Li, Lyn Wang
NetLogic	Ryan Coutts, Antonis Orphanou
Oracle	Gustav Blando
Pericom Semiconductor	Zhangqi Guo*, Jun Li*, Qing Mao*
Politecnico di Torino	Igor Stievano, Stefano Grivet-Talocia
Pristine Signals	AbdulRahman (Abbey) Rafiq
Renesas Electronics	Takuji Komeda
Samsung Electronics	Il Seong
Siemens	Manfred Maurer
Simberian	Yuriy Shlepnev
Spreadtrum Communications	Xianyu Meng*
ST Microelectronics	Fabio Brina, Alan Smith
TechAmerica	(Chris Denham)
Tellabs	Yuehui Zhu*
Thales Communication	Alexandre Amedeo, Cyrip Chastang
Tianma Micro-electronics	Xiaoyan Lai*, Shengjie Yang*
Trident Microsystems	Andy (Zhiguang) Li*
University of Illinois	Jose Schutt-Aine
University of L'Aquila	Danilo di Febo
Vitesse Semiconductor	Siris Tsang
Xpeedic Technology	Feng Ling*, Wenliang Dai*, Shisheng Wu*
Independent	Yoichi Niioka, [Mike LaBonte], Mingwei Chen*, Liping Wang*

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
November 18, 2011	Asian IBIS Summit – Yokohama – no teleconference	
November 21, 2011	Asian IBIS Summit – Taipei – no teleconference	
December 9, 2011	205 475 958	IBIS

For teleconference dial-in information, use the password at the following website:

https://ciscosales.webex.com/ciscosales/j.php?J=205475958

All teleconference meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the

prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

The statements below summarize the material presented. More details are available through the summit presentations posted online at:

http://www.eda.org/ibis/summits/nov11a/

The Asian IBIS Summit (Shanghai) took place on Tuesday, November 15, 2011 at the Parkyard Hotel in Shanghai. Approximately 152 people from 33 organizations attended.

Michael Mirmak convened the meeting and introduced Chunxing Huang of Huawei for his comments. Chunxing welcomed the attendees and thanked the IBIS Open Forum for their ongoing support of the IBIS Summit series in the People's Republic.

Michael continued the meeting by thanking the co-sponsors: the major sponsor Huawei Technologies, Agilent Technologies, ANSYS, Cadence Design Systems, Intel Corporation, IO Methodology, Sigrity, Synopsys and ZTE Corporation.

IBIS STATUS AND FUTURE DIRECTION
Michael Mirmak (Intel Corporation, USA)

Michael Mirmak summarized the recent accomplishments of the IBIS Open Forum as an organization. He noted the recent approval of IBIS-ISS, a specification to describe SPICE interconnect subcircuits, and how it offers an opportunity to update support offered by EBD, PKG and ICM. Michael also presented plans for changes to the IBIS and Touchstone specifications, to take effect within the next few months.

Chunxing Huang asked about backchannel support. Michael noted that a BIRD had recently been filed to address this.

IBIS MODEL AS DE-FACTO STANDARD
Kazuhiko Kusunoki* and Wenliang Dai** (*WADOW, Japan and **Xpeedic Technology, China)

Wenliang Dai presented an analysis of identical IBIS models across six different simulation tools, using a simple differential transmission line pair, terminated outside the receiving device. The evaluated result was simply the crossing point of the complementary single-ended signals, with differences as much as 160 mV noted between tools. Wenliang noted that JEITA has established a quality framework for IBIS models, but a similar document may be required for simulation tools. He concluded by noting that different tool users can obtain different results, even for the same tool and models.

Audience questions included inquiries on the exact correlation metrics and the sensitivity or resolution of the simulators used. Additionally, Wenliang clarified that the IBIS models used included V-t curve tables.

IBIS VT WAVEFORM AND OVER CLOCKING
Xuefeng Chen (Synopsys, China)

Xuefeng reviewed the treatment of V-t tables for buffers when the operating frequency in simulation is higher than the frequency targeted by the design. The length (time duration) of the V-t tables becomes a problem, as buffers will switch before some or all of the V-t tables will complete transitions from start to finish. Xuefeng noted that solutions include removing unchanging portions of the waveform or removing initial delays. However, these may conflict with the IBIS Cookbook, due to the requirement for output stability and may also conflict with the [Composite Current] power delivery keyword, as useful information would be removed.

Michael Mirmak asked whether removing the same amount of time between V-t table corners would be acceptable. Xuefeng replied that this approach would not address all the issues he raised.

IBIS PARSERS
Bob Ross (Teraspeed Consulting Group, USA)

Bob Ross described the basic coverage and features of the IBISCHK IBIS parser and the TSCHK2 Touchstone 2.0 parser. He also described the specific messages provided plus the bug reporting system for both.

One audience member asked about converting H and Y parameters from Touchstone 2 to Touchstone 1 format. Bob replied that H and Y parameters are 2-port only, and they are normalized to the given reference value in Touchstone 1. Touchstone 2 removes the normalization requirement, though not all tools may support this consistently.

DDR3 SYSTEM TIMING BUDGET ANALYSIS BY SI & PI CO-SIMULATION
Bi Yi, Ping Wang and Shunlin Zhu (ZTE Corporation, China)

Bi Yi summarized the traditional approach to DDR3 memory simulation, including how timing analysis is performed through budgets. While SI simulations and their resulting waveforms are used to calculate setup and hold margins, this approach doesn't include important power delivery, jitter or crosstalk effects. Bi showed how some jitter effects may be incorporated into the device models used in SI simulations for DDR3, eliminating some timing uncertainties. Additional advantages can be gained by using IBIS models rather than SPICE models, including significant speed improvements.

Audience questions included inquiries on fast/typical/slow splits in simulations plus clarifications on IBIS package models versus SPICE package models.

MODELING THE ON-DIE DE-CAP OF IBIS 5.0 PDN-AWARE BUFFERS
Lance Wang* and Randy Wolff** (*IO Methodology and **Micron Technology, USA)

Lance Wang reviewed the two recent improvements in IBIS 5.0 for modeling power delivery behaviors: [ISSO_PU]/[ISSO_PD] and [Composite Current]. Incorporating these into buffer models can result in very good matching to SPICE simulations. However, some current and voltage behaviors for non-ideal supplies may not be captured correctly without adding on-die package resistance and on-die decoupling circuits. Lance noted that some current IBIS keywords can help address these issues in limited cases, but that support for on-die power delivery features, including possibly those in BIRD145, should be added to ensure best accuracy.

POWER-AWARE I/O MODELING FOR HIGH-SPEED PARALLEL BUS SIMULATION
Zuli Qin#, Haisan Wang#, Jack W.C. Lin# and Raymond Y. Chen## (Sigrity, #China and ##USA)

Zuli Qin presented a summary of issues and solutions related to high-speed simulation and power delivery for parallel busses. Current memory interface speeds are increasingly limited by power delivery effects, which should be modeled in IBIS due to its speed and IP protection advantages. Zuli noted that IBIS 5.0 includes useful power delivery features, but still omits on-die power delivery network impedances and represents buffer capacitance too simply. Adding Zpd, Zpu and Zpg (power-ground impedance) elements through multi-lingual features can improve the accuracy of IBIS 5.0 while still preserving the IBIS speed advantage over SPICE. Zuli concluded by showing a case study of DDR3 power delivery effects modeled using IBIS 5.0 and "IBIS Plus" (using the multi-lingual power delivery elements).

THE APPLICATION OF IBIS-AMI MODEL CASCADED SIMULATION FOR 10 GIGABIT REPEATER SERIAL LINK ANALYSIS
Zhengrong Xu*, Luyu Ma*, Ken Willis**# and Haisan Wang**##, Lee Sledjeski*** and Nate Unger*** (*Huawei Technologies, China, **Sigrity, #USA and ##China, ***Texas Instruments, USA)

Zhengrong presented a brief overview of repeaters and related devices and how they may be modeled using IBIS-AMI for 10 Gbps interface simulations. For channels involving high loss, repeaters may be used but simulation is required to address areas outside the specification. Channels may be broken into two parts, with IBIS-AMI Init and GetWave used for the first and second parts, respectively, on either side of the repeater. The two-part channels are "cascaded", and simulation can be used to predict both system performance and the necessary device equalization settings. No additional modifications to IBIS-AMI are needed to support this scenario.

AMI APPLICATIONS IN HIGH-SPEED SERIAL CHANNEL ANALYSIS AND MEASUREMENT CORRELATION
Wei Jia, Anbing Sun and ShunLin Zhu (ZTE Corporation, China)

Wei presented correlation results for 10 Gbps serial interfaces between simulations and lab data. Two channels were simulated using IBIS-AMI and a SPICE tool for device modeling and 3D field solvers for the interconnect portions. Simulations with the same settings and data pattern showed some differences against the lab in terms of edge rate but good overall eye matching. Wei concluded by noting that IBIS-AMI implementation still has issues in the

industry, particularly with inconsistent tool usage of IBIS-AMI models, inconvenient configuration requirements and lack of adaptive DFE support.

PSEUDO TRANSIENT EYE ANALYSIS BY CONVOLUTION METHOD
Baolong Li (ANSYS, China)

Mingang Hou presented on behalf of Baolong Li. Mingang summarized how convolution can be used for both linear and non-linear systems to construct eyes. He also noted how pseudo-transient eyes can closely match SPICE transient eyes using step responses from SPICE simulation, with large increases in efficiency.

INTRODUCTION OF FEC IL GAIN ESTIMATION METHOD IN HIGH SPEED LINK
Xiaoqing Dong and Chunxing Huang (Huawei Technologies, China)

Chunxing Huang presented information on forward error correction (FEC) and how it can be used to compensate for lengthy, lossy channels. While FEC is beneficial for extending performance of longer channels, industry estimates of performance improvements in terms of dB tend to overestimate the benefits. Chunxing showed a modified method for predicting FEC performance. Additionally, he showed how random and burst errors may appear in serial-differential systems and how FEC performance may be affected by them. Chunxing noted that some current industry tools lack DFE coefficient outputs or voltage bathtub curve outputs, which makes incorporation of FEC into simulations difficult.

SUPPORTING EXTERNAL CIRCUIT AS SPICE OR S-PARAMETERS IN CONJUNCTION WITH I-V/V-T TABLES
Kent Drumstad*#, Adge Hawes*##, Taranjit Kukal**###, Feras Al-Hawari**#, Ambrish Varma**# and Terry Jernberg**# (*IBM, #USA, ##United Kingdom, **Cadence Design Systems, ###India and #USA) [Presented by Zhangmin Zhong, Cadence Design Systems, China]

Zhangmin Zhong presented on a proposal to add new keywords and features to IBIS to support S-parameters and SPICE. For specific cases, such as on-die terminations or on-die networks that vary with frequency, both SPICE circuit models and S-parameters can be highly useful. A simple way to combine these with traditional table-based IBIS model data is needed. While Touchstone files may be wrapped within a supporting SPICE circuit, a proposal is presented that supports Touchstone S-parameter files in IBIS directly. Further, some high-speed buffer behaviors may be more conveniently modeled in SPICE, but must be used in combination with existing IBIS data. Zhangmin concluded by showing an extended set of examples of syntax enabling IBIS buffer data to be combined with Touchstone or SPICE information, as proposed in BIRD 144 and BIRD 145.

BOARD-ONLY POWER DELIVERY PREDICTION FOR VOLTAGE REGULATOR AND MOTHER BOARD DESIGNS
Jiangqi He# and Y.L. Li## (Intel Corporation, #USA and ##China)

Y.L. Li presented a simplified approach for power delivery simulation using behavioral SPICE models. The method involves transient simulations based on resistor models of the PCB, R &

L modeling of any sockets, voltage regulator models and current-versus-time data from suppliers. The simplified model's transient results characterize the whole system and would be compared against targets provided by IC vendors. Y.L. showed case studies where voltage regulator performance could be assessed and numbers of decoupling capacitors could be optimized.

CONCLUDING ITEMS

Michael Mirmak thanked the co-sponsors, presenters and attendees for their participation and support and reminded the attendees to register. Lance Wang made a few announcements regarding gifts to the attendees. The meeting adjourned shortly after 5 PM.

NEXT MEETING

The Asian IBIS Summit – Yokohama will be held November 18, 2011. The Asian IBIS Summit – Taipei will be held November 21, 2011. The next IBIS Open Forum teleconference will be held December 9, 2011 from 8:00 to 10:00 AM US Pacific Time. Votes on BIRD127.4 and BIRD146 are scheduled.

==========

NOTES

IBIS CHAIR: Michael Mirmak (916) 356-4261, Fax (916) 377-3788
michael.mirmak@intel.com
Data Center Platform Applications Engineering
Intel Corporation
FM5-239
1900 Prairie City Rd.,
Folsom, CA 95630

VICE CHAIR: Lance Wang (978) 633-3388
lwang@iometh.com
President/CEO, IO Methodology, Inc.
PO Box 2099
Acton, MA 01720

SECRETARY: Randy Wolff (208) 363-1764, Fax: (208) 368-3475
rrwolff@micron.com
SI Modeling Manager, Micron Technology, Inc.
8000 S. Federal Way
Mail Stop: 01-711
Boise, ID 83707-0006

LIBRARIAN: Anders Ekholm (46) 10 714 27 58, Fax: (46) 8 757 23 40
ibis-librarian@eda.org
Digital Modules Design, PDU Base Stations, Ericsson AB
BU Network

Färögatan 6
164 80 Stockholm, Sweden

WEBMASTER: Mike LaBonte
mikelabonte@eda.org
IBIS-AMI Modeling Specialist, Signal Integrity Software
6 Clock Tower Place
Maynard, MA 01754

POSTMASTER: Mike LaBonte
mikelabonte@eda.org
IBIS-AMI Modeling Specialist, Signal Integrity Software
6 Clock Tower Place
Maynard, MA 01754

This meeting was conducted in accordance with the TechAmerica Legal Guides and TechAmerica Manual of Organization and Procedure.

The following e-mail addresses are used:

majordomo@eda.org

In the body, for the IBIS Open Forum Reflector:
subscribe ibis <your e-mail address>

In the body, for the IBIS Users' Group Reflector:
subscribe ibis-users <your e-mail address>

Help and other commands:
help

ibis-request@eda.org

To join, change, or drop from either or both:
IBIS Open Forum Reflector (ibis@eda.org)
IBIS Users' Group Reflector (ibis-users@eda.org)
State your request.

ibis-info@eda.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the IBIS Open Forum as a full Member.

ibis@eda.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/
http://www.eda.org/ibis/bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/
http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eda.org/ibis

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

To create an account on the TechAmerica KAVI workspace, check out:

http://workspace.techamerica.org/kwspub/join/

IBIS CURRENT MEMBER VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	September 16, 2011	October 7, 2011	October 28, 2011	November 15, 2011
Advanced Micro Devices	Producer	Active	X	X	X	-
Agilent Technologies	User	Active	X	-	X	-
Altera	Producer	Inactive	X	X	-	-
ANSYS	User	Inactive	-	-	-	X
Apple Computer	User	Inactive	-	-	-	-
Applied Simulation Technology	User	Inactive	-	-	-	-
Cadence Design Systems	User	Active	-	-	X	X
Cisco Systems	User	Inactive	-	-	-	X
Ericsson	Producer	Active	X	-	X	X
Foxconn Technology Group	Producer	Inactive	-	-	-	-
Freescale	Producer	Inactive	-	-	-	-
Green Streak Programs	General Interest	Inactive	-	-	-	-
Huawei Technologies	Producer	Inactive	-	-	-	X
IBM	Producer	Active	X	X	X	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	X	-	X
IO Methodology	User	Active	X	X	-	X
LSI	Producer	Active	-	X	X	-
Mentor Graphics	User	Active	X	X	X	-
Micron Technology	Producer	Active	X	X	X	-
Nokia Siemens Networks	Producer	Active	-	X	X	X
QLogic	Producer	Inactive	-	-	-	-
Signal Integrity Software	User	Active	X	X	X	-
Sigrity	User	Inactive	-	-	-	X
Synopsys	User	Inactive	-	-	-	X
Teraspeed Consulting	General Interest	Active	X	X	X	X
Texas Instruments	Producer	Inactive	-	-	-	-
Toshiba	Producer	Inactive	-	-	-	-
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	-	-	X
Zuken	User	Inactive	-	-	-	-

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH TECHAMERICA BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
- PRODUCERS - MEMBERS THAT SUPPLY ELECTRONIC EQUIPMENT.
- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.