IBIS Open Forum Minutes

Meeting Date: **November 12, 2010**
Meeting Location: **Taipei, Taiwan**

VOTING MEMBERS AND 2010 PARTICIPANTS

Agilent	Radek Biernacki, Ming Yan, Fangyi Rao, Gilbert Berger, Amolak Badeasa, Jose Pino, Junaid Khan, Charles Lu, Xuliang Yuan, Ming-Chih Lin*, David Huang*, Avery Chung*
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Ansys (Ansoft Corporation)	Danil Kirsanov, Baolong Li
Apple Computer	(Matt Herndon)
Applied Simulation Technology	(Fred Balistreri)
ARM	(Nirav Patel)
Cadence Design Systems	Terry Jernberg, Wenliang Dai*, Ambrish Varma Shisheng Wu, Lanbing Chen, Daisy Cheung, Fang Li, Sammi (Rong) Fu, William Fu, Weichun Ke, Ciron Wu, Jun Wu, Thunder Lay*
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Freescale	Jon Burnett, Om Mandhana
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Hitachi ULSI Systems	Yutaka Uematsu
Huawei Technologies	Jinjun Li, Zhenghua Yuan, Wencuan Gong, Jun Li, Zhipeng Luo, Dunxiong Song, Xiaoqing Dong, Chuyao Liu, Xinhao Bai, Yinwei Yan, Xinyun Lao, Gang Li, Gang Zhu, Zhang Li
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Mentor Graphics	Arpad Muranyi, Neil Fernandes, Zhen Mu, Jack Yang, Sophia Yang
Micron Technology	Randy Wolff*
Nokia Siemens Networks GmbH	Eckhard Lenski
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	Barry Katz
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Xilinx	Mike Jenkins
ZTE	Jian Pang, Ping Wang, Shunlin Zhu, Zhiwei Yang, Jinku Guan, Wei Jia, Nan Jian, Guanghui Li, Xian Lu, Yingxin Wang, Bi Yi, Wei Zhou, Shunlin Zhu
Zuken	Michael Schaeder, Ralf Bruening

OTHER PARTICIPANTS IN 2010

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Advantech	Josh Lin*
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Altek Corp.	Randy Hsiao*, Collin Tseng*
Altera	John Oh, Hui Fu
Apache Design Solutions	Shulong Wu
ASE Group	Marco Cheng*, AlexCC Wang*, Paddy Wu*
ASUSTek Computer	David Chou*, Yu-Ching Liao*, Vincent Lu*
Avago	Razi Kaw
Avant Technology	Megy Wang, Raymond Chen, Yao-Chang Chang*, Jill Chen*, Jyam Huang*, Mandy Yang*
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Broadcom	Mohammad Ali
CeraMicro Technology	Vivian Wu*
Chang-Gung University	Jefferson (Chzu-Chinag) Tseng*
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Curtiss-Wright	John Phillips
Delta Network	Skipper Liang*, Min-Hong Tsai*
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Etron	Chunmu Lin*, Stu Tsai*
eSilicon	Hanza Rahmai
EVOC Intelligent Technology	ChangQian Yu
Exar Corp.	Helen Nguyen

Faraday Technology	Way Chin-Wei Chang*, Wells Jong*, Jung-Chi Ho*, Boris Tseng*, Pao Sun*
Flextronics	Tommy Chan*, Sam Chuang*, John Lin*, Trina Shih*, Alan Sun*, Devin Tsai*, Cathy Tu*, Panda Wang*
Foxconn Technology Corp.	Cortex Chen*, Ted Chou*, Danny Ho*, Sogo Hsu*, Daniel Lai*, Scott Li*, Frank Pai*, Weiliang Tseng*, Eric Wu*, Joyce Yeh*
Giga-byte Technology	Eric Chien*, Corey Huang*, Andy Lee*, Alex Lu*
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Himax Technologies	Wei-De (Brian) Kuo*
Huawei Symantec Technologies	Zihong Zhang, Jieping Zheng, Qinglin Zhou Yongyao Li, Guanghui Liu, Yalun Liu, Hongjun Bi, Senliang Han, Chuanbing Li, Qiangqiang Wang, Kang Wei
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Inventec	Ian Chen*, Elien Tseng*
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Mindspeed	Bobby Altaf
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National University of Kaohsiung (NUK)	Ming Haei Huang*, Kao-Yi Wang*
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Siemens, AG.	Manfred Maurer, Michael Flint
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TechAmerica	(Chris Denham)
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YanHua Technology	Xiuchun Peng
ZyXEL Communications Corp.	Frank Chang*
Independent	AbdulRahman (Abbey) Rafiq, Robert Badal

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
November 15, 2010 – Asian IBIS Summit in Tokyo, Japan – no teleconference		
November 19, 2010	204 170 411	IBIS

For teleconference dial-in information, use the password at the following website:

https://cisco.webex.com/cisco/j.php?J=204170411

All teleconference meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

WELCOME AND KEYNOTE COMMENTS

The IBIS Open Forum summit was held in Taipei, Taiwan at the Sherwood Hotel. About 121 people representing 42 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda.org/pub/ibis/summits/nov10b/

Michael Mirmak opened the 1st Asian IBIS Summit - Taiwan meeting with a brief welcome announcement.

Sogo Hsu of Foxconn Technology Group began the meeting shortly after 9:00 AM. Sogo noted that there are many silicon designers and computer companies in Taiwan. Sogo welcomed the participants and expressed appreciation to the IBIS Committee and sponsors for holding the event.

Michael Mirmak also welcomed everyone to the Asian IBIS Summit. He introduced Lance Wang, IBIS Vice Chair, Randy Wolff, IBIS Secretary, and Anders Ekholm, IBIS Model Librarian. He also thanked Bob Ross who organized much of the meeting. He discussed the importance of standards and standards organizations. He noted that IBIS is a common language that allows us to communicate amongst each other. This summit was made possible by 7 co-sponsors, and he pointed to the backdrop showing the logos of Agilent Technologies, Avant Technologies, Foxconn, ICT-Lanto, Intel Corporation, Sigrity and Synopsys.

Lance Wang surveyed the attendees. He noted that most of the attendees were IBIS users, with only a few vendors present.

INTRODUCING IBIS

Michael Mirmak (Intel Corporation, USA)

Michael gave a brief introduction to the IBIS standard. The specification is currently at version 5.0. Recent extensions to IBIS add support for AMS and AMI modeling. IBIS now manages the Touchstone specification. Changes to IBIS are made through the BIRD process. IBIS parser issues are noted as BUGs. TSIRDs are issued for Touchstone issues. Two email reflectors are available for discussion of IBIS issues and usage. Teleconferences are held every three weeks. Several task groups also work on specific IBIS issues. More information on IBIS is found on the IBIS website at:

http://www.eda.org/ibis

POINT REDUCTION METHOD FOR IBIS CURVES

Lance Wang (IO Methodology, USA)

Lance Wang described how a point reduction system uses algorithms for proper point number reduction with minimum sacrifices to accuracy. A point reduction method is useful in IBIS for representations of I-V curves with only 100 data points. The IBIS cookbook mentions two methods: points selected with a regular interval or using a ‘greatest change’ algorithm. The interval spacing method is easy but may lack enough detail in some areas of the curves. He described the methodology of developing a ‘greatest change’ algorithm. The two methods were compared to a Golden Waveform curve to show the superiority of the ‘greatest change’ method. The ‘greatest change’ algorithm works well with IBIS V-t curve point reduction but may still cause inaccuracies in I-V curves. This inaccuracy was demonstrated by showing simulation

results to a test circuit. Lance then introduced a 'Weighted Best Point' (WBP) method. The WBP method combines the 'regular interval' and 'greatest change' methods by focusing the 'greatest change' method on the working range of the I-V curves. This method improves accuracy.

IBIS FOR SSO ANALYSIS

Haisan Wang#, Joshua Luo##, Jack Lin##, Zhangmin Zhong# (Sigrity, #PRC and #ROC)

Joshua Luo began with an overview of a traditional I/O SSO analysis investigating PDN noise and crosstalk. He listed fundamentals of SSO mechanisms. Simulations of power supply voltage noise were compared to measurements. SSO simulation requires models of boards, packages and IO buffers. IBIS buffer model accuracy is questionable for Power Integrity (PI) analysis as compared to a SPICE model. SPICE limitations make use of IBIS for PI analysis a requirement. IBIS models of Version 4.2 or older do not model pre-driver currents which can have significantly higher dI/dt than the driver current. Crowbar current can be modeled fairly well when all four sets of V-t curves are in the IBIS model, but pre-driver currents are missing. The BIRD95 [Composite Current] keyword found in IBIS 5.0 adds pre-driver current characteristics to the IBIS model. Using [Composite Current] results in significantly improved correlation to SPICE results. A BIRD95 model is still missing the on-die decoupling capacitor between power and ground. Adding an RC circuit for this capacitance in parallel with the IBIS driver improves the model accuracy: oscillations occur at the proper frequencies and the SSO magnitude is correct. Simulations were compared to measurements with good correlation. IBIS 5.0 improves accuracy in SSO simulation.

CORRELATING C_PIN CAPACITANCE WITH MEASUREMENTS

Randy Wolff (Micron Technology, USA)

Randy noted that C_pin, the per-pin capacitance found in the [Pin] section of an IBIS model, is typically found through 3-D field solvers and is the diagonal element of the capacitance matrix. This value is also called the Maxwell capacitance and is the total capacitance of the pin with all other pins of the package grounded. When capacitance of a packaged device is measured, each signal is usually referenced to power and ground with all other pins of the package left floating. Due to other pins floating, measured capacitance is not the same as Maxwell capacitance. Correlating a model to measurement becomes difficult when the capacitance values are different. Analyzing the correct capacitance is also important when comparing a package capacitance simulation to datasheet specifications which are measurement based.

Randy described a method of using matrix math to convert a capacitance matrix from a field solver into measured capacitance values, taking into account other signals in a floating state instead of being grounded. He noted that Micron developed a spreadsheet macro tool to do this conversion using inputs from many common field solver tools. He showed a chart comparing measured versus simulated C_pin values for a 2-layer BGA package. He noted that the largest difference occurred on signals that were the least coupled to powers and grounds. He concluded that capacitance matrix data must be manipulated when comparing it to measured capacitance.

A question was asked if C_pin(measured) should be used for C_pin in the IBIS model. Randy clarified that the Maxwell capacitance is ok to use for C_pin.

ENFORCED PASSIVITY OF S-PARAMETER SAMPLED FREQUENCY DATA

Wenliang Tseng, Sogo Hsu, Frank Y.C. Pai, Scott C.S. Li (Foxconn Technology Group, ROC)

Wenliang noted that S-parameter data used in simulation is shared in the Touchstone format. He showed the effect in simulation of a causality violation and a passivity violation. Passivity and causality conditions were defined. Current methods for checking passivity look for eigenvalues less than zero or greater than one. Simple and perturbation methods for correcting data to be passive are not adequate. Passivity enforcement is improved by using a rational function approximation with a vector fitting algorithm to correct the S-parameter data. Wenliang proposed defining a common-pole rational function file standard. The file would present full spectrum S-parameter data, and causality and passivity could be guaranteed. The file size is also significantly reduced from the original Touchstone file size.

A question was asked about how much simulation time can be reduced using the rational function. Wenliang responded that it was reduced by 95% when using a rational function method for modeling the S-parameter data in some simulators. A question was asked about what determines the number of poles that must be used for the rational function. Wenliang responded that the number is determined by the desired accuracy, range of frequency data and number of ports.

AUTOMATED AMI MODEL GENERATION AND VALIDATION

Jose Luis Pino*, Amolak Badesha*, Manuel Luschas**, Antonis Orphanou**, Halil Civit** (*Agilent Technologies and **NetLogic Microsystems, USA)

Ming-Chih Lin of Agilent Technologies, China gave the presentation. He noted that AMI model generation takes significant time and resources. Models are now coming late in the design cycle and are used only for validation, not design. Typical SI engineers are not programmers. The challenge is to convert algorithmic design code into the AMI format. An automated AMI model generation flow is needed to shorten the model development cycle. Ming-Chih defined Electronic System Level (ESL) design as a methodology that focuses on the higher abstraction level concerns first and foremost. He showed examples of SerDes modeling using the ESL flow. FIR filter models should support arbitrary sampling rates. A generic model library speeds up the process, but for customized IP, you must still bring in math code or C++ code. Simulation results for an Rx model at SATA 3.0 (6 Gb/s) and 10-Gb Ethernet speeds were shown. An AMI model correlation study looked at transistor simulation and measurements versus the AMI model. The correlation results looked very good.

EXTENDING/LEVERAGING IBIS CONSTRUCTS TO MODEL HIGH-SPEED I/O'S AND PACKAGES USING AMI, SPICE, AND S-PARAMETERS

John Lin*, Feras Al-Hawari**##, Taranjit Kukal**# and Ambrish Varma**## (*Flextronics, ROC and **Cadence Design Systems, #India and ##USA)

Kevin Liu of Cadence, ROC delivered the presentation. With current IBIS constructs, RDL and/or pin parasitic are lumped into pin R/L/C values. At high frequencies, IO buffers could have portions that need to be modeled using Spice files such as On-die termination with frequency dependence. Multiple Spice subcircuits could be used to model different process corners, buffer configurations or dynamic ODT. There are many limitations to current inclusion of Spice subcircuits with [External Model]. [External Model] could be leveraged to support S-parameter package modeling. Long term, IBIS could have keywords to support S-parameters

under the Package section to provide port mapping and prompt SI tools to ignore RLC values. An example was shown of using [External Model] to include an S-parameter package model. Package RLC values were zeroed out when doing this to avoid double-counting. Kevin proposed extending [External Model] to point to Spice sub-circuits that augment V-I and V-t data for complete characterization of the IO buffer. [External Model] would also be extended to allow dynamic switching of subcircuits for corners and parametric variations. AMI models should also work in conjunction with [External Model].

IBIS-ISS: WHAT IS IT AND WHAT IT MEANS TO YOU

Michael Mirmak (Intel Corporation, USA)

Michael noted that the problem with SPICE model portability is that a standard SPICE does not exist. IBIS-ISS (Interconnect SPICE Subcircuits) establishes an industry standard baseline for interconnect modeling in SPICE. It defines a limited set of common, basic elements useful for SI interconnect modeling. It is based on documents and concepts donated by Synopsys as seen in Synopsys HSPICE. IBIS-ISS was developed with the SI community through the IBIS Interconnect task group. IBIS-ISS supports fundamental circuit elements, subcircuit definitions and instantiation and some other basic commands, but no engine commands, no active device support and no field solver.

IBIS-ISS consists entirely of subcircuits, so it does not define netlists. All parameters are local and passed explicitly. Multiple files are supported. Good SPICE habits will make IBIS-ISS adoption and use easier. Michael listed several IBIS-ISS rules to follow. Draft 0.7 is now in review and a parser is under consideration. Michael encouraged questions and comments.

A question was asked about what dependent sources are supported. Michael responded that details are in the specification draft. Not all options are currently being supported for the dependent sources, as they are not meant to be able to model active elements through PWL options for instance. A question was asked about whether there is a cookbook for IBIS-ISS. Michael responded that one may be developed once the specification is finished. A question was asked about why IBIS-ISS is necessary when IBIS has package models and other options. Michael responded that IBIS-ISS allows for new types of lossy modeling. Lance Wang added that IBIS-ISS could be useful for improving EBD modeling.

MODEL CONNECTION PROTOCOL EXTENSIONS FOR MIXED SIGNAL SIP

Taranjit Kukal*#, WenLiang Dai*##, Brad Brim** and Eiji Fujine*** (*Cadence Design Systems, #India, ##PRC, **Sigrity, USA and ***Fujitsu VLSI Limited, Japan)

WenLiang described how chip/package/board connections can have 100s to 1000s of physical connections, but not all electrical nodes can have per-pin resolution. A method is needed to group pins and auto-connect models across the chip/package/board boundaries. Model Connection Protocol (MCP) establishes pin grouping and mapping of physical to electrical nodes. MCP extensions can be used for mixed-signal System-in-Package (SiP) power delivery analysis. Connecting two disparately pin-grouped models is possible by choosing to short together electrical nodes that have overlapping pin domains. Support for modules is needed in MCP as a category for structures drawing power within the package such as RF modules and metal passive structures. Connections by reference designator instead of x-y location are another recommended extension to existing MCP. An optional column showing connection by REFDES makes for easy mapping for mixed-signal modules and pre-layout analysis.

CONCLUDING ITEMS

Michael Mirmak thanked all the co-sponsors who made the event possible. He also thanked the presenters for the excellent presentations and the attendees. He invited people to subscribe to the IBIS email reflectors. The meeting adjourned at approximately 4:05 PM.

NEXT MEETING

The next IBIS Open Forum summit will be held November 15, 2010 in Tokyo, Japan. The next IBIS Open Forum teleconference will be held November 19, 2010 from 8:00 to 10:00 AM US Pacific Standard Time. A vote on BIRD113 is scheduled.

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NOTES

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This meeting was conducted in accordance with the GEIA Legal Guides and GEIA Manual of Organization and Procedure.

The following e-mail addresses are used:

majordomo@eda.org

In the body, for the IBIS Open Forum Reflector:
subscribe ibis <your e-mail address>

In the body, for the IBIS Users' Group Reflector:
subscribe ibis-users <your e-mail address>

Help and other commands:
help

ibis-request@eda.org

To join, change, or drop from either or both:
IBIS Open Forum Reflector (ibis@eda.org)
IBIS Users' Group Reflector (ibis-users@eda.org)
State your request.

ibis-info@eda.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the EIA-IBIS Open Forum as a full Member.

ibis@eda.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/
http://www.eda.org/ibis/bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/
http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eigroup.org/ibis/ibis.htm

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

IBIS CURRENT MEMBER VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	October 1, 2010	October 22, 2010	November 9, 2010	November 12, 2010
Advanced Micro Devices	Producer	Inactive	X	-	-	-
Agilent Technologies	User	Active	-	X	X	X
Ansys	User	Inactive	-	-	X	-
Apple Computer	User	Inactive	-	-	-	-
Applied Simulation Technology	User	Inactive	-	-	-	-
ARM	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Active	-	X	X	X
Cisco Systems	User	Inactive	X	X	-	-
Ericsson	Producer	Active	-	X	X	X
Freescale	Producer	Inactive	-	-	-	-
Green Streak Programs	General Interest	Inactive	-	-	-	-
Huawei Technologies	Producer	Inactive	-	-	X	-
Hitachi ULSI Systems	Producer	Inactive	-	-	-	-
IBM	Producer	Active	X	X	-	X
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	X	X	X
IO Methodology	User	Active	X	-	X	X
LSI	Producer	Inactive	X	X	-	-
Mentor Graphics	User	Active	X	X	X	-
Micron Technology	Producer	Active	X	X	X	X
Nokia Siemens Networks	Producer	Inactive	-	X	-	-
Samtec	Producer	Inactive	-	-	-	-
Signal Integrity Software	User	Inactive	X	X	-	-
Sigrity	User	Active	-	-	X	X
Synopsys	User	Inactive	-	-	X	-
Teraspeed Consulting	General Interest	Active	X	X	X	X
Texas Instruments	Producer	Inactive	-	-	-	-
Toshiba	Producer	Inactive	-	-	-	-
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	-	X	-
Zuken	User	Inactive	-	-	-	-

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

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