IBIS Open Forum Minutes

Meeting Date: **November 9, 2010**
Meeting Location: **Shenzhen, P. R. China**

VOTING MEMBERS AND 2010 PARTICIPANTS

Agilent	Radek Biernacki, Ming Yan, Fangyi Rao, Gilbert Berger, Amolak Badeasa, Jose Pino, Junaid Khan, Charles Lu*, Xuliang Yuan*
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Ansys (Ansoft Corporation)	Danil Kirsanov, Baolong Li*
Apple Computer	(Matt Herndon)
Applied Simulation Technology	(Fred Balistreri)
ARM	(Nirav Patel)
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Hitachi ULSI Systems	Yutaka Uematsu
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LSI	Brian Burdick
Mentor Graphics	Arpad Muranyi, Neil Fernandes, Zhen Mu, Jack Yang*, Sophia Yang*
Micron Technology	Randy Wolff*
Nokia Siemens Networks GmbH	Eckhard Lenski
Samtec	(Corey Kimble)
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Sigrity	Brad Brim, Kumar Keshavan, Srdjan Djordjevic, Ben Franklin, Zhangmin Zhong*, Raymond Y. Chen*, Xianfeng Li*, Haisan Wang*

Synopsys	Ted Mido, Paul Lo, Geoffrey Ying, Frank Lee, Xuefeng Chen*, Deng Shi*
Teraspeed Consulting Group	Bob Ross*, Tom Dagostino
Texas Instruments	Bonnie Baker
Toshiba	Yoshihiro Hamaji
Xilinx	Mike Jenkins
ZTE	Jian Pang*, Ping Wang*, Shunlin Zhu*, Zhiwei Yang*, Jinku Guan*, Wei Jia*, Nan Jian*, Guanghui Li*, Xian Lu*, Yingxin Wang*, Bi Yi*, Wei Zhou*, Shunlin Zhu*
Zuken	Michael Schaeder, Ralf Bruening

OTHER PARTICIPANTS IN 2010

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Apache Design Solutions	Shulong Wu*
Avago	Razi Kaw
Avant Technology	Megy Wang*, Raymond Chen*
Bosch Car Multimedia	Rene Steinberg, Patric Kessler
Broadcom	Mohammad Ali
China Fastprint	Matthew Li*, Mark Long*
Curtiss-Wright	John Phillips
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eSilicon	Hanza Rahmai
EVOC Intelligent Technology	ChangQian Yu*
Exar Corp.	Helen Nguyen
Hanpu Electronics	Chijiang Way*, Pinting Hu*
Huawei Symantec Technologies	Zihong Zhang*, Jieping Zheng*, Qinglin Zhou* Yongyao Li*, Guanghui Liu*, Yalun Liu*, Hongjun Bi*, Senliang Han*, Chuanbing Li*, Qiangqiang Wang*, Kang Wei*
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JEITA	Atsushi Ishikawa
Leading Edge	Pietro Vergine
Lenovo	Mandy Yang*, Lu Zhang*
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Mindspeed	Bobby Altaf
National Semiconductor	Hsinho Wu
NetLogic Microsystems	Eric Hsu, Edward Wu, Antonio Orphanou, Halil Civit
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NXP Semiconductors	Gerald Krasemann
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	Flavio Canavero
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Simberian	Yuriy Shlepnev
Span Systems Corporation	Vidya (Viddy) Amirapu
Summit Computer Systems	Bob Davis
Tabula	David Banas
TechAmerica	(Chris Denham)
Vitesse Semiconductor	Bob McDonough
YanHua Technology	Xiuchun Peng*
Independent	AbdulRahman (Abbey) Rafiq, Robert Badal

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
November 12, 2010 – Asian IBIS Summit in Taipei, Taiwan – no teleconference		
November 15, 2010 – Asian IBIS Summit in Tokyo, Japan – no teleconference		
November 19, 2010	204 170 411	IBIS

For teleconference dial-in information, use the password at the following website:

https://cisco.webex.com/cisco/j.php?J=204170411

All teleconference meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

WELCOME AND KEYNOTE COMMENTS

The IBIS Open Forum summit was held in Shenzhen, P.R. China at the Four Points Sheraton Hotel. About 81 people representing 24 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda.org/pub/ibis/summits/nov10a/

Michael Mirmak opened the 6th annual Asian IBIS Summit meeting with a brief welcome announcement.

Jinjun Li of Huawei Technologies began the meeting shortly after 9:20 AM. Jinjun welcomed the participants and expressed appreciation to the IBIS Committee and sponsors for holding the event.

Michael Mirmak also welcomed everyone to the Asian IBIS Summit. He introduced Lance Wang, IBIS Vice Chair, Randy Wolff, IBIS Secretary, and Anders Ekholm, IBIS Model Librarian. He also thanked Bob Ross who organized much of the meeting. He noted that IBIS is a common language that allows us to communicate amongst each other. Over the years the summit has accumulated 12 co-sponsors to make the meeting possible, and he pointed to the backdrop showing the logos of Agilent Technologies, Ansys (Ansoft), Cadence Design Systems, Cybernet Systems, Huawei Technologies, Intel Corporation, IO Methodology, Mentor Graphics, SiSoft, Sigrity, Synopsys and ZTE Corporation.

POINT REDUCTION METHOD FOR IBIS CURVES

Lance Wang (IO Methodology, USA)

Lance Wang described how a point reduction system uses algorithms for proper point number reduction with minimum sacrifices to accuracy. A point reduction method is useful in IBIS for representations of I-V curves with only 100 data points. The IBIS cookbook mentions two methods: points selected with a regular interval or using a 'greatest change' algorithm. The interval spacing method is easy but may lack enough detail in some areas of the curves. He described the methodology of developing a 'greatest change' algorithm. The two methods were compared to a Golden Waveform curve to show the superiority of the 'greatest change' method. The 'greatest change' algorithm works well with IBIS V-t curve point reduction but may still cause inaccuracies in I-V curves. This inaccuracy was demonstrated by showing simulation results to a test circuit. Lance then introduced a 'Weighted Best Point' (WBP) method. The WBP method combines the 'regular interval' and 'greatest change' methods by focusing the 'greatest change' method on the working range of the I-V curves. This method improves accuracy.

IBIS FOR SSO ANALYSIS

Haisan Wang, Joshua Luo, Jack Lin, Zhangmin Zhong (Sigrity, China)

Haisan began with an overview of a traditional I/O SSO analysis investigating PDN noise and crosstalk. He listed fundamentals of SSO mechanisms. Simulations of power supply voltage noise were compared to measurements. SSO simulation requires models of boards, packages and IO buffers. IBIS buffer model accuracy is questionable for Power Integrity (PI) analysis as compared to a SPICE model. SPICE limitations make use of IBIS for PI analysis a requirement. IBIS models of Version 4.2 or older do not model pre-driver currents which can have significantly higher dI/dt than the driver current. Crowbar current can be modeled fairly well when all four sets of V-t curves are in the IBIS model, but pre-driver currents are missing. The BIRD95 [Composite Current] keyword found in IBIS 5.0 adds pre-driver current characteristics to the IBIS model. Using [Composite Current] results in significantly improved correlation to

SPICE results. A BIRD95 model is still missing the on-die decoupling capacitor between power and ground. Adding an RC circuit for this capacitance in parallel with the IBIS driver improves the model accuracy: oscillations occur at the proper frequencies and the SSO magnitude is correct. Simulations were compared to measurements with good correlation. IBIS 5.0 improves accuracy in SSO simulation.

A question was asked about how to model the Cpwr_gnd and Rpwr_gnd elements since these elements are not supported in IBIS currently. Bob Ross noted that the IBIS Series model elements can be used with [Series Pin Mapping] to model these currently. IBIS ISS may allow for better modeling in the future.

PDN DESIGN AND ANALYSIS METHODOLOGY IN SI & PI CO-DESIGN

Zipeng Luo, Suyao Liu (Huawei Technologies, China)

Zipeng noted that SI and PI co-design is a challenge. Independent SI and PI analyses have limitations. He showed key parameters in PDN design. At the board level, high frequency decoupling capacitors and the power and ground plane design is important in PDN design. The loop inductance of the high frequency capacitors may be dominated by via inductance, up to 75-80% of the total loop inductance. He compared capacitor decoupling effects with different via inductances. Plane spreading inductance can be reduced by locating decoupling capacitors directly underneath the IC, usually on the opposite side of the PCB. With power and ground plane spacing of more than 30 mils, high frequency capacitors show a local effect due to resonance. With power and ground plane spacing less than 10 mils, high frequency capacitors show a global effect due to resonance increasing in frequency. SSN analysis with an IBIS model including PDN models enhances simulation efficiency and speed.

CORRELATING C_PIN CAPACITANCE WITH MEASUREMENTS

Randy Wolff (Micron Technology, USA)

Randy noted that C_pin, the per-pin capacitance found in the [Pin] section of an IBIS model, is typically found through 3-D field solvers and is the diagonal element of the capacitance matrix. This value is also called the Maxwell capacitance and is the total capacitance of the pin with all other pins of the package grounded. When capacitance of a packaged device is measured, each signal is usually referenced to power and ground with all other pins of the package left floating. Due to other pins floating, measured capacitance is not the same as Maxwell capacitance. Correlating a model to measurement becomes difficult when the capacitance values are different. Analyzing the correct capacitance is also important when comparing a package capacitance simulation to datasheet specifications which are measurement based.

Randy described a method of using matrix math to convert a capacitance matrix from a field solver into measured capacitance values, taking into account other signals in a floating state instead of being grounded. He noted that Micron developed a spreadsheet macro tool to do this conversion using inputs from many common field solver tools. He showed a chart comparing measured versus simulated C_pin values for a 2-layer BGA package. He noted that the largest difference occurred on signals that were the least coupled to powers and grounds. He concluded that capacitance matrix data must be manipulated when comparing it to measured capacitance.

A question was asked about the largest delta seen between C_pin and C_pin(measured).

Randy responded that 100fF is the largest delta as shown in the LPDDR (worst case) package. Another question was asked about defining nets within the spreadsheet. Randy answered that signals are all considered floating and power and ground pins that are references in the measurement are considered grounded. One comment was made on the ability of existing software tools to give these values. Randy commented that the spreadsheet method was compared to a simulation with exactly the same results but with much reduced time involved.

AUTOMATED AMI MODEL GENERATION AND VALIDATION

Jose Luis Pino*, Amolak Badesha*, Manuel Luschas**, Antonis Orphanou**, Halil Civit** (*Agilent Technologies and **NetLogic Microsystems, USA)

Xuliang Yuan of Agilent gave the presentation. He noted that AMI model generation takes significant time and resources. Models are now coming late in the design cycle and are used only for validation, not design. Typical SI engineers are not programmers. The challenge is to convert algorithmic design code into the AMI format. An automated AMI model generation flow is needed to shorten the model development cycle. Xuliang defined Electronic System Level (ESL) design as a methodology that focuses on the higher abstraction level concerns first and foremost. He showed examples of SerDes modeling using the ESL flow. FIR filter models should support arbitrary sampling rates. A generic model library speeds up the process, but for customized IP, you must still bring in math code or C++ code. Simulation results for an Rx model at SATA 3.0 (6 Gb/s) and 10-Gb Ethernet speeds were shown. An AMI model correlation study looked at transistor simulation and measurements versus the AMI model. The correlation results looked very good.

One question was if the AMI Reserved Parameters could be used in all channel simulators. The response was that yes, this is the intention.

SPICE SUBCIRCUIT SUPPORT FOR SERIAL LINK CHANNEL DESIGN USING IBIS [EXTERNAL MODEL]

Xiaoqing Dong*, Zhangmin Zhong**#, Ken Willis**## (*Huawei Technologies and **Sigrity, #China and ##USA)

Xiaoqing reviewed existing solutions for serial link IBIS circuit models. Most models use SPICE-based subcircuits with no standards for use of the netlist in EDA tools. A SPICE-based IO circuit model can easily represent the actual IO structure such as a pullup resistor with pulldown current source for CML. SPICE-based models also incorporate hookups for non-ideal power connections, and on-chip parasitics are easily included. The IBIS [External Model] keyword can be used to reference an external file written in one of the supported languages containing an arbitrary circuit definition. Examples were shown of using SPICE models with [External Model] for both a Tx and Rx circuit. With use of the [External Model] keyword for support of SPICE-based IO models, [Pulldown], [Pullup], [POWER Clamp] and [GND Clamp] data is not required.

EXTENDING/LEVERAGING IBIS CONSTRUCTS TO MODEL HIGH-SPEED I/O'S AND PACKAGES USING AMI, SPICE, AND S-PARAMETERS

John Lin*, Feras Al-Hawari**##, Taranjit Kukal**# and Ambrish Varma**## (*Flextronics, China and **Cadence Design Systems, #India and ##USA)

Dr. Wenliang Dai of Cadence delivered the presentation. With current IBIS constructs, RDL

and/or pin parasitic are lumped into pin R/L/C values. At high frequencies, IO buffers could have portions that need to be modeled using SPICE files such as On-die termination with frequency dependence. Multiple SPICE subcircuits could be used to model different process corners, buffer configurations or dynamic ODT. There are many limitations to current inclusion of SPICE subcircuits with [External Model]. [External Model] could be leveraged to support S-parameter package modeling. Long term, IBIS could have keywords to support S-parameters under the [Package] section to provide port mapping and prompt SI tools to ignore RLC values. An example was shown of using [External Model] to include an S-parameter package model. Package RLC values were zeroed out when doing this to avoid double-counting. Wenliang proposed extending [External Model] to point to SPICE sub-circuits that augment V-I and V-t data for complete characterization of the IO buffer. [External Model] would also be extended to allow dynamic switching of sub-circuits for corners and parametric variations. AMI models should also work in conjunction with [External Model].

IBIS-ISS: WHAT IS IT AND WHAT IT MEANS TO YOU

Michael Mirmak (Intel Corporation, USA)

Michael noted that the problem with SPICE model portability is that a standard SPICE does not exist. IBIS-ISS (Interconnect SPICE Subcircuits) establishes an industry standard baseline for interconnect modeling in SPICE. It defines a limited set of common, basic elements useful for SI interconnect modeling. It is based on documents and concepts donated by Synopsys as seen in Synopsys HSPICE. IBIS-ISS was developed with the SI community through the IBIS Interconnect task group. IBIS-ISS supports fundamental circuit elements, subcircuit definitions and instantiation and some other basic commands, but no engine commands, no active device support and no field solver.

IBIS-ISS consists entirely of subcircuits, so it does not define netlists. All parameters are local and passed explicitly. Multiple files are supported. Good SPICE habits will make IBIS-ISS adoption and use easier. Michael listed several IBIS-ISS rules to follow. Draft 0.7 is now in review and a parser is under consideration. Michael encouraged questions and comments.

A question was asked about whether the parser would be developed as a standalone executable or as part of ibischk. Also, would there be a licensing fee for the code. Michael responded that the parser is planned to be standalone, and as such would have a licensing fee to pay for development costs.

MODELING METHODS FOR COMPLEX S-PARAMETERS IN TOUCHSTONE 2.0

Jinku Guan and Shunlin Zhu (ZTE Corporation, China)

Jinku noted that for crosstalk analysis of connectors, multi-port S-parameters are required, such as a 28-port model in the case shown. He showed some advantages to the new Touchstone 2.0 specification such as no restrictions on the number of data pairs on a line. VNAs with less than 4 ports are very common. An s4p file can be created using a 2-port VNA with 6 measurements. A 28-port S-parameter can be created with 91 measurements using a 4-port VNA. MATLAB was used to convert the 91 .s4p measurement files into a .s28p file. Lab correlation was performed using the .s28p file to model a complete channel. The correlation looked at far-end crosstalk in time and frequency domain and near-end crosstalk in time and frequency domain. Jinku proposed a [Combine Information] keyword for Touchstone to allow for this type of conversion, such as from many .s4p measurements into a single .s28p

measurement Touchstone file.

MODEL CONNECTION PROTOCOL EXTENSIONS FOR MIXED SIGNAL SIP

Taranjit Kukal*#, Wenliang Dai*##, Brad Brim** and Eiji Fujine*** (*Cadence Design Systems, #India, ##China, **Sigrity, USA and ***Fujitsu VLSI Limited, Japan)

Wenliang described how chip/package/board connections can have 100s to 1000s of physical connections, but not all electrical nodes can have per-pin resolution. A method is needed to group pins and auto-connect models across the chip/package/board boundaries. Model Connection Protocol (MCP) establishes pin grouping and mapping of physical to electrical nodes. MCP extensions can be used for mixed-signal System-in-Package (SiP) power delivery analysis. Connecting two disparately pin-grouped models is possible by choosing to short together electrical nodes that have overlapping pin domains. Support for modules is needed in MCP as a category for structures drawing power within the package such as RF modules and metal passive structures. Connections by reference designator instead of x-y location are another recommended extension to existing MCP. An optional column showing connection by REFDES makes for easy mapping for mixed-signal modules and pre-layout analysis.

CONCLUDING ITEMS

Michael Mirmak thanked all the co-sponsors who made the event possible. He also thanked the presenters for the excellent presentations and Bob Ross for help in organizing the event. The meeting adjourned at approximately 4:40 PM.

NEXT MEETING

The next IBIS Open Forum summits will be held November 12, 2010 in Taipei, Taiwan and November 15, 2010 in Tokyo, Japan. The next IBIS Open Forum teleconference will be held November 19, 2010 from 8:00 to 10:00 AM US Pacific Standard Time. A vote on BIRD113 is scheduled.

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NOTES

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This meeting was conducted in accordance with the GEIA Legal Guides and GEIA Manual of Organization and Procedure.

The following e-mail addresses are used:

majordomo@eda.org

In the body, for the IBIS Open Forum Reflector:
subscribe ibis <your e-mail address>

In the body, for the IBIS Users' Group Reflector:
subscribe ibis-users <your e-mail address>

Help and other commands:
help

ibis-request@eda.org

To join, change, or drop from either or both:
IBIS Open Forum Reflector (ibis@eda.org)
IBIS Users' Group Reflector (ibis-users@eda.org)
State your request.

ibis-info@eda.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the EIA-IBIS Open Forum as a full Member.

ibis@eda.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/
http://www.eda.org/ibis/bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/
http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eigroup.org/ibis/ibis.htm

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

IBIS CURRENT MEMBER VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	September 10, 2010	October 1, 2010	October 22, 2010	November 9, 2010
Advanced Micro Devices	Producer	Inactive	X	X	-	-
Agilent Technologies	User	Active	-	-	X	X
Ansys	User	Inactive	-	-	-	X
Apple Computer	User	Inactive	-	-	-	-
Applied Simulation Technology	User	Inactive	-	-	-	-
ARM	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Active	X	-	X	X
Cisco Systems	User	Active	X	X	X	-
Ericsson	Producer	Active	X	-	X	X
Freescale	Producer	Inactive	-	-	-	-
Green Streak Programs	General Interest	Inactive	-	-	-	-
Huawei Technologies	Producer	Inactive	-	-	-	X
Hitachi ULSI Systems	Producer	Inactive	-	-	-	-
IBM	Producer	Active	X	X	X	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	X	X	X
IO Methodology	User	Active	X	X	-	X
LSI	Producer	Active	X	X	X	-
Mentor Graphics	User	Active	X	X	X	X
Micron Technology	Producer	Active	X	X	X	X
Nokia Siemens Networks	Producer	Active	X	-	X	-
Samtec	Producer	Inactive	-	-	-	-
Signal Integrity Software	User	Active	X	X	X	-
Sigrity	User	Inactive	-	-	-	X
Synopsys	User	Inactive	-	-	-	X
Teraspeed Consulting	General Interest	Active	X	X	X	X
Texas Instruments	Producer	Inactive	X	-	-	-
Toshiba	Producer	Inactive	-	-	-	-
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	-	-	X
Zuken	User	Inactive	-	-	-	-

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH TECHAMERICA BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
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- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.