# IBIS Open Forum Minutes

Meeting Date: **November 4, 2009**
Meeting Location: **Shanghai, P. R. China**

**VOTING MEMBERS AND 2009 PARTICIPANTS**

| | |
|---|---|
| Actel | (Prabhu Mohan) |
| Agilent | Brian Andresen, Radek Biernacki, Saliou Dieye, Yutao Hu, Fangyi Rao, Xuliang Yuan* |
| AMD | Nam Nguyen |
| Ansoft Corporation | Steve Pytel, Chris Eric*, Dan Hou*, Baolong Li*, Jack Qiu*, Davis Yan* |
| Apple Computer | (Matt Herndon) |
| Applied Simulation Technology | (Fred Balistreri) |
| ARM | V. Muniswara Reddy |
| Cadence Design Systems | Terry Jernberg, Ambrish Varma, Aileen Chen*, Lanbing Chen*, Wenliang Dai*, Fenghua Gao*, Feng Li*, Ping Liu*, Yubao Meng*, Jian (John) Peng*, Qian (Candy) Shen*, Muker Wang*, Yifong Wen*, Jun Wu*, Zhi (Benny) Yan*, Wayne Zhang*, Wenjiang Zhang*, Qi (Alex) Zhao* |
| Cisco Systems | Luis Boluna, Tram Bui, Bill Chen, Syed Huq, Mike LaBonte, Pedo Miran, Huyen Pham, [AbdulRahman (Abbey) Rafiq], Ashwin Vasudevan, Zhiping Yang, Guan (Greg) Fu*, Jin (Leo) Hu*, Chunhai Li*, Weifeng Shu*, Xinghai Tang* |
| Ericsson | Anders Ekholm* |
| Green Streak Programs | Lynne Green |
| Huawei Technologies | Xiaoqing Dong, Chunxing Huang, Guan Tao, Yu Chen*, Zengzing Hu*, Chun Huang*, Jun Li*, Han Li*, Jinjun Li*, Benguo Lin*, Bo Liu*, Shuyao (Charles) Liu*, Longfang Lu*, Luyu Ma*, Huang Peng*, Lin Qiang*, Kaler Ren*, Minghua Wu*, Jianhong Xiang*, Hang Yan*, Xubo Ye*, Hongcheng Yin*, Xuequan (Tony) Yu*, Cheng Zhang*, Gezi Zhang*, Yi Zhao*, Yi Zhou* |
| Hitachi ULSI Systems | (Kazuyoshi Shoji) |
| IBM | Adge Hawes |
| Infineon Technologies AG | (Christian Sporrer) |
| Intel Corporation | Myoung J. Choi, Michael Mirmak, Vishram Pandit, Jon Powell, Sirisha Prayaga, Lili Deng*, Leo Fang*, Haifeng (Bill) Gong*, Fanghui Li*, Jenny Li*, Wenjie Mao*, Yiunglei Ren*, Yang Wu*, Maoxin Yin*, Xinjun Zhang* |
| IO Methodology | Li (Kathy) Chen*, Lance Wang*, [Zhi (Benny) Yan] |
| LSI | Brian Burdick |

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|---|---|
| Mentor Graphics | Weston Beal, Vladimir Dmitriev-Zdorov, Zhen Mu, Arpad Muranyi |
| Micron Technology | Randy Wolff |
| Nokia Siemens Networks GmbH | Eckhard Lenski |
| Samtec | (Corey Kimble) |
| Signal Integrity Software | Barry Katz, Walter Katz, Todd Westerhoff |
| Sigrity | Brad Brim, Sam Chitwood, Raymond Chen*, Jiangsong Hu*, Li Li*, Xianfeng Li*, Lily Lou*, Zhangmin Zhong* |
| Synopsys | Ted Mido, Xuefeng Chen*, Wenyun Gu*, Jinghua Huang*, Bo Liu*, Qin (Kitty) Zhang* |
| Teraspeed Consulting Group | Bob Ross* |
| Toshiba | (Yasumasa Kondo) |
| Xilinx | [David Banas] |
| ZTE | Xiaolin Chen*, Yanbin Chen*, Jinku Guan*, Mai Hu*, Nan Jiang*, Fei Lu*, Xiaorong Lu*, Xianyu Meng*, Junwei Zhang*, Shunlin Zhu* |
| Zuken | Michael Schaeder, Ralf Bruening |

**OTHER PARTICIPANTS IN 2009**

| | |
|---|---|
| 3M | Kylin Chen*, Shiang Yao* |
| AET | Mikio Kiyono |
| Altera | Hui Fu |
| Apache | Yu Lin, Junyong Deng*, Shulong Wu* |
| ATE | Nob Tanak, Kenny Suga |
| Bayside Design | Stephen Coe, Elliot Nahas |
| Celestica | Fajiang Liu*, Cao Wang*, David Wu*, Baoshu Xu*, Fei Xue*, Van Zhu* |
| Circuit Spectrum | Zaven Tashjian |
| CST | Antonio Ciccomancini, Martin Schauem |
| Curtiss-Wright Embedded Computing | J. Phillips |
| Cybernet Systems | Golden Qian* |
| EM Integrity | Guy de Burgh |
| EMC Corporation | Mingchang Wang*, Vincent Yan* |
| Exar | Helen Nguyen |
| Freescale | Jon Burnett, Om Mandhama, Jesse Qin* |
| H3C | Huanyang Chen*, Xiaoqun Li* |
| Hua Symantec | Senliang Han* |
| ICT Solutions | Steven Wong |
| Interactive Devices Technology (IDT) | Zhiguang (Andy) Li* |
| IdemWorks | Michelangelo Bandinu |
| Juniper | Kevin Ko |
| Kineret Design | Ricardo Teliuteuesh |

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|---|---|
| LeCroy Corporation | Weidong (Derek) Hu*, Scott Zhang* |
| Leventhal Design & Communications | Roy Leventhal |
| Marvell | Mingzhen (Jane) Liu*, Fang Lv*, Yuyang Wang* |
| Maxim Integrated Products | Ron Olisar |
| Mindspeed Technologies | Bobby Alkay |
| NetLogic Microsystems | Eric Hsu |
| Politecnico di Torino | Igor Stievano |
| Sanmina SCI | Vladimir Drivanenko |
| Sedona International | Joe Socha |
| Shanghai ITG Information Technology | Rongsheng Yuan* |
| Siemens | Manfred Maurer |
| Signal Consulting Group | Timothy Coyle, Nicole Mitchell |
| Simberian | Yuriy Shlepnev |
| TechAmerica (GEIA) | (Chris Denham) |
| Texas Instruments | Pavani Jella |
| Vendor Chain International | Jing Lou* |
| Xsigo Systems | Robert Badel |
| Independent | Ian Dodd |

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

**UPCOMING MEETINGS**

The bridge numbers for future IBIS teleconferences are as follows:

| Date | Meeting Number | Meeting Password |
|---|---|---|
| November 6, 2009 | IBIS Japan Summit (Japan) | No teleconference |
| November 20, 2009 | 208 910 728 | IBIS |

For teleconference dial-in information, use the password at the following website:
https://cisco.webex.com/cisco/j.php?J=208910728

All teleconference meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

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**WELCOME AND KEYNOTE COMMENTS**

The IBIS Open Forum summit was held in Shanghai, P.R. China at the Four Points Hotel in the Pudong district. About 112 people representing 25 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda.org/pub/ibis/summits/nov09a/

Jinjun Li of Huawei Technologies began the meeting shortly after 9 AM. Jinjun welcomed the participants to the fifth IBIS summit and expressed appreciation to the IBIS Committee and sponsors for holding the event.

Bob Ross also welcomed everyone to the Asian IBIS Summit and noted that the meeting will cover several IBIS topics. The IBIS committee wants to learn the concerns of China and other regions of the world. Over the years the summit has accumulated 12 co-sponsors to make the meeting possible, and pointed to the backdrop showing the logos of Agilent Technologies, Ansoft, Cadence Design Systems, Cybernet Systems, Huawei Technologies, Intel Corporation, IO Methodology, Mentor Graphics, SiSoft, Sigrity, Synopsys and ZTE Corporation.

Bob introduced Lance Wang, IBIS Vice Chair who would conduct most of the meeting and Anders Ekholm, IBIS Model Librarian. Bob also introduced two other international participants. He looked forward to a productive meeting.

**RECENT IBIS ACTIVITIES**

Bob Ross (Teraspeed Consulting Group, USA)

Bob Ross showed the new IBIS logo and the list of new IBIS officers, most who have been to the Asian IBIS summits. He thanked Michael Mirmak, past Chair for his six years of service. He showed the active task groups and noted that IBIS has been active since 1993 with regular meetings.

IBIS Version 5.0 was released in 2008, and Bob illustrated the ibischk5 (available the previous week) new flags for the algorithmic modeling interface (-ami) and numbered errors and warnings (-numbered). Bob also noted that Touchstone Version 2.0 was approved and also that he just received an alpha release of the tschk2 parser. The Quality Specification Version 2.0 was approved the previous week. While advances on the Algorithmic Modeling Interface are continuing, the Interconnect Spice Subcircuit project is temporarily on hold.

Overall work is continuing on IBIS advances, and the IBIS committee remains very active, attracts top talent, and has active international participation.

**C_COMP EXTRACTION METHODS FOR HIGH-SPEED I/O BUFFERS**

Lance Wang (IO Methodology, USA)

Lance Wang introduced several methods to extract C_comp. They were the time-domain ramp

up/down approach, the resonant frequency approach, and a direct .AC extraction of the impedance. While the first two methods can show voltage dependencies, the .AC approach can also show a C_comp dependency on frequency. Lance used the last approach for the remainder of the study.

In a test setup, Lance extracted the individual C_comp values for both clamps and the pullup and pulldown transistors. He presented several plots showing voltage and frequency dependences for driving and non-driving modes.

The C_comp values for clamps showed minor variation, and a high frequency extraction would be reasonable. More variation existed for the C_comp values associated with the pullup and pulldown transistors.

Lance provided some guidance that the extraction frequency should be related to the [Ramp] information (Foutput = 1/(dt_r + dt_f). The voltage settings could be centered around actual operation. He also concluded that the IBIS specification could be improved with separate driving and non-driving C_comp values and with separate C_comps for different DC values depending on the application.

**IBIS QUALITY REVIEW, A STATUS REVIEW OF THE IBIS QUALITY SPECIFICATION**

Anders Ekholm* and Mike LaBonte** (*Ericsson, Sweden and **Cisco Systems, USA)

Anders Ekholm provided the basic meeting information for the Quality Task Group and how to subscribe to its reflector. He gave a brief history from its beginning in 2002, Version 1.0 release in 2004, and the recent release of Version 2.0 on the previous Friday, October 30, 2009.

Anders outlined the levels of the IBIS Quality Specification Version 1.0 from IQ0 through IQ3. He noted its issues, particularly with level 0 meaning that the IBIS model passed ibischk. The IBIS Quality Specification Version 2.0 adjusted the levels from IQ0 though IQ4 and also added some modifiers: S, M, X, and G. The new levels are:

IQ0 - not checked
IQ1 - passes ibischk
IQ2 - suitable for waveform simulations
IQ3 - suitable for timing analysis
IQ4 - suitable for power analysis (defined but no checks yet)

And modifiers:

S - simulation correlated
M - measurement correlated
X - exceptions
G - has golden waveforms

He showed some sample tests related to each level. The previous correlation section will be moved to refer to the IBIS Accuracy Handbook. The committee produced many drafts and will produce a few BUG reports related to some of the checks. Anders noted that the active

members included systems companies, users and semiconductor company developers of IBIS models. He expects adoption by IC vendors and librarians in systems companies and quality checks to be included in modeling tools.

**HUAWEI'S IBIS MODEL QUALITY SPECIFICATION AND TECHNOLOGY**

Jun Li (Huawei Technologies, China)

Jun Li reported on Huawei's quality process, which follows the IBIS Quality Specification, but in more detail. It also has PCB based correlation and the following model levels:

Copper
Silver
Golden1 (for signal reflection)
Golden2 (for timing)
Golden3 (for SI+PI co-design)

The Quality report contains (1) Huawei's model quality checklist, (2) waveform comparison, and (3) electrical specifications of simulation versus measurement.

The model quality checklist is similar to the IBIS Quality Specification checklist, but with pass/fail buttons for each item. The waveform comparison compared simulation and measurement waveforms for fast, typical and slow cases for a 50 ohm PCB trace system. The electrical specification provided waveforms and correlation figures of merit.

Jun then showed the IBIS model correlation process. It compares simulation and measurement waveforms through interconnect channels and then adjusts the IBIS model where needed, after any data issues with IBIS models are resolved. The package values are checked against entered values using TDR measurements on the physical device. The strengths and speeds are adjusted to match waveform reflection properties. In addition, a behavioral current source is added as a macro-model to deal with SSN issues. With this adjustment methodology, the overlaying comparisons are improved significantly. Jun showed one case where the correlation improved from 35% mismatch to only 5% mismatch over a full cycle.

In response to one question, Jun responded that the socket is included in the correlation. For another question, Jun noted that the actual circuit board traces are used for realistic comparisons. Huawei tries its best to minimize the differences between the physical path and its characterization for simulation comparisons.

**THE USE OF OPTIMIZATION IN SIGNAL INTEGRITY PERFORMANCE CENTRIC HIGH SPEED DIGITAL DESIGN FLOW**

Brahim Bensalem**#, Lihau Wang*#, Sanjeev Gupta*#, and Xuliang Yuan*##, (*Agilent Technologies and **Intel Corporation, #USA and ##China)

Xuliang Yuan introduced an eye-centric design flow and showed some commonly used eye diagram measurements (level 1 & level 0, rise/fall time, opening, width, height, amplitude, and peak to peak & RMS jitter). Histograms can be used for binning of data, and the eye delay calculation is needed for automatic eye crossing detection. Eye probes can be used to make the measurements. Xuliang then presented some measurement examples.

Xuliang provided advantages of optimization over parameter sweeping to improve designs. Certain physical parameters can be optimized based on eye diagram measurements to set optimization goals. He showed some examples and indicated that much of the process can be automated.

The method can be improved to include IBIS model optimization such as for drive strength and on-die termination selection as part of the process.

**BEHAVIORAL MODEL APPLICATION IN HSS SIMULATION**

Nan Jiang, Zhiwei Yang, and Shunlin Zhu (ZTE Corporation, China)

Nan Jiang indicated that High Speed Serial (HSS) link signal integrity is becoming more important for Ser-Des devices. Behavioral-level models are needed for reasonable analysis times. Nan stated the advantages and disadvantages of SPICE, IBIS, and macro model based IBIS models.

Nan then presented an example for applying an AMI model as another behavioral approach. This example showed that the model can be tuned to get a good eye-diagram result.

He then introduced an IBIS-AMS model example based on Verilog-AMS. It also produced a good eye diagram through setting coefficients for DFE and FFE and with pre/de-emphasis adjustments.

Behavioral models can be supplied by vendors for higher data rate designs since the SPICE model is not available. However, better model availability is needed. Nan discussed the need and set some expectations for better vendor support for behavioral models including getting more advanced (Version 5.0) IBIS models.

**IBIS-AMI FOR IBM HSS15 CORE TECHNOLOGY**

Chris Herrick (Ansoft, USA)

Chris Herrick gave a brief overview of IBIS AMI and showed how Tx and Rx models can be used with a linear (4-port) channel. A channel impulse response is generated for full scale transient analysis. A random bit generator and piece-wise linear source can provide the signals to drive a user's TX library. This is convolved with the channel impulse response. Contributions from aggressors can be added linearly. RX libraries can also be added to the simulation, and clock ticks can be generated automatically for post processing.

Chris outlined some existing challenges including no way to sweep the parameters, and different parameter sets from different vendors. Vendor-specific design kits provide a way to add such features.

A proprietary simulator supports IBM's HSS cores and is a current standard for evaluating channels with IBM ICs. Chris demonstrated that IBIS-AMI can produce identical results and showed some applications that can be automated such as for sweeping taps and for sweeping the cursor lag. He concluded that IBIS-AMI is a promising means of modeling transmit and receiver equalization, and that design kits can be developed to make IBIS-AMI adoption easier.

**RECENT DEVELOPMENT OF IBIS AND RELATED EDA TECHNOLOGIES**

Jinsong Hu* and Raymond Y. Chen** (Sigrity, *China and **USA)

Jinsong Hu gave a very brief overview of IBIS Version 5.0 and also of Touchstone Version 2.0. He then introduced some IBIS-AMI key concepts, dividing the flow into the Tx algorithmic part, the analog channel, and the Rx algorithmic part.

Jinsong then discussed several needed advanced features. They were (1) cascaded AMI for more flexible modeling and debugging, (2) crosstalk aware models allowing the filter coefficients of the main channel to be used with adjacent channels for crosstalk analysis, (3) some advanced customizable function blocks for real world devices, (4) hybrid support allowing a mixture of models, and (5) adding AMI models to power delivery system nets.

He then switched to S-parameter considerations by first introducing existing IBIS capabilities for the IBIS PKG model and the IBIS EBD model. Jinsong then outlined the features of the recently introduced Touchstone Version 2.0 specification for S-parameters.

For existing applications the data file can be huge. A pole/zero format can be more compact, and Jinsong then introduced a proprietary binary format which combines pole/zero efficiency with binary encoding. This will be proposed for consideration by IBIS.

**SPARSE MATRIX MAPPING IN FUTURE TOUCHSTONE 2.1**

Bob Ross (Teraspeed Consulting Group, USA)

Bob Ross first gave a brief overview of the recently released Touchstone Version 2.0 history and 13 IBIS-like keywords and block arrangement. He also showed the more rigid Touchstone 1.0 fixed format structure that contains less direct information about its content.

Bob then introduced the sparse matrix mapping concept with a 2-row, 3-column physically symmetrical connector. First, he showed the existing .pkg and .ebd coupled package concept with unique coupling from pin 1 to global ground, to the other pins 2 to 6 and the thru path to the other side. This is the standard LRGC model structure, as used for [Define Package Model]. It documents only the upper triangle coupling relationships since for passive networks, the lower triangle are identical about the matrix diagonal.

He then used the same example to demonstrate the [Sparse Matrix Mapping] keyword under discussion for Touchstone Version 2.1. Because of the physical symmetry assumption, the amount of data can be reduced significantly in a Touchstone file. Many of the columns that are required under [Network Data] are identical. So, an indirect method mapping all the identical columns (designated by their row,column index-pairs) into a single column of complex data entries (data-pairs) under [Network Data] can be done using integer-labels, an integer that references the specific column storing the complex data information for each frequency.

The example of the 6-pin connector corresponds to a fully filled out 12-port file (the port numbers 1-6 were chosen for side 1, and port numbers 7-12 were chosen for side 2 so that the labeling would be identified with the port to which the coupling occurs. In general there is no restriction to the port labeling. The corresponding N-port would require 144 complex entries per

frequency under [Network Data]. But by identifying the unique coupling on side 1 (including to global ground, and the thru path to side 2), only 7 unique entries are needed. An additional 5 entries are needed for the unique coupling from side 1 to the remaining 5 ports of side 2, but some users might need to include these entries. These effects are currently neglected in the standard .pkg and .ebd formats.

Bob used one coupling (port 1 to 5 on side 1) and identified the 16 identical coupling relationships if physical symmetry is assumed. Since the reciprocal relationships are included, this set can be reduced to 8 upper or 8 lower relationships by making use of the [Matrix Format] keyword and choices Upper or Lower.

With similar reductions for all the coupling relationships, Bob showed the syntax for a complete example (with only 7 integer-labels and only 7 columns of complex data-pairs. (If all the unique coupling relationships were included, 12 columns would be needed.) Only 7 (or 12) columns of complex data are needed for an N-port instead of up to 144 columns.

This set of unique coupling relationships can be used to document the coupling to the adjacent two physical columns on either side and then expanded to model larger connectors with many more physical columns. The relationships beyond two columns are assumed “0” and omitted. So Bob showed tables for 6-pin, 40-pin, and 200-pin connectors and the number of index-pairs needed for each integer-label. He also showed a bank of isolated 40 pin connector blocks that a manufacturer might design for expandable configurations. In all cases the number of data-pairs is 7 (or 12), and this amount of data is less than a traditional 3-port description.

The exact details are still being discussed. All other keywords are compatible with this approach including differential representations with [Mixed-Mode Order].

**USING S-PARAMETERS FOR ACCURATE SIMULATON**

Baolong Li* and Greg Pitner** (Ansoft, *China and **USA)

Baolong Li provided a mathematical foundation for Fourier transform methods. Two approximations exist in real applications: finite bandwidth and discrete data points. A finite bandwidth corresponds to an ideal rectangular window (1 inside, 0 outside the bandwidth), but such a window produces oscillations. Baolong introduced several other window functions (Hamming, Hanning, Blackman, Welch, and Bartlett) and showed their trade-offs between edge speed and oscillation.

Baolong noted that rectangular windows are non-causal. So, increasing the bandwidth improves the edge response and reduces the overshoot.

For guidance with discrete data, these relationships are recommended: Tstep = 1/(2*Fmax) and Tmax = 1/(2*Fstep).

For parallel signals, the frequency step should be denser than 1/T. For serial signals, the frequency step should be denser then 1/(n*UI).

The Fknee is limited to 5/Tr to 10/Tr for broadband channel characterization, not just 1/(2Tr) for standard transmission line modeling.

**SUBCKT PACKAGE MODEL IN IBIS**

Wenliang Dai (Cadence Design Systems, China)

Wenliang Dai gave an overview of the existing IBIS package model options: (1) simplified RLC, (2) segmented/forked RLC, and (3) coupled RLC matrix values. Currently, field solvers can extract coupled package model SPICE subcircuits and Touchstone S-parameter models.

Because of current requirements and the need to consider decoupling capacitors for power and SSN analysis, the subckt and S-parameter models are needed along with pin-port mappings.

Wenliang showed the existing [Define Package Model] structure and then proposed enhancing it with the following keywords: [Subckt Package Model], [Pin-Node Mapping]/[End Pin-Node Mapping], [Subckt Model Data]/[End Subckt Model Data]. He presented more syntactical details and concluded that such a structure can support accurate Power/SSN analysis, bring in SPICE or S-parameter data, and work with IC-Package-Board co-design applications.

**SYSTEM SIMULATION AUTOMATION - MODEL CONNECTION REVIEW**

Zhangmin Zhong*, Brad Brim**, and Raymond Y. Chen** (Sigrity, *China and **USA)

Zhangmin Zhong noted that no standards exist for dealing with chip/package/board system designs consisting of hundreds or thousands of physical connections (such as pins). One issue is to connect a large number of pins from one model format to another. IBIS has pin connection methods, but does not provide return path power/ground information. Also IBIS does not provide die (chip) side information.

Zhangmin outlined some requirements including arbitrarily pin-grouped models and automated connection among models in EDA tools. Several vendor-specific model protocols exist and are implemented by comment lines in “headers”.

Zhangmin introduced the Sigrity Model Connection Protocol (MCP). It includes pinName, modelNodeName, netName and x and y positions for physical pins. It can group [Power Nets], [Ground Nets] and [Signal Nets]. It has IBIS-like keywords and supports [Structure Type] and [Connecton Type] choices of {DIE | PKG | PCB}. The syntax is implemented as comment lines in the header. SPICE and Touchstone files can be supported.

Several examples were given including SPICE circuit listings with MCP headers as comment lines in the header. Zhangmin concluded that a standard model connection protocol should be defined (by IBIS) to better serve industry than the proprietary protocols currently being used.

**CONCLUDING ITEMS**

Bob Ross thanked Coco Xu (Cadence Design Systems) and Aileen Chen for helping setup the meeting. Bob thanked the presenters for excellent presentations covering several important IBIS topics, the sponsors, and Lance Wang for chairing the meeting. The meeting adjourned at approximately 5:10 PM.

**NEXT MEETING**

The next IBIS Open Forum Meeting is the Asian IBIS Summit (Japan) on November 6, 2009. There will be no teleconference access. The next IBIS Open Forum teleconference will be held November 20, 2009 from 8:00 to 10:00 AM US Pacific Standard Time.

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**NOTES**

IBIS CHAIR: Bob Ross (503) 246-8048, Fax: (503) 239-4400
bob@teraspeed.com
Staff Scientist, Teraspeed Consulting Group
10238 SW Lancaster Road
Portland, OR 97219

VICE CHAIR: Lance Wang (978) 633-3388
lwang@iometh.com
President / CEO, IO Methodology, Inc.
PO Box 2099
Acton, MA 01720

SECRETARY: Randy Wolff (208) 363-1764, Fax: (208) 368-3475
rrwolff@micron.com
SI Modeling Manager, Micron Technology, Inc.
8000 S. Federal Way
Mail Stop: 01-711
Boise, ID 83707-0006

LIBRARIAN: Anders Ekholm (46) 10 714 27 58, Fax: (46) 8 757 23 40
ibis-librarian@eda.org
Digital Modules Design, PDU Base Stations, Ericsson AB
BU Network
Färögatan 6
164 80 Stockholm, Sweden

WEBMASTER: Syed Huq (408) 525-3399, Fax: (408) 526-5504
huqs@cisco.com
Manager, Hardware Engineering, Cisco Systems
170 West Tasman Drive
San Jose, CA 95134-1706

POSTMASTER: Mike LaBonte (978) 936-2147
milabont@cisco.com
Signal Integrity Engineer, Cisco Systems
Mail Stop BXB01/1/
1414 Massachusetts Ave
Boxborough, MA 01719

This meeting was conducted in accordance with the GEIA Legal Guides and GEIA Manual of Organization and Procedure.

The following e-mail addresses are used:

majordomo@eda.org

In the body, for the IBIS Open Forum Reflector:
subscribe ibis <your e-mail address>

In the body, for the IBIS Users' Group Reflector:
subscribe ibis-users <your e-mail address>

Help and other commands:
help

ibis-request@eda.org

To join, change, or drop from either or both:
IBIS Open Forum Reflector (ibis@eda.org)
IBIS Users' Group Reflector (ibis-users@eda.org)
State your request.

ibis-info@eda.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the EIA-IBIS Open Forum as a full Member.

ibis@eda.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/
http://www.eda.org/ibis/bugs/ibischk/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eigroup.org/ibis/ibis.htm

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

## IBIS CURRENT MEMBER VOTING STATUS

### I/O Buffer Information Specification Committee (IBIS)

| Organization | Interest Category | Standards Ballot Voting Status | September 18, 2009 | October 9, 2009 | October 30, 2009 | November 4, 2009 |
|---|---|---|---|---|---|---|
| Actel | Producer | Inactive | | | | |
| Advanced Micro Devices | Producer | Inactive | | | | |
| Agilent Technologies | User | Inactive | | | | √ |
| Ansoft | User | Inactive | | | | √ |
| Apple Computer | User | Inactive | | | | |
| Applied Simulation Technology | User | Inactive | | | | |
| ARM | Producer | Inactive | | | | |
| Cadence Design Systems | User | Active | | √ | √ | √ |
| Cisco Systems | User | Active | √ | √ | √ | √ |
| Ericsson | Producer | Active | √ | √ | √ | √ |
| Green Streak Programs | General Interest | Inactive | | | | |
| Hitachi ULSI Systems | Producer | Inactive | | | | |
| Huawei Technologies | Producer | Inactive | | | | √ |
| IBM | Producer | Inactive | | | √ | |
| Infineon Technologies AG | Producer | Inactive | | | | |
| Intel Corp. | Producer | Active | √ | √ | | √ |
| IO Methodology | User | Active | √ | √ | | √ |
| LSI | Producer | Active | √ | √ | √ | |
| Mentor Graphics | User | Inactive | √ | √ | | |
| Micron Technology | Producer | Active | √ | √ | √ | |
| Nokia Siemens Networks | Producer | Active | √ | √ | √ | |
| Samtec | Producer | Inactive | | | | |
| Signal Integrity Software | User | Active | √ | √ | √ | |
| Sigrity | User | Inactive | | | | √ |
| Synopsys | User | Inactive | | | | √ |
| Teraspeed Consulting | General Interest | Active | √ | √ | √ | √ |
| Toshiba | Producer | Inactive | | | | |
| Xilinx | Producer | Inactive | | | | |
| ZTE | User | Inactive | | | | √ |
| Zuken | User | Inactive | | | | |

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH GEIA BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
- PRODUCERS - MEMBERS THAT SUPPLY ELECTRONIC EQUIPMENT.
- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.