IBIS Open Forum Summit Minutes

Meeting Date: **April 23, 2009**

VOTING MEMBERS AND 2009 PARTICIPANTS

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Ansoft Corporation	Steve Pytel
Apple Computer	(Matt Herndon)
Applied Simulation Technology	(Fred Balistreri)
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Cadence Design Systems	Terry Jernberg, Ambrish Varma
Cisco Systems	Luis Boluna, Tram Bui, Bill Chen, Syed Huq, Mike LaBonte, Pedo Miran Huyen Pham, AbdulRahman (Abbey) Rafiq, Ashwin Vasudevan, Zhiping Yang
Ericsson	Anders Ekholm*
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Green Streak Programs	Lynne Green
Hitachi ULSI Systems	(Kazuyoshi Shoji)
Huawei Technologies	Xiaoqing Dong, Chunxing Huang, Guan Tao
IBM	Adge Hawes
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Michael Mirmak, Jon Powell, Sirisha Prayaga
LSI	Brian Burdick
Marvell Semiconductor	(Itzik Peleg)
Mentor Graphics	Weston Beal, Vladimir Dmitriev-Zdorov, Zhen Mu, Arpad Muranyi
Micron Technology	Randy Wolff
Nokia Siemens Networks GmbH	Eckhard Lenski*
Samtec	(Corey Kimble)
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Sigrity	Sam Chitwood
Synopsys	Ted Mido
Teraspeed Consulting Group	Bob Ross
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Xilinx	David Banas
ZTE	(Ying Xiong)
Zuken	Michael Schaeder*, Ralf Bruening*

OTHER PARTICIPANTS IN 2009

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Circuit Spectrum	Zaven Tashjian
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IO Methodology	Li (Kathy) Chen, Lance Wang, Zhi (Benny) Yan
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Leventhal Design & Communications	Roy Leventhal
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Mindspeed Technologies	Bobby Alkay
NetLogic Microsystems	Eric Hsu
Politecnico di Torino	Igor Stievano*
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Sedona International	Joe Socha
Siemens	Manfred Maurer*
Signal Consulting Group	Timothy Coyle, Nicole Mitchell
Simberian	Yuriy Shlepnev
Xsigo Systems	Robert Badel
Independent	Ian Dodd

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

Date	Telephone Number	Meeting ID
April 24, 2009	1-866-432-9903	121564807

All meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, press 1 to attend the meeting, then follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

WELCOME AND INTRODUCTIONS

The European IBIS Summit Meeting was held in Nice, France at the Novotel Nice Centre during the Design Automation and Test Exhibition (DATE) conference. About 8 people attended representing 6 companies.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda-stds.org/pub/IBIS/summits/apr09/

Thanks to Eckhard Lenski for supplying the notes used for this set of minutes.

Ralf Bruening hosted the meeting and opened the meeting noting that this is the twelfth IBIS summit in Europe. He thanked the three co-sponsors: Agilent Technologies, Sigrity and Zuken and also the people who keep the spirit of IBIS alive. Ralf continued, that despite the current situation, the European IBIS meeting must continue. Also in the future the users and the model makers must meet to discuss their needs. Ralf mentioned that he had received a lot of cancellations from people from Asia, Germany, Italy and France. He also has a presentation from Sigrity that he might show later, because the presenter was unable to attend the summit. He stated that he had been to the DATE exhibition, and that there was little attendance. He said he would like to add a new item to the agenda to discuss the future of the European IBIS summit. A second item could be a discussion about the AMI modeling feature. Anders Ekholm added that if there is time, he would like to talk about adding new timing analysis parameters to IBIS.

SIZE MATTERS – RECENT EXPERIENCES WITH IBIS FILES

Ralf Bruening and Michael Schaeder, Zuken, Germany

Ralf Bruening started his presentation by telling about the experience from customers that the size of some IBIS files has increased tremendously and that it almost can not be handled. A user who is not working daily with IBIS models is overly challenged; even some [Model Selector]s have up to 50 models. He then talked about the early days of IBIS with just a few I/O models per device and that from time to time the size did grow. But during the last two years, the size of IBIS files is exploding. Files with 70MB including up to 7000 different I/O models appeared. The IBIS parser can handle these big files, although it might take up to 5 minutes for a file to be checked, but some third party tools (especially freeware viewers) have problems with these big files. Some vendors deliver an extra file with a model description, while others are using an almost encrypted model name convention, which is not easy to understand. And there are other models for parts that are even divided by technology or functional block, and the package is delivered as an HSPICE model. So, the user has to do a lot of handwork, which is error prone. Ralf concluded that the handling of IBIS data must be improved and more and more users are asking him for help.

The discussion started with the suggestion to split the IBIS file into different technologies to make it easier to handle, but the drawback would be that now, not all models are in one file. The user wants a ‘push-button’ solution, which is not possible with these huge IBIS files. Another suggestion was a new hierarchy level by making special [Model Selector]s to signal groups. Nowadays user training is almost necessary to help the user to mange these files. Another point is that for the IBIS Quality report a readable file would be difficult to create.

DECODING IBISCHK STATIC VS DYNAMIC WAVEFORMS

Eckhard Lenski, Nokia Siemens Networks, Germany

Eckhard Lenski started with some excerpts from Michael Mirmak's ibischk parser specification. The parser program does syntax checking, looks for parameters exceeding certain limits and contains a lot of more checks. His presentation talks about the mismatch check between static and dynamic waveforms. He showed a normal warning message and showed the I-V and V-t waveforms that the different numbers are coming from. He continued with the remarks that although IBIS check warning messages are printed out with 2 digits, the parser itself is calculating with 3 or more digits of accuracy. He explained what qualifies a mismatch as an error or a warning. He thanked Bob Ross for the discussions. He then showed the difference between a calculation of the errors/warnings with 2 or with 3 significant digits. The calculation with 3 significant digits supplied the correct calculation. In his first example he showed how the modeling of an internal pulldown behavior in the clamping curves will cause discrepancies in the waveform matching. The solution for this kind of problem is to use [Submodel] syntax instead in the non-driving mode. This makes sure that the internal pullup current will no longer be included in the calculation of mismatch. In his second example he asked the question if a mismatch of 25mV should be considered as a big difference. He showed that for some buffers this might the case, and in his example the 25mv turned out to be an error of 10%. The last example was about a driver that did not have any rising or falling V-t waveforms. For buffers with only [Ramp] data, ibischk can not catch any discrepancies. He explained that an easy way of getting the parser to work is to create default waveforms. The information can be either taken from the [Ramp] by extrapolating the ramp dV value to 0-100% or from the static curves by calculating the crossing point with the load lines. By using both methods a difference between the voltage swing of the ramp-method and the static-curve method could be seen. The ibischk message showed this error for the extrapolated ramp. With this approach the [Ramp] dV value could be corrected. For the time value (dt) of the [Ramp], there are now two options. Either the extrapolation of the time value was correct and only the [Ramp] extraction was wrong, or if the [Ramp] dV value is wrong, the [Ramp] dt value has to be changed correspondingly. He pointed out that both options are very risky to use, and that in any case the vendor has to be informed about this mismatch/error. He ended his presentation with the remarks that it is important to use for the static swing calculation the difference, as described in the IBIS specification, between the sum of the [Pulldown] plus [..clamps] and the sum of the [Pullup] plus [..clamps].

A question was asked about how much time it took to find the solution to the problem with the internal pullup and if this timing effort is justified. Eckhard answered that it took more than one day, and that only in the long term view can this be justified. These problems occur more and more often, and with the reducing power supply, the influences of these incorrectly modeled internal pullup behaviors will increase. He also pointed out that the less warnings (and errors) his customers get from the tool and their check procedures for the models, the more confidence they have in these models.

Then Eckhard asked the audience what they were doing with warnings and errors form ibischk. He got the answer that some users are generally ignoring these messages, while others said that warnings do contain valuable information that should be used. Another answer was that some users do not use ibischk at all. Another question was if he had used both models in a simulation and compared the results, and if there had been differences. Eckhard said that he did not compare, but this would an interesting thing to do when he has more time.

The last question was about the [Ramp]-only driver, as both options presented seem to be unreliable. Eckhard answered that a solution was needed at that time very urgently, so he created both models, released them in the library, marked them as default models and told the designer about the problems with the hint of using the model with caution. At the same time he started a request for updated information from the vendor, and as of today, no answer has been received.

THE TOUCHSTONE 2.0 FORMAT FOR INTERCONNECT MODELING

Manfred Maurer, Siemens AG, Germany

Manfred Maurer stated that at the moment there is a renaissance of Touchstone models for two reasons. The channel models are getting more and more complex and not everybody feels comfortable with the new AMI-modeling. He explained that a good channel model is important for SI and PI analysis. He showed a picture of a channel that consists of seven different sections and it is obvious that the influence of the channel is increasing. There are three ways of modeling a channel and all of them have pros and cons. The first is to create for each segment a different model, the second is to use the impulse response and the last is the general approach with Touchstone models. He gave an overview of the advantages and limits of the Touchstone format 1.0, with the biggest advantage being that it is a standard. In the next slide he described in detail the new features of the Touchstone 2.0 format that will contain 'IBIS-like' keywords and mixed mode support. He continued with his experiences of analyzing a high speed SerDes channel with a Touchstone 1.0 model for the cable. The reason for his analysis was to find out whether a cable can be used and up to what length, then which vendor would deliver the better results, and finally if the design itself has to be changed. He pointed out that he was in the lucky situation that in the Touchstone file the pinout was described in the comment section and also the usage of magnitude and angle/phase for the values. This information would be included in Touchstone 2.0 as keywords. He ended his presentation with the statement that he was missing the information about the power delivery system (PDS) necessary to do an SSO analysis. He is looking forward to getting a model in Touchstone 2.0 format to compare the results.

He was asked why the mixed mode data is linked to PDS analysis. Manfred explained that the leakage of the PDS has influence on the differential signal. It was mentioned that a Touchstone 1.0 format would be sufficient to do all the things he mentioned, but only the linkage to mixed mode is missing. One problem might be the excitation of the model, which could be easier with Touchstone 2.0. Also, a translation from differential mode to common mode can be done, but this requires a lot of knowledge. Another problem might be the measurement for the power pins with a 1.0 ohm reference. Everybody agreed that a big advantage of Touchstone 2.0 will be that this format will be IBIS-like and ports will be described.

ENHANCED MPILOG MODEL FOR POWER INTEGRITY ANALYSIS

Antonio Girardi*, Igor Stievano**, Roberto Izzi*, T. Lessio*, Flavio Canavero**, Ivan Maio** and Luca Rigazio**, *Nymonyx and **Politecnico di Torino, Italy

Igor Stievano opened his presentation by stating that his current work is part of a European project in which IC vendors, EDA vendors and universities are involved. He gave a short summary of the history of the Mpilog model and his improvements. He pointed out that the advantage of the model is its application and accuracy for large power supply variations. He showed that, in general, IBIS and Mpilog have the same 2-equation 2-unknown representation,

and that for the usage of the models in PI simulations, you will only have to change two coefficients for dependency of both v(out) and vdd. He explained that the model equations have now also been implemented in SPICE and Verilog-A. He continued with his validation test cases each containing 4 drivers in parallel and each one with a lumped capacitance. For the second test case in addition a transmission line was used. He explained that for the IBIS driver model the results for the power supplies (bouncing) seems to be completely wrong, but that he expects a huge improvement if the features of the gate modulation effects are included. The same is valid for the output signal. The results for the second test case are even worse, which can be explained by the fact that the transmission line adds more stress to the device. He also showed a comparison between the Mpilog and the IBIS model in a statistical error overview. He pointed out that his eye measurements could only be done with a bit stream of 300 bits, but even with this short bit stream, it can be seen that the Mpilog models showed very similar behavior to the reference. He ended his presentation with a comparison of the cpu times used for IBIS and Mpilog models. It looked as if the speedup for IBIS is greater than the one for Mpilog, but the accuracy of the Mpilog model is better than the IBIS model.

It was asked whether he had made any measurements, and Igor answered that he had not yet. He pointed out that, at the moment, two further steps are missing. One will be the implementation of the gate modulation effect and the second one will be measurements. It was asked why the gnd- and the vcc-bounce are so much greater in the IBIS model. Igor said that the power supply is currently implemented in the Mpilog model, which explains its accuracy. The last question was why he had used a simple model for the power supply parasitics, and he pointed out that a network of vdd parasitics will be included in the future.

FIRST EXPERIENCES IN DEALING WITH ICEM (IC EMISSION) MODELS

Ralf Bruening, Zuken, Germany

Ralf Bruening opened his presentation by asking who has ever worked with an ICEM model. No one had. He continued that the demand for ICEM models arises from the lack of IBIS models to model the core switching behavior and that the demand mostly comes from the automotive and aerospace industry. He wondered whether ICEM models could close the gap, as it is very close to SPICE with a large number of elements needed to get the netlist of the core. He said that, together with a vendor, he started an investigation to find out if this large netlist could be reduced in size. He explained that most of the ICEM work is very research oriented, but not development oriented, and that in the model there exist a lot of controlling units for interference. The challenges for modeling are enormous, as there is large granularity and a lot of internal coupling effects. He explained that only a few vendors are supporting ICEM models, and a lot of work is necessary like getting information about the current profile of the die and the coupling between functional blocks. This results in a long SPICE netlist. He pointed out that a reduction process for this large netlist is under development. His experiences showed that correlation is difficult and that he had seen problems in getting this netlist to run at all, depending on the SPICE simulator. For even the one that worked, it took 3 days to finish the simulation. His current challenge is to create a model that has a frequency dependency for the current. For him, it looked as if ICEM is nowadays more used in IC-design rather than for PCB design.

There was a question if ICEM could be understood as a methodology and not as a standard. It looks as if it is more of a methodology on how to get the current flow inside. In his last statement, he pointed out that he also is involved in a project called Parachute, and this is much more a demonstrator to get curves as a result of EMI simulations. At the moment there is still

no good correlation between simulation and measurement.

THE USE OF OPTIMIZATION IN SIGNAL INTEGRITY PERFORMANCE CENTRIC HIGH SPEED DIGITAL DESIGN FLOWS

Saliou Dieye*#, Brahim Bensalem**##, Lihau Wang*## and Sanjeev Gupta*##, *Agilent Technologies and **Intel Corporation, #France and ##USA

Saliou Dieye started the presentation with the comparison between a conventional design flow and the new flow using a so called centric eye design flow. The conventional design flow has the drawback that a lot of simulations have to done with corner and Monte Carlo analysis. Then, the results have to be examined and new parameter settings have to be chosen to set up a new simulation. Sometimes many loops are necessary until the design targets are met. The new method delivered a great reduction in channel design time and the channel is even more robust. He explained that looking at the eye is necessary, where by just looking at the time domain timing signal, it is not clear where the levels for static 0 or 1 are reached, what the rise and fall times are, etc. By using eye diagrams either with 1 or 2 unit intervals (UI), these things can be measured exactly. Another important thing that can be done is statistical calculations of the eye diagram. He showed an example that, with eye binning (slice and dice), another important view on the signal is possible. He continued by showing histogram plots for peak to peak jitter and amplitude height to see the distribution errors for the levels for 0 and 1. He then showed how, by using the binning technique, it is possible to make an eye delay calculation. Also an automated eye crossing detection can be done. He then showed how measurements on an eye level for 0 and 1 can be done by statistical methods. By using eye measurement during the simulation, an optimization will be done at the same time. He pointed out that the difference to a pure (and long) Monte Carlo analysis is the fact that with the centric eye optimized (CEO) process approach, a kind of pre-selection is done, but that the parameters are not varied in a random way. He ended his presentation with a comparison between designs done with or without the CEO process and the difference had been a significant improvement in both eye height and eye width. Furthermore, the result was reached in a very short time of 30 minutes of simulation time.

A question came up if this method can only be used for DDR2 and DDR3 designs, and Saliou answered that this should be possible for all high speed memories where eye diagrams are used and that the examination is on the way.

CLOSING REMARKS

Ralf Bruening said that as the time is now so advanced, there is no more time left for a short view on the interesting presentation from Sigrity. He started with the first adhoc item about the future of the location of the European IBIS summit meeting. There are the possibilities of sticking with DATE or making it independent from DATE and trying to connect to the SPI conference or even going with EMC-COMPO (with the drawback of a two year cycle). He said that SPI seems to be good choice, as its audience is well above 100 attendees. Also, the topics will fit with IBIS. Even some presentations do have great IBIS relevance. The audience agreed and asked Ralf to inform Bob Ross and Michael Mirmak about these plans. Also, Ralf will start investigating with the SPI committee to see if it would be possible to add IBIS as an optional slot at the SPI/conference.

Ralf closed the meeting by saying that this was the first time that the discussions took almost

more time than the presentations itself. He thanked the attendees, and he hopes that next year we will meet under better economic conditions.

NEXT MEETING

The next teleconference will be held April 24, 2009 from 8:00am to 10:00am US Pacific Time.

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NOTES

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help

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IBIS Open Forum Reflector (IBIS@eda.org)
IBIS Users' Group Reflector (IBIS-users@eda.org)
State your request.

IBIS-info@eda.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the EIA-IBIS Open Forum as a full Member.

IBIS@eda.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

IBIS-users@eda.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

IBIS-bug@eda.org

To report IBISchk parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/IBIS/bugs/IBISchk/
http://www.eda.org/IBIS/bugs/IBISchk/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/IBIS/icm_bugs/
http://www.eda.org/IBIS/icm_bugs/icm_bugform.txt

To report s2IBIS, s2IBIS2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/IBIS/bugs/s2IBIS/bugs2i.txt
http://www.eda.org/IBIS/bugs/s2IBIS2/bugs2i2.txt
http://www.eda.org/IBIS/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eigroup.org/IBIS/IBIS.htm

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/IBIS/directory.html

IBIS CURRENT MEMBER VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	February 20, 2009	March 13, 2009	April 3, 2009	April 23, 2009
Actel	Producer	Inactive				
Advanced Micro Devices	Producer	Inactive	√		√	
Agilent Technologies	User	Inactive				√
Ansoft	User	Inactive	√			
Apple Computer	User	Inactive				
Applied Simulation Technology	User	Inactive				
ARM	Producer	Inactive	√			
Cadence Design Systems	User	Inactive			√	
Cisco Systems	User	Active	√	√	√	
Ericsson	Producer	Active	√		√	√
Freescale	Producer	Inactive				
Green Streak Programs	General Interest	Inactive	√			
Hitachi ULSI Systems	Producer	Inactive				
Huawei	User	Inactive		√		
IBM	Producer	Inactive	√	√		
Infineon Technologies AG	Producer	Inactive				
Intel Corp.	Producer	Inactive	√	√		
LSI	Producer	Active	√	√	√	
Marvell Semiconductor	Producer	Inactive				
Mentor Graphics	User	Inactive	√	√		
Micron Technology	Producer	Active	√	√	√	
Nokia Siemens Networks	Producer	Active	√		√	√
Samtec	Producer	Inactive				
Signal Integrity Software	User	Active	√	√	√	
Sigrity	User	Inactive				
Synopsys	User	Inactive				
Teraspeed Consulting	General Interest	Active	√	√	√	
Texas Instruments	Producer	Inactive	√			
Toshiba	Producer	Inactive				
Xilinx	Producer	Inactive			√	
ZTE	User	Inactive				
Zuken	User	Inactive				√

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

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