EIA IBIS Open Forum Minutes

Meeting Date: **November 11, 2008**

GEIA STANDARDS BALLOT VOTING STATUS
See last page of the minutes for the voting status of all member companies.

VOTING MEMBERS AND 2008 PARTICIPANTS

Actel	(Prabhu Mohan)
Agilent Technologies	Sanjeev Gupta, Radek Biernacki, Amolak Badesha Fangyi Rao, [Ian Dodd], Yutao Hu, Vuk Borich Nobutaka Arai, Ludwig Eichingner, Cheng-ming Ren*, Xuliang Yuan*, Jianping Zhu*
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Ansoft Corporation	Steve Pytel, Ricardo Teliuteuesh, Dan Dvorscak, Steele Deng*, Donny Hou*, Baolong Li*, Davis Yan*, Long Yang*, Song Zheng*
Apple Computer	(Bill Cornelius)
Applied Simulation Technology	(Fred Balistreri)
ARM	(Nirav Patel)
Cadence Design Systems	Terry Jernberg, Hemant Shah, Ambrish Varma [C. Kumar], Brad Griffin, Zhen Mu, Lanbing Chen*, Wenliang Dai*, Feng Li*, Shirley Li*, Jinbai Liu*, Ping Liu*, Yabao Meng*, Jian (John) Peng*, Jain Shan*, Hui Wang*, Yitong Wen*, Yitong Wu*, Dingru Xiao*, Ke (Coco) Xu*, Feng Yu*, Rong Zhang*, Wenjiang Zhang*, Alex Zhao*, George Zhou*
Cisco Systems	Syed Huq, Mike LaBonte, AbdulRahman (Abbey) Rafiq Huyen Pham, Emily Yao, Susmita Mutsuddy John Fisher, Paul Ruddy, Jun Li, Jianmin Zhang Luis Boluna, Kelvin Qiu, Jane Lim, Ilyoung Park Rick Brooks, Chris Padilla, Ehsan Kabir, Jin (Leo) Hu*, Weifeng Shu*, Xinghai (Sean) Tang*, Huihui (Iris) Zhao*
Ericsson	Anders Ekholm*
Freescale	Jon Burnett
Green Streak Programs	Lynne Green
Hitachi ULSI Systems	Kazuyoshi Shoji
Huawei Technologies	Tao Guan*, Xiaoqing Dong, Yu Chen*, Jing Fu*, Peng Huang*, Jinjun Li*, Bo Liu*, Mongfang Lv*, Shaokun Shen*, Victor Wang*, Shisheng Wu*, Qilin Xu*, Zhenlong Xu*, Hang Ya*, Zhou Yang*, Wen Yu*, Cheng Zhang*, Gezhi Zhang*, Yuehui Zhu*
IBM	Adge Hawes
Infineon Technologies AG	Christian Sporrer

Intel Corporation	Michael Mirmak*, Rich Mellitz, Wei-hsing Huang Vishram Pandit, Lili Deng*, Haifeng Gong*, Fanghui Li*, Wenjie Mao*, Yang Qu*, Yiunglei Ren*, Wayne Tsuchimoto*, Yang Wu*, Maoxin Yin*, Xinjun Zhang*, James Zhou*
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Mentor Graphics	Arpad Muranyi, John Angulo, Minggang Hou*, Jane Liao*, Xuefeng Liu*
Micron Technology	Randy Wolff*
Nokia Siemens Networks GmbH	Eckhard Lenski, Klaus Huebner, Katja Koller, Xianyun Wang*
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Sigrity	Sam Chitwood, Brad Brim, Ben Franklin Kristopher Stytte, Raymond Chen*, Jiangsong Hu*, Xianfeng Li*, Tao (Helen) Xu*
Synopsys	Ted Mido, Xuefeng Chen*, Wenyun Gu*, Jinghua Huang*, Deng Shi*
Teraspeed Consulting Group	Bob Ross*, Tom Dagostino, Al Neves
Texas Instruments	Richard Ward, Pavani Jella
Toshiba	Yasumasa Kondo, Noriyasu Yoshikawa
Xilinx	David Banas*, Ajay Shah, Suzanne Yiu Mustansir Fanaswalla
Zuken	Michael Schaeder, Ralf Bruening
ZTE	Huifeng Chen*, Xiaolin Chen*, Jinku Guan*, Hui Jiang*, Nan Jiang*, Shiju Sui*, Zhiwei Yang*, Shunlin Zhu*

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Aica Kogyo	Akihiro Tanaka
Alcatel-Lucent	Haibo Wang*
Alcatel-Shell	Weiping Chen*, Feng Ji*
Altera	Ravindra Gali, Jing Wu, John Oh, Hui Fu
Avago Technologies	Minh Quach, Sari Tocco
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Tyco Electronics	Chad Morgan
Universal Scientific Industrial	Lurker Li*, Spenser Tang*
VeriSilicon Microelectronics	Qiang Chen*, Steven Gou*, Zhiying Yuan*
Vertical Circuits	Mark Egbers
Winwin Corporation	Haiphe Lau*, Linfa Liu*
Xsigo Systems	Robert Bada
Independent	Guy de Burgh, Ardy Forouhar, Dave Galloi Kazuhiko Kusunoki

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS summits teleconferences are as follows:

Date	Telephone Number	Bridge #	Passcode
November 14, 2008	ASIAN IBIS SUMMIT (JAPAN)		NO TELECONFERENCE
November 21, 2008	1-866-432-9903		121522040

All meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, provide the bridge number and passcode at the automated prompts. If asked by an operator, please request to join the IBIS Open Forum hosted by Michael Mirmak. For international dial-in numbers, please contact Michael Mirmak.

NOTE: "AR" = Action Required.

WELCOME AND KEYNOTE COMMENTS

The IBIS Open Forum Summit was held in Shanghai, PRC at the Shanghai Mart. About 142 people representing 39 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda.org/pub/ibis/summits/nov08a/

Jinjun Li of Huawei Technologies began the meeting shortly after 9 AM. Mr. Lance Wang assisted with translations.

Jinjun expressed appreciation to the IBIS group and sponsors of the event. He mentioned that IBIS Summits have been happening since 2005, and there have been excellent paper presentations at the summits. He welcomed all to Shanghai.

Michael Mirmak made brief remarks and opened the meeting. He recognized the IBIS committee members present at the meeting. He mentioned the importance of technology in our lives and the importance of specifications such as IBIS in developing new technology. He thanked all the sponsors of the event including Huawei Technologies, Agilent Technologies, Ansoft, Cadence Design, Cybernet Systems, Intel, Mentor Graphics, SiSoft, Sigrity, Synopsys and ZTE Corporation. He also thanked the summit organizers.

LOOK INTO IBIS BUFFER CURVES

Lance Wang, IO Methodology

Lance reviewed the circuit elements of a basic I/O buffer. He then related these elements to their corresponding I-V curves in IBIS. He noted that all I-V curves are related to specific voltage references and showed examples of I-V curves for high, low and open buffer states. He overlaid load lines on the I-V curves. The voltage point where the load line intersected to the [Pullup] or [Pulldown] I-V curve corresponded to the endpoint voltage found in the V-t curves of the same load. He discussed the importance of maintaining timing relationships between the V-t curves. [Submodel] I-V curves were shown to demonstrate how to model on-die termination characteristics.

A question was asked about the difference between using the [Ramp] data and the V-t data. Lance explained that it was important to include V-t data for more correct results from simulation.

STUDY OF SOLVING IBIS SINGLE VT

Xuefeng Chen, Synopsys

Xuefeng began by reviewing that solving for [Pullup] and [Pulldown] scaling coefficients is commonly done with the 2-equation, 2-unknown method. Theoretically, there is no solution for a single V-t curve. He showed waveforms of Kd and Ku values during a low to high transition of a buffer output. He demonstrated one method of solving for Ku and Kd values when only one V-t waveform is available. Results were shown for various test loads. A second method imposed a constraint relating Ku and Kd. This method showed worse accuracy. He concluded that there is not a good general method to get an accurate solution for all IBIS models with a single V-t waveform.

A question was asked if Ku and Kd parameters change with different loads. Xuefeng explained that these parameters relate to the physical device and do not change with load. A question was asked about how to use more than two sets of V-t curves. The answer was that you use two sets at a time, but use the sets that most closely match the load of the system. Also, one should try to set R_fixture to a value close to the transmission line impedance of the system.

MICRON'S IBIS MODEL QUALITY PROCESS

Randy Wolff, Micron Technology

Randy highlighted that building a quality IBIS model involves building quality checks into each step of the model creation process. The process begins with a quality Spice model. Including multiple pre-driver stages ensures that the model input stimulus does not affect the output slew rate and timing. Critical timing paths should not be modified. Micron has two choices of netlists for inclusion of layout parasitics. An RC netlist provides the best match to silicon but is a much larger netlist than a C-only netlist. A good compromise is to use a C-only netlist but add RC models on critical nets to match timing delays of long metal lines. The resulting netlist shows good correlation to the RC netlist when looking at rising and falling waveform crossing voltage, Vox. C_comp minimum and maximum corners should be adjusted to match the range seen from silicon measurements including the package. When correlating I-V curves to measurements, voltage and temperature are easy to adjust, but it is more difficult to know how to adjust the transistor process model to match the silicon. Randy detailed a method for adjusting the process model to match the silicon. Detailed checklists should be used during both the Spice and IBIS model creation processes. Example checklists were shown. Randy mentioned the importance of the IBIS Quality task group's work. Micron releases a detailed

report with each IBIS model comparing the model to specification data and measurement data and comparing the IBIS model to the Spice model. Randy showed an example of Micron's quality report. He concluded that model users should demand quality models from vendors and show them examples of quality models.

David Banas asked about bounding of capacitance measurements and how to adjust C_comp. Randy explained that he uses variation in C_comp to bound the measurement data, but this is kept within a reasonable range, such as +/- 200fF for a mature process. Another question was asked if the process model could be adjusted in the corners if enough measurement data of the process was taken. Randy said that this could be done to create a model showing less process variation than may be found in the transistor model library, but only with enough measurement data to justify less process variation.

USING BEHAVIORAL-LEVEL MODEL FOR SSN ANALYSIS

Zhiwei Yang, Shunlin Zhu, ZTE Corporation

Zhiwei showed a schematic of a multi-driver model for analyzing simultaneous switching characteristics. He introduced three simulation methods including using Spice models, IBIS models and macro-model based IBIS models. The test circuit included five drivers and a 2-port RLGC package model. He showed waveform results from the simulations. The IBIS model results are not accurate enough for full SSN evaluation, as they overestimate power, ground and quiet line noise. Improvements are needed to the model such as use of macro-models to provide voltage feedback or use of a BIRD95 methodology. He stressed the importance of developing software to convert BIRD95 Spice data to IBIS format and supporting IBIS 5.0 in EDA software.

A question was asked if coupling of the package from power to ground was considered. Zhiwei answered that no, a simplified model was used for this part of the analysis.

NEW TABLE-BASED MODELS IN IBIS 5.0, A COOKBOOK-STYLE GUIDE

Michael Mirmak, Intel Corporation

Michael began with a summary of IBIS development. He noted two new table-based keywords in IBIS 5.0. BIRD98 introduced [ISSO_PD] and [ISSO_PU] and BIRD95 introduced [Composite Current]. A cookbook style method was demonstrated for extracting the [ISSO_PD] and [ISSO_PU] data from a buffer. He stressed the importance of excluding diode clamp current from ISSO tables (including on-die termination effects). He noted that the ISSO keywords do not describe the pre-driver stage but describe static current modulation. The [Composite Current] data should include tables using the same load as the V-t tables and be time correlated to the V-t tables. The power delivery structure must be complete including buffer rail inductances and resistances, pre-driver structures and on-die decoupling structures. He summarized that model makers should start collecting this data now and encouraged the EDA tool providers to support these keywords.

A question was asked if BIRD95 includes a way to model the on-die decoupling. Michael explained that there are no keywords included in the BIRD for this now. A second question was asked if the on-die decoupling is included on a per-buffer basis. Michael responded that one must be consistent with modeling an entire device or a single buffer. Bob Ross commented that you can use the series element keywords to model the on-die decoupling circuit. Another

question was asked if [ISSO_PU] and [ISSO_PD] should be used with a model simulated with power supplies internal or external to the model. Michael said that the keywords are best used when modeling an external power supply where you could then model power supply noise.

IBIS EBD MODELING, USAGE AND ENHANCEMENT, AN EXAMPLE OF MEMORY CHANNEL MULTI-BOARD SIMULATION

Tao Xu, Sigrity

Tao began by showing the typical system memory bus structure for a two DIMM system. Several challenges in memory channel simulation exist including multi-drop topologies, high speed signaling with transmission loss, tighter timing among different signal groups, significant crosstalk and SSO and model accuracy. She introduced EBDs and noted that they are good for transmission effect assessment and timing analysis for first order considerations. Sections of EBD syntax were shown for a DIMM module address path and for a differential data strobe path. An EBD simulation problem was presented. Tao noted that PDS noise was simulated on the motherboard, but the EBD assumes ideal powers and grounds, so much information is lost by using an EBD for the DIMM. Also, crosstalk analysis is incomplete. She recommended enhancing EBD for improvements to crosstalk and power and ground effects analysis. She demonstrated the ability to simulate both power integrity and signal integrity effects for proper SSN analysis and concluded that enhancements are required for EBD.

A question was posed that lots of vendors support multi-board simulation, so why not use more complete board models than EBDs. Tao explained that multi-board simulation is very slow to simulate and board models are not always available due to IP protection.

TOUCHSTONE VERSION 2.0 MIXED-MODEL SYNTAX

Bob Ross, Teraspeed Consulting Group

Bob noted that terms used in Touchstone include SE for single-ended, MM for mixed-mode and GMM for generalized mixed-mode. The original Touchstone was issued in 1984. Touchstone version 2.0 is extended to remove some format limitations and to add some resistance-per-port flexibility for PDS applications. Touchstone 2.0 adds eight IBIS-like keywords. Details of the keywords are found in the IBIS summit meeting at DesignCon 2008. Only four of the keywords are required. He showed the differences in block arrangement between Touchstone version 1.0 and 2.0. He highlighted that the new [Mixed-Mode Order] keyword applies to S, Y and Z n-port matrices. Mathematical details are found in the Touchstone 2.0 specification. Examples were shown of converting single-ended data to generalized mixed-mode and mixed-mode data formats. Several EDA tools are already implementing portions of the mixed-mode syntax. He noted that the specification is not yet completed, so minor changes are still being considered.

OPTIMUM FREQUENCY SAMPLING IN S-PARAMETER EXTRACTION AND SIMULATION

Jinghua Huang, Synopsys

Jinghua noted that there are many issues in S-parameter creation such as limited frequency range coverage, no DC point, coarse sampling, non-passivity and noise. These issues cause problems in simulation. AC analysis results were shown for two models using sparse and dense sampling points. Transient analysis showed significant differences between the models as well. A good S-parameter data set provides the DC point, covers a wide enough frequency range, has dense enough data, is passive and has no measurement noise. Interpolation and

extrapolation methods can be used to correct bad S-parameter data and make it useful. Several methods are available with various advantages and disadvantages. Differences were shown between using Real/Imaginary and Magnitude/Angle interpolation. Noise filters can be used to smooth data. Passivity checking and enforcement are very important. Data should be plotted on a Smith chart before determining which methods to use for data correction. Good S-parameters always show beautiful curves on the Smith chart.

A question was asked if using the Smith Chart, can you check for causality. Jinghua explained that you need tools to convert to the time domain to see if any data occurs before time zero.

SYSTEM-LEVEL SERIAL LINK ANALYSIS USING IBIS-AMI MODELS

Todd Westerhoff, SiSoft

Todd began by detailing requirements for analyzing serial links. Multi-million bit simulations are needed as well as modeling of equalization and clock recovery circuits. IP must also be protected. There are challenges with using traditional SerDes analysis. SerDes vendor tools don't work together and open-source tools lack IP vendor models. IBIS-AMI is a new serial link analysis method and is now part of IBIS 5.0. It divides SerDes simulation into two parts – network characterization and communications analysis. IBIS-AMI models include an analog model and an algorithmic model. Designing a serial link involves a lot of analysis and design decisions. Statistical analysis directly computes eye distributions and is extremely fast. Tap settings are easily optimized for a transmitter to minimize bit error rate. Time domain analysis can be used to model non-linear effects and time-varying behavior including adaptive optimization. The Rx DFE model can include adaptive equalization to optimize tap coefficients based on an input data stream. IBIS-AMI models provide significant performance enhancement over Spice simulation and equivalent performance to proprietary SerDes simulation tools. Comparisons were shown between an IBIS-AMI model and both Spice and IBM HSSCDR. The results correlated very well.

IBIS-AMI SUPPORT VIA VHDL-AMS

Arpad Muranyi, Minggang Hou, Mentor Graphics

Minggang began by noting that one vendor's implementation of VHDL-AMS has a built-in function that acts as a C-code interface. This function was used to call an IBIS-AMI model into a VHDL-AMS simulator using a C-code wrapper. An example was shown using IBIS-AMI Tx and Rx models. A time domain simulation generates a channel response, and then the AMI Tx and Rx models are executed using that channel response. Waveform results are then plotted. In conclusion, IBIS-AMI models (DLLs) are fully supported in VHDL-AMS through attributes. Any programming language capable of producing executables could also be supported in the same way.

A question was asked of where the DLL model came from. Minggang responded that it came from a vendor.

AMI MODEL IN SI SIMULATION

Tao Guan, Huawei Technologies

Tao began with background on serial link simulation development. IBIS 5.0 now provides users

with a good solution for serial link simulation. He showed a simulation using an AMI model including a 3-tap Tx FFE and a 5-tap Rx DFE simulated at 11.0Gbps. Three different channels were analyzed. A channel analysis report was shown that summarized eye height and eye width under different bit error rates. Eye diagram and bathtub curve results were plotted. Highlights of the simulation approach included simulation of a large number of bits, inclusion of FFE, CDR and CDR circuits, consideration of jitter and DFE and FFE coefficient auto-calculation. A drawback of the simulation was that the AMI model was in a vendor specific (non-IBIS) format, and with current AMI models, users can't analyze the contribution of clock jitter and power noise due to the lack of a jitter transfer function (JTF) and power noise sensitivity (PNS). Also, a mask specification was not included with the model, and Tao felt that this needs to be included in AMI. JTF and PNS contributions were analyzed in more detail as they apply to a PLL. If PLLs are to be modeled in IBIS-AMI, JTF and PNS will need to be added to the AMI model.

EYE DIAGRAMS IN IBIS

Yubao Meng, Cadence Design Systems

Yubao noted that eye diagrams are very important for SI analysis, but IBIS does not support inclusion of eye mask data in the specification. Including eye mask data in IBIS models would improve design flows by encouraging earlier eye mask checking. Eye mask data added to the specification could represent either standards such as PCI Express or device specific eye limits. Eye masks included for SerDes channel analysis would allow easy checking of interface compliance. For source synchronous channels, the eye mask might relate to setup and hold time limits and be aligned to the clock/strobe. Examples were shown for HDMI, HDMI TP2, source synchronous and common clock eye masks. By including eye masks in the IBIS model, this will promote earlier use of eye masks in the design process and IC vendors might also be allowed to advertise their device-specific, less stringent eye mask requirements.

QUASI-ANALYTICAL ESTIMATION OF VERY LOW BIT ERROR RATE

Dingqing Lu, Sanjeev Gupta, Mihai Marcu, Xuliang Yuan, Agilent Technologies

Dingqing noted that a very low bit error rate (BER) estimation for a system with ISI, jitter and noise is needed. Monte Carlo analysis is very slow, so fast BER techniques have been proposed. First the BER is estimated using a Monte Carlo analysis. Then, a quasi-analytical (QA) method is used. The results matched very well. The QA analysis was also used to plot the BER versus time offset. The QA method showed a large reduction in simulation data points needed to determine a small BER versus the Monte Carlo method.

A question was asked if the QA method is similar to what is used in StatEye. Dingqing noted that they are not easily compared.

ACCURATE GHZ CHANNEL SIMULATION AND STATISTICAL ANALYSIS FOR SSE (SOLUTION SPACE EXPLORATION)

Baolong Li*, Weiping Hou**, Ansoft*, Huawei Technologies**

Baolong explained that the traditional serial link analysis was done with Spice simulation or mathematical methods such as Matlab. A Spice simulation was used to analyze a 6.25Gbps serial link and compared to measurements. Then the fast convolution method of statistical analysis was shown. An LTI assumption was made for the statistical analysis. Solution space

exploration is much easier using statistical analysis methods due to simulation speed improvements. Statistical analysis methods can be used to analyze BER as well as jitter and plotting of an eye mask. With a full channel model, the effects of back-drill length, anti-pad diameter, connector parasitic and transmission line length can be analyzed separately and swept together in SSE simulations. This analysis methodology is realistically only possible with use of statistical analysis techniques.

CONCLUDING ITEMS

Michael Mirmak thanked the presenters, sponsors, co-sponsors and attendees for their support and participation. The meeting adjourned at approximately 5:30 PM.

NEXT MEETING

The next IBIS Open Forum summit will be held in Tokyo, Japan on November 14. The next teleconference will be held November 21, 2007 from 8:00 AM to 10:00 AM US Pacific Time. Minutes may be delayed due to summit activities.

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NOTES

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To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

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To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS

clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

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http://www.eda.org/ibis/bugs/ibischk/
http://www.eda.org/ibis/bugs/ibischk/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
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Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eigroup.org/ibis/ibis.htm

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

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GEIA STANDARDS BALLOT VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	September1 9, 2008	October 10, 2008	October 31, 2008	November 11, 2008
Actel	Producer	Inactive				
Advanced Micro Devices	Producer	Active	√	√	√	
Agilent Technologies	User	Inactive				√
Ansoft	User	Inactive				√
Apple Computer	User	Inactive				
Applied Simulation Technology	User	Inactive				
ARM	Producer	Inactive				
Cadence Design Systems	User	Inactive				√
Cisco Systems	User	Active	√	√	√	√
Ericsson	Producer	Active		√	√	√
Freescale	Producer	Inactive				
Green Streak Programs	General Interest	Inactive				
Hitachi ULSI Systems	Producer	Inactive				
Huawei	User	Inactive				√
IBM	Producer	Active		√	√	
Infineon Technologies AG	Producer	Inactive				
Intel Corp.	Producer	Active	√		√	√
LSI	Producer	Inactive				
Marvell Semiconductor	Producer	Inactive				√
Mentor Graphics	User	Active	√	√		√
Micron Technology	Producer	Active	√	√	√	√
Nokia Siemens Networks	Producer	Active	√	√	√	√
Samtec	Producer	Inactive				
Signal Integrity Software	User	Active		√		√
Sigrity	User	Inactive				√
Synopsys	User	Inactive				√
Teraspeed Consulting	General Interest	Active	√	√	√	√
Texas Instruments	Producer	Active	√		√	
Toshiba	Producer	Inactive				
Xilinx	Producer	Active	√		√	√
ZTE	User	Inactive				√
Zuken	User	Inactive				

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH GEIA BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
- PRODUCERS - MEMBERS THAT SUPPLY ELECTRONIC EQUIPMENT.
- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.