EIA IBIS Open Forum Minutes

Meeting Date: **September 14, 2007**

GEIA STANDARDS BALLOT VOTING STATUS
See last page of the minutes for the voting status of all member companies.

VOTING MEMBERS AND 2007 PARTICIPANTS

Agilent	Ian Dodd*, Radek Biernacki, Saliou Dieye, Riccardo Giacometti, Quanli Li, Mike Resso, Chengming Ren, Dong Wei, Tim Wu, Xindong Xue, Nianmin Zhang, Jianping Zhu, Takahiro Sato*
AMD	Nam Nguyen, Tadashi Arai*
Ansoft Corporation	Haiqiang Ding, Baolong Li, Ying Liu
Applied Simulation Technology	(Fred Balistreri)
Apple Computer	(Bill Cornelius)
Cadence Design Systems	[Lance Wang], C. Kumar, Hemant Shah, Patrick dos Santos, Ambrish Varma, Shangli Wu, Lanbing Chen, Jianwei Hu, Jacob Lai, Yubao Meng, Jian Peng, Ke (Coco) Xu, Liu Zheng, Norikazu Takada*, Yukio Masuko*
Cisco Systems	Syed Huq*, Tram Bui, AbdulRahman Rafiq, Huyen Pham, Darja Padilla, Mike LaBonte, Paul Ruddy, Gurpreet Hundal, Luis Boluna, Ehsan Kabir, Jehyoung Lee, Susmita Mutsuddy, Eddie Wu, Bill (Qinghua) Chen
Ericsson	Anders Ekholm*, Ole Segtum, Peng Fu,
Freescale	Jon Burnett
Green Streak Programs	Lynne Green
Hitachi ULSI Systems	Kazuyoshi Shoji*, Shinmei Hirano*
Intel Corporation	Michael Mirmak*, [Arpad Muranyi], Lili Deng, Haifeng (Bill) Gong, Tao Hu, Karen Kang, Fanghui Li, Maoxin Yin, James Zhou
IO Methodology	Lance Wang*, Esther Gao, Nancy Peng, Benny Yan, Xinjun Zhang, Wei Zhu
LSI	Frank Gasparik, Kim Helliwell, Dinh Tran, Praveen Soora, Brian Burdick
Mentor Graphics	John Angulo, Arpad Muranyi*, [Ian Dodd], Eric Rongere, Stephane Rousseau, Bill Hargin, Patrick Carrier, Vivian Pan, Tao Wang, Lifu You, Kenji Kushima*, Masahiro Nakajima*
Micron Technology	Randy Wolff, Pavani Jella
Nokia Siemens Networks GmbH[1]	Eckhard Lenski, Flavio Maggioni, Roberto Preatoni, Umberto Gatti, Massimo Ceppi

Panasonic	Atsuji Ito*
Samtec	(Corey Kimble)
Signal Integrity Software	Barry Katz, Douglas Burns, Mike Steinberger, Walter Katz, Todd Westerhoff*
Sigrity	Sam Chitwood*, Sandy Dung, Raymond Chen, Xianfeng Li, Tao (Helen) Xu
STMicroelectronics	Antonio Girardi, Giacomo Bernardi, Roberto Izzi, Akhilesh Chandra*
Synopsys	Ted Mido, Xuefeng Chen, Changlei Zhang
Teraspeed Consulting Group	Bob Ross*, Tom Dagostino
Texas Instruments	Otis Gorley, Richard Ward, Bonnie Baker
Toshiba	Yoshihiro Hamaji*, Yasumasa Kondo*, Atshshi Osaki* Nonyasu Yoshikawa*, Toshihiro Tsajimura*
Xilinx	Bruce Bandeli, David Banas*
ZTE	Songrui Chen, Xianhui Hu, Wei Jia, Dongfeng Sun Changjun Wang, Ying Xiong, Shenglong Yang Yanfeng Yu, Xiaojun Zhou, Shunlin Zhu
Zuken	Michael Schaeder, Ralf Bruening, John Berrie, Hayashi*, Hirohiko Matsuwawa*

OTHER PARTICIPANTS IN 2007

74ze Engineering	Linc Jepson
AcconSys	David Lan, Suny Li, Jianfeng Tan, Jiangtao Wu, Frank Xiao
Agere	(Nirav Patel)
Alcatel Shanghai Bell	Wei Li, Lifan Sun
Altera	Hui Liu, Zhe Lin, Ravindra Gali, Salman Jiva
Apache Design Solutions	(Ji Zheng)
Applied Telisis, Inc. (ATI)	Vladimar Mandrusov
ATE Service Corporation	Yutaka Honda*
Canon	Seiji Hayashi*, Shoji Matsumoto*, Tatsuo Nishino*, Sakuragi Takamasa*, Haruka Watanabe*, Nobuaki Yamashita*
Cavium Networks	Johann Nittmann
CEC Huada Electronic Design	Weiwei Liu
China Integrated Circuit	Jingcheng Luo
ChipX	Jay Hidy, Oren Dvir
Cybernet Systems	[Kazuhiki Kusunoki], Masahito Kobayashi*, Junko Kuriyama*
Dangtang Mobile	Fanjie Meng, Hongying Li, Hongwei Wang
EDN China	Frank Yao
EE Times Japan	Norihiro Satsukawa*
EFM	Ekkehard Miersch
EMC Technology	Michael Liu, Feng Lu, Changzheng Yang
Enterasys	Robert Haller

Extreme Networks	Kevin Ko
Fluent	(Chetan Desai)
Force10 Networks	Robert Badal
Free Electron Software	Al Davis
Fujitsu Limited	Kouichiro Asoh*, Tetsuya Inoue*, Toshiro Sato*, Fujimori Shogo*, Wasaki Tosaka*
GEIA	(Chris Denham)
Gnovo Technologies	Harris Ma
Hangzhou H3C Technologies	Chunbao Yan
Hewlett Packard	Shafiq Rahman
Huawei 3Com	Junjun Cui, Zhenyu Liu, Jun Mao, Bao Wang, Kai Xie, Haitao Zhang
Huawei Technologies	ChunXing Huang, Bob He, Tao Guan, Peng Hu, Xiangzhong Jiang, Meidan Liu, Haiyan Yu
IBM	Michael Sorna, Adge Hawes, Kevin Kramer, Wei Wang
IMECAS	Yunfeng Wang
IVIS Co.	Hiroyuki Mashima*
Infineon	Christian Sporrer
Integrated Circuit Systems (ICS)	(Dan Clementi)
Japan Aviation Electronics Industries	Hiroaki Ikeda*
JEITA	Atsushi Ishikawa*
Juniper Networks	Raul Lozano
Kawasaki Microlelectronics	Hiroyuki Sato*, Takashi Kawahara*
Leventhal Design	Roy Leventhal
LHWT Microelectronics	Jiahui Wang
Lynguent	Andrew Levy
Motorola	Hong Chen, Haiying Jiang, Daniel Tang
National Institute of Applied Science (INSA)	Etienne Sicard
National Instruments	Lee Maixman
Netlogic	Eric Hsu
NEC Electronics Corporation	Takeshi Watanabe*, Hock Seow, Huy Tran, Itsuki Yamada*
NESA	Edward Sayre
Northrop Grumman	Dusan Radosevic
Nortel Networks	Jingxin Bian, Feng Shi
Nuova Systems	Zhiping Yang, Lin Shen
NVIDA Corporation	Jing (Jane) Zhang
NXP	H N Sudarshan
Optimal Corporation	Marc Kowalski
Politecnico di Torino	Igor Stievano, Michelangelo Bandinu
Renesas Technology	Takuji Komeda
Samsung	Sang-Soo Park

Sedona International	Joe Socha
Sharp	Tetsuo Iwaki*
Shizu Technology	Zuofu Qi
Siemens AG [1]	[Eckhard Lenski], Manfred Maurer
Silego	(Joe Froniewski)
Sony Corporation	Toshiro Honda*, Keisuke Matsunami*
Shu Zi Tai He	Chunyu Zhao
Sun Microelectronics	Leon Yang
Tiburon Design Automation	Patrick O'Halloran
Via Technologies	Jimmy Hsu
White Electronics Designs	John Perez
Xyratex	Paul Levin, Joseph Chan
Zuken Support and Service	Seikou Go*, Tomotaka Unose*

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Telephone Number	Bridge #	Passcode
September 21, 2007	1-916-356-2663	4	627-8629

All meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, provide the bridge number and passcode at the automated prompts. If asked by an operator, please request to join the IBIS Open Forum hosted by Michael Mirmak. For international dial-in numbers, please contact Michael Mirmak.

NOTE: "AR" = Action Required.

WELCOME AND KEYNOTE COMMENTS

The Asian IBIS Open Forum Summit (Japan) was held in Tokyo, Japan at the headquarters of JEITA (Japan Electronics and IT Industries Association). About 54 people representing 29 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda-stds.org/summits/sep07b/

Takeshi Watanabe opened the Summit with a few comments of welcome to the presenters and attendees. Michael Mirmak and Toshiro Honda, chair of JEITA's Technical Committee for

Standardization, also made opening statements, thanking the presenters and attendees for their support.

JEITA EDA WG ACTIVITY

Takeshi Watanabe, NEC ELECTRONICS

Takeshi summarized the structure and efforts of JEITA's EDA Work Group. This group supports standardization of passive devices, interconnects and active devices. Eight separate component groups are handled within the work group, including 16 member companies. The current activities of the work group include writing an IBIS guidebook for EDA simulation, providing comments on the proposed Touchstone® version 2.0 specification, assisting the IBIS Quality Task Group with quality improvements and in correlation of passive interconnect models to measurement. Takeshi concluded by thanking the IBIS Committee for its support.

IBIS QUALITY ACTIVITIES IN JEITA EDA WG

Yasumasa Kondo, Toshiba

Yasumasa began by noting that users of IBIS have tended to find many errors in commonly available models in recent years. Chip makers, system vendors and EDA vendors must cooperate to improve IBIS models, and JEITA is helping to work on quality improvement.

Quality was defined as comparing simulation result with measurement result. Errors in correlation can result from problems with EDA tool issues, measurement tool operator error or SPICE model in accuracy. JEITA does not focus on these areas. Instead, they focus on SPICE vs. IBIS comparison. Miscorrelations here can result from timestep control problems, other user settings or simulation tool differences. Individual companies have to reconfirm behaviors across various simulation tools. Is a simulation result calculated by different simulators "the same?" Several comparisons were shown.

Yasumasa compared two simulators using simple RLC packages and a resistive load at 100 MHz. A similar test was run using a lumped transmission line with 10 lumps. Both single-ended cases showed excellent matching across several tools. Differential response begins to cause variances in output, even with a simple resistor between two independent buffers with complementary drive patterns. Differences are significant both with RLC and lumped transmission lines. This is a major problem, as verification and validation are needed for ISO9001 compliance.

During the question period, Lance Wang suggested that a lack of split C_comp may account for the mismatches in the distributed T-line comparison. Arpad Muranyi suggested using two 50 ohm resistors in place of a single 50 ohm resistor in those cases, to check the common mode response (as a simple V-fixture is different than the moving complementary IBIS model). In response to a separate question, Yasumasa noted that no SPICE transistor-level comparison was performed.

VALIDATION FOR IBIS MODELS

Lance Wang, XinJun Zhang and Benny Yan, IO Methodology, Inc.

Lance reviewed current literature, noting that several quoted sources mentioned IBIS models

available today as being not accurate. This is, in his view, not a specification problem but a model quality problem. The IBIS Quality Task Group has committed resources here, but the most important idea is to validate the models before using them. Lance showed several examples involving V-T tables and C_comp sweeps. While excellent correlation was shown between tools using the same IBIS model containing four V-T tables, correlation became much worse when a V-T table was removed. Sweeps of C_comp showed that some tools were using C_comp data in simulating IBIS models into a purely resistive load. Lance generalized, stating that cross-tool correlation is often needed to validate IBIS model performance, but that this could be too costly and time consuming for IBIS model users and authors. He then described a separate, private effort to provide free validation reports for IBIS models.

IBIS TREE AND EVOLUTION DOCUMENT UPDATE

Bob Ross, Teraspeed Consulting Group

Bob summarized two documents now available that document the evolution of IBIS keywords and subparameters. The first, the IBIS tree, shows the relative hierarchy of keywords and their associated subparameters. The second, the IBIS evolution document, lists the major revisions of IBIS and the keywords each supports. This has been slightly updated since its last public review in July 2007.

JEITA ACTIVITY; IBIS GUIDE FOR THE JAPANESE ENGINEER

Kazuyoshi Shoji, Hitachi ULSI Systems

Kazuyoshi provided a brief introduction to IBIS for those not familiar with the standard and development. He noted that JEITA is now directly represented on the IBIS Committee through three member companies: Hitachi ULSI Systems, NEC Electronics and Toshiba. He continued by noting that frequently Japanese engineers are not familiar with IBIS and usually do not want to read 150 pages in English to become more knowledgeable As a result, a Japanese guidebook is under development by JEITA that would introduce and summarize IBIS, but would not be a direct translation of the specification. This document would include clean up for unused keywords and detailed common-language descriptions of features as the most important part of the guide. "Fuzzy" language used in the specification makes direct translation not very useful. He noted that the IBIS Cookbook is a very good reference, but it is still in English. The guidebook is expected to be published early next year. Case studies would be added and EDA vendors were encouraged to contribute.

Ian Dodd asked about whether examples of models would be contributed. Kazuyoshi suggested this would be most welcome. Arpad asked how the guide is to be different than the IBIS cookbook. Kazuyoshi responded that the cookbook does not cover the difficult keywords and their meaning in Japanese in plain language. Most model makers can create simple models easily today, so guidance is required on the more complex features not already part of the cookbook.

UNDERSTANDING AND USING ICM MODELS

YuBao Meng, Cadence Design Systems (presented by Yukio Masuko)

Yukio provided a brief review of the ICM (IBIS Interconnect Modeling) specification, including its support for both RLGC and S-parameter data. He showed three test cases where ICM can make interconnect modeling convenient: ICM for a package as a separate device in a topology

(used as a connector, for example), ICM as an explicit package model, and ICM S-parameters used in either situation. Swathing was also described, as a means of compactly describing interconnects with repetitive coupling behaviors.

A participant inquired regarding EBD versus ICM models and whether vendors were providing ICM models today. The questioner also noted that interconnect measurements are very hard, so vendors may not be willing to provide this model. The question was deferred to Hiroki Ikeda, who presented on this topic afterward. Hiroki did note that interconnect models in these formats are sometimes provided on a request basis today.

GUIDANCE OF PASSIVE EDA MODELS

Hiroki Ikeda, Japan Aviation Electronics Industry (JAE)

Hiroki summarized efforts to correlate EDA models of interconnects to actual measurements, particularly for S-parameters. VNA and TDR analyses were conducted for differential pairs over solid and mesh planes, a ribbon cable and a PCB filter fixture. Previous reports show correlation differences between three commercial simulators and measurement. Simulations were good match, generally. The basic problems include a lack of DC points within S-parameters and mismatches between the S-parameter bandwidth and size. Some manufacturers have disclosed measuring methods to the public. Hiroki showed numerous results of various measurement and modeling efforts. Correlations are very good for the ribbon cables. Any mismatches seen there may be due to FFT used to convert TDR data to S-parameter format. Solid-plane differential and filter fixture PCB results were also well matched to the measurements up to 20 GHz. The meshed plane differential pair results less so. All the data sets showed poorer matching between measurements and models between 0 and 100 MHz. Calculated waveforms tend to be more noisy than measured.

A participant asked how to calibrate the DC point using measurements. Is extrapolation enough to guarantee accuracy? Hiroki responded that extrapolation may provide questionable results. Further study is needed in this area.

ISSUES COMBINING BUFFER AND INTERCONNECT MODEL FORMATS

Michael Mirmak, Intel Corp.

Michael summarized the state of today's industry in terms of the different model formats provided for packages, other interconnects and buffers. IBIS has attempted to include all competing buffer modeling formats available today, including Berkeley SPICE, Verilog-A, VHDL-AMS and Verilog-AMS, to ensure that their advantages and disadvantages offset within IBIS. Similarly, package and interconnect formats are proliferating, with ICM being the latest attempt to create a standard, tool-neutral approach to interconnect descriptions. Earlier board and package descriptions included in IBIS now fail, as they do not describe coupling or loss effectively for today's designs.

Tying all these formats together is the latest challenge, as IC vendors need to provide full simulation "decks" or working topologies to their customers to prove their designs in a full system context. This often means using or supporting only one EDA tool, as no tool and no format can tie all the other buffer, package and interconnect formats together. Michael concluded by reviewing potential universal topology formats. At present, Verilog-A seems most promising but it does not contain a transmission line library or standard element, and does not

directly support IBIS or ICM as elements. A standard SPICE, as proposed in an earlier summit, may be the most effective general solution, but much work will be needed to finalize it.

Anders Ekholm inquired about packages models. Michael noted that ICM is the most promising package format, but that no direct links exist between it and IBIS. Anders also asked whether IBIS 4.2+Verilog-A+ICM is Michael's recommended solution. Michael responded that it seems to be the most advanced, but that Verilog-A still lacks any transmission line element, including ICM as well as lacking direct links to IBIS. A standard SPICE may still be the best long-term option for system integration, so long as it can include IBIS and ICM.

POWER DELIVERY SYSTEM DESIGN AUTOMATION

Tao Xu, Sigrity (presented by Sam Chitwood)

Sam reviewed how the PDS (power delivery system) of a platform can negatively influence signal quality and timing, noting that current increases and speed increases are driving a greater need for PDS analysis. Better system PDS performance comes from lower overall system input impedance looking "into" the system from the buffer, on the planes and power delivery network itself (not the buffer). For buffer-level SSO analysis, one can use BIRD95 or at least 4 V-t tables (not ramps). However, IBIS models do have limitations in SSO simulations, even beyond advantages over SPICE. One issue with PDN simulations is that results are very much pattern-dependent. Patterns such as 1010, etc. don't give the worst-case PDN integrity performance. IBIS also tends to be used for post-layout analysis, but it is less effective for pre-layout analysis.

Where power integrity really matters is at the silicon power rail pads. Most designs, Sam noted, have too many capacitors. Customers need to optimize costs by optimizing power delivery solution for performance target. Analysis and cost optimization of a system PD network can be optimized using an automated flow, including physical stackup and layout, decap library, and the electrical data on the initial placement of caps or a target impedance for the network. This Z_target provides an optimization goal for the system and can be used to either reduce overall costs or find the lowest cost for increasing performance. Sam proposed adding Z_target to the IBIS specification, to cover PDS design goals. For IO design, use individual cells to generate an acceptable target noise. Z_target is the acceptable impedance for those cells. Also, one can use a Z_target based on a previous design, if its performance was acceptable.

Arpad Muranyi asked where in the IBIS specification Z_target would be included. Sam suggested providing it at the [Pin Mapping] level, as a frequency-dependent table for the relationship between supply rails. Another participant asked whether a user can determine the optimum impedance using the power supply current, when several power supplies are involved. Sam answered that one would simply provide the target for each voltage rail, not one table for several rails. Anders Ekholm noted that this could not be done per pin pair as one would miss any individual trace behaviors due to use of shorted "average" rail behavior in IBIS.

IBIS-ATM UPDATE - SERDES MODELING AND IBIS

Todd Westerhoff, Signal Integrity Software (SiSoft)

Todd provided an overview of the work done by the Advanced Technology Modeling (ATM) Task Group within IBIS. Today, serial differential (SerDes) systems are more prevalent, with communications methods being applied to PCB signal integrity analysis. Most people are using

a two-step process: first, an analog simulation, then a network computation is done separately. This means characterizing the driver, receiver and interconnect network first, either in time or frequency domain. This is followed by analyzing how the network responds to multiple bits, similar to a DSP, and equalization. Serial links require modeling of TX and RX equalization, prediction of link behavior, analysis of error rates and protection of IP.

The ATM group has been working on developing an interoperable standard for describing SerDes devices. The models are algorithms in binary code, operating on analog information derived from simulation. The interfaces for execution and parameters are also standard, to exchange parameter and waveform information between the model and tool. The two methods described in the proposed standard, INIT and GETWAVE, provide this framework for channel impulse response and continuous waveforms, respectively.

Today, the current version of the standard was taken from an original developed by Cadence and IBM. Many participants contributed. Presentations are on-line, including the draft BIRD and demonstration toolkits are also available. Participants are invited to submit comments, suggestions and test the toolkits.

SERDES MODELING: IBIS-AMI EVALUATION TOOLKIT

Todd Westerhoff, Signal Integrity Software (SiSoft)

Todd summarized the free transmitter algorithmic toolkit published for industry testing. The model includes a model test program, model source code and compiled DLLs to perform TX equalization on an impulse response. Example input and expected output waveforms are provided. Todd noted that the source code of the actual tester program would be provided to the IBIS Open Forum in the future. He concluded by asking for industry comments and noted the existence of a new e-mail reflector for discussion of the files.

IBIS AMI MODEL DEVELOPERS TOOLBOX

Hemant Shah, Cadence Design Systems (presented by Hideko Masuko)

Hideko began by summarizing current problems with analysis of buses above 6 Gbps. These include problems of interoperability between the best solutions and poor accuracy among the standard ones. He noted the flow used in the ATM Work Group's proposals and provided an overview of the RX equalizer example to be made available shortly to the public. The equalizer model is a continuous time filter and will provide filtered output based upon an input impulse response. Example input and expected output waveforms for given settings will be provided.

Tadashi Arai asked about using this receiver model with a transmitter model. Is a transmitter model available? Hideko responded that a transmitter model was part of the Signal Integrity Software (SiSoft) release noted earlier and that both executables are compatible and interchangeable.

A REVIEW OF EXISTING MULTI-GBPS SERIAL CHANNEL ANALYSIS METHODS AND THE EVOLUTION OF THE PROPOSED IBIS ATM ALGORITHMIC MODELING STANDARD

Ian Dodd*, Richard Ward** and Sanjeev Gupta*, Agilent Technologies*, Texas Instruments**

Ian reviewed today's methods for analysis and drawing up standards for serial differential

systems. Today's IEEE standards address ICs while IBIS addresses PCBs and systems. These may need to be combined in future, as they are arriving at complementary solutions for various parts of systems. Silicon vendor design RX and TX circuits using models of PCB interconnects, correlating to measurements to fine-tune the results. PCB vendors choose IC vendors and technology, laying out the channel and resimulating based on PCB measurements and other data.

IC vendors face a challenge, in that SPICE is preferred for easy modeling of devices. Vendors want to minimize costs and protect IP but SPICE may no longer be appropriate for multi-GHz simulations, and PCB vendors would like tool interoperability and high simulation speeds. Three options therefore remain: circuit-level simulations with IBIS/SPICE transistor-level, etc. with high accuracy but low performance. Second: IBIS/SPICE macromodels for devices, with C, AMS, etc. for more complex behaviors, preserving circuit level data for system and interconnect. Third method: simulate entirely at the system level, with no circuit data, even of interconnect. S-parameters or pulse response characterization would be used alone, instead of circuit-level interconnect descriptions. In addition, circuit and system level co-simulation represents a good hybrid, with examples such as the public-domain StatEye tool. StatEye assumes fixed coefficients but the industry needs adaptive equalization for 10 Gbps, which implies a maximum frequency where StatEye no longer applies. One also needs statistical methods to include random jitter, because low-frequency events cause trouble. Additionally, one needs a means of including deterministic jitter.

ATM is a good option and start toward fast, interoperable device descriptions. However, it overlooks that most device designers actually create designs using RTL-oriented tools and flows. The standard does not support RTL directly, but requires it to be converted to C and then wrapped with the standard interface. ATM is also missing standard encryption for RTL code. The built-in drivers and receivers as used in StatEye are insufficient for today's complex and often proprietary designs – that is why we need a data exchange standard. Ian concluded by suggesting direct RTL code support in the ATM proposal.

One participant asked who creates the algorithmic model. Does the device vendor have to also create the interconnect model? Ian answered that the IC vendor will simulate with a representative model and (reference) boards but EDA vendors will also create example models for devices.

AN OVERVIEW OF HIGH-SPEED SERIAL BUS SIMULATION TECHNOLOGIES

Arpad Muranyi, Vladimir Dmitriev-Zdorov, Mentor Graphics Corp.

Arpad provided a detailed overview of serial-differential analysis techniques. Most simulators and system designs use LTI (linear and time-invariant) assumptions for interface architecture and analysis, using fast algorithms (including superposition and convolution) to get quick worst-case responses. Worst-case eye openings can be obtained through superposition of eye widths of a UI as a single waveform and summing appropriately. Statistical eyes for BER (bit error ratio or rate) use the probability of each cursor combination to calculate the chance of interface failure.

Jitter and crosstalk must also be considered, including whether victims and aggressors are synchronized and including the self-response of the driver. Deterministic jitter can be included using statistical techniques, sometimes using a sinusoidal shape; for simplification, people use

two pulse responses for this, but the accuracy is questionable. In a Gaussian distribution of probability, the tails of the distribution are where the eye can get closed down. For a worst-case bit pattern containing 50 pulses, the probability of finding the worst-case eye by applying a long random sequence would be 1 in 2^50 or less than 1 in 1e^15. The true worst-case pattern may occur more or less often depending on the tails of the PDF (probability distribution function).

Convolution-based algorithms are often used, but are limited by the length of the waveform used for the input. Fitted functions can be faster, are independent of waveform length and may have better dynamic range. Arpad suggested that the low-frequency response of a channel viewed in the AC domain can be analyzed to find resonances that may get missed in short, magnified impulse or pulse sequences.

Arpad also summarized equalization, including Finite Impulse Response (FIR) and Infinite Impulse Response (IIR). Both can be used for TX or RX designs. However, he cautioned that a feedback-type equalizer is non-linear compared to IIR and FIR. He concluded with a comparison of eye diagrams and BER bathtub curves for two types of feedback equalization.

Tadashi Arai asked whether there any established methods to get the worst-case bit sequence. Arpad responded that he knew of several proprietary ones. Tadashi followed up with a question regarding how we know the “realistic model” response Arpad mentioned is actually realistic. Arpad responded that users have to check several responses using several methods to draw any conclusions.

CONCLUDING ITEMS

Michael Mirmak thanked the presenters, co-sponsors and attendees for their support and participation. Takeshi Watanabe also thanked the participants and IBIS for their attendance and support. The meeting adjourned at approximately 5:00 PM

NEXT MEETING

The next IBIS Open Forum teleconference will be held September 21, 2007 from 8:00 AM to 10:00 AM US Pacific Time. Minutes may be delayed due to summit activities.

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NOTES

IBIS CHAIR: Michael Mirmak (916) 356-4261, Fax: (916) 377-3788
michael.mirmak@intel.com
Server Platform Technical Marketing Engineer, Intel Corporation
FM5-239
1900 Prairie City Rd.
Folsom, CA 95630

VICE CHAIR: Syed Huq (408) 525-3399, Fax: (408) 526-5504
shuq@cisco.com
Manager, Hardware Engineering, Cisco Systems

170 West Tasman Drive
San Jose, CA 95134-1706

SECRETARY: Randy Wolff (208) 363-1764, Fax: (208) 368-3475
rrwolff@micron.com
SI Modeling Manager, Micron Technology, Inc.
8000 S. Federal Way
Mail Stop: 01-711
Boise, ID 83707-0006

LIBRARIAN: Lance Wang (978) 633-3388
lwang@iometh.com
President / CEO, IO Methodology, Inc.
PO Box 2099
Acton, MA 01720

WEBMASTER: Syed Huq (408) 525-3399, Fax: (408) 526-5504
shuq@cisco.com
Manager, Hardware Engineering, Cisco Systems
170 West Tasman Drive
San Jose, CA 95134-1706

POSTMASTER: Bob Ross (503) 246-8048, Fax : (503) 239-4400
bob@teraspeed.com
Staff Scientist, Teraspeed Consulting Group
10238 SW Lancaster Road
Portland, OR 97219

This meeting was conducted in accordance with the GEIA Legal Guides and GEIA Manual of Organization and Procedure.

The following e-mail addresses are used:

majordomo@eda-stds.org
In the body, for the IBIS Open Forum Reflector:
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In the body, for the IBIS Users' Group Reflector:
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State your request.

ibis-info@eda-stds.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the EIA-IBIS Open Forum as a full Member.

ibis@eda-stds.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda-stds.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda-stds.org

To report ibischk parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda-stds.org/ibis/bugs/ibischk/
http://www.eda-stds.org/ibis/bugs/ibischk/bugform.txt

icm-bug@eda-stds.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda-stds.org/ibis/icm_bugs/
http://www.eda-stds.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda-stds.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda-stds.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda-stds.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eigroup.org/ibis/ibis.htm

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda-stds.org/ibis/directory.html

All eda.org documents can be accessed using a mirror:

http://www.ibis-information.org

Note that the "/ibis" text should be removed from directory names when this URL mirror is used.

GEIA STANDARDS BALLOT VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	August 3, 2007	August 24, 2007	September 11, 2007	September 14, 2007
Advanced Micro Devices	Producer	Inactive	√			√
Agilent Technologies	User	Active			√	√
Ansoft	User	Inactive			√	
Apple Computer	User	Inactive				
Applied Simulation Technology	User	Inactive				
Cadence Design Systems	User	Active	√	√	√	√
Cisco Systems	User	Active	√	√	√	√
Ericsson	Producer	Active		√	√	√
Freescale	Producer	Inactive				
Green Streak Programs	General Interest	Inactive				
Hitachi ULSI Systems	Producer	Active			√	√
Intel Corp.	Producer	Active	√	√	√	√
IO Methodology	User	Active	√		√	√
LSI Logic	Producer	Inactive	√	√		
Mentor Graphics	User	Active	√	√	√	√
Micron Technology	Producer	Inactive	√			
Nokia Siemens Networks	Producer	Inactive	√			
Panasonic	Producer	Inactive				√
Samtec	Producer	Inactive				
Signal Integrity Software	User	Active		√	√	√
Sigrity	User	Active		√	√	√
STMicroelectronics	Producer	Inactive				√
Synopsys	User	Inactive			√	
Teraspeed Consulting	General Interest	Active	√	√	√	√
Texas Instruments	Producer	Inactive				
Toshiba	Producer	Inactive				√
Xilinx	Producer	Inactive				√
ZTE	User	Inactive			√	
Zuken GmbH	User	Inactive				√

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH GEIA BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
- PRODUCERS - MEMBERS THAT SUPPLY ELECTRONIC EQUIPMENT.
- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.