EIA IBIS Open Forum Minutes

Meeting Date: **September 11, 2007**

GEIA STANDARDS BALLOT VOTING STATUS
See last page of the minutes for the voting status of all member companies.

VOTING MEMBERS AND 2007 PARTICIPANTS

Agilent	Ian Dodd*, Radek Biernacki, Saliou Dieye, Riccardo Giacometti, Quanli Li*, Mike Resso*, Chengming Ren*, Dong Wei*, Tim Wu*, Xindong Xue*, Nianmin Zhang*, Jianping Zhu*
AMD	Nam Nguyen, Tadashi Arai
Ansoft Corporation	Haiqiang Ding*, Baolong Li*, Ying Liu*
Applied Simulation Technology	(Fred Balistreri)
Apple Computer	(Bill Cornelius)
Cadence Design Systems	[Lance Wang], C. Kumar, Hemant Shah, Patrick dos Santos, Ambrish Varma, Shangli Wu, Lanbing Chen*, Jianwei Hu*, Jacob Lai*, Yubao Meng*, Jian Peng*, Ke (Coco) Xu*, Liu Zheng*
Cisco Systems	Syed Huq*, Tram Bui, AbdulRahman Rafiq, Huyen Pham, Darja Padilla, Mike LaBonte, Paul Ruddy, Gurpreet Hundal, Luis Boluna, Ehsan Kabir, Jehyoung Lee, Susmita Mutsuddy, Eddie Wu, Bill (Qinghua) Chen*
Ericsson	Anders Ekholm*, Ole Segtum, Peng Fu*,
Freescale	Jon Burnett
Green Streak Programs	Lynne Green
Hitachi ULSI Systems	Kazuyoshi Shoji*
Intel Corporation	Michael Mirmak*, [Arpad Muranyi], Lili Deng*, Haifeng (Bill) Gong*, Tao Hu*, Karen Kang*, Fanghui Li*, Maoxin Yin*, James Zhou*
IO Methodology	Lance Wang*, Esther Gao*, Nancy Peng*, Benny Yan*, Xinjun Zhang*, Wei Zhu*
LSI	Frank Gasparik, Kim Helliwell, Dinh Tran, Praveen Soora, Brian Burdick
Mentor Graphics	John Angulo, Arpad Muranyi*, [Ian Dodd], Eric Rongere, Stephane Rousseau, Bill Hargin, Patrick Carrier, Vivian Pan*, Tao Wang*, Lifu You*,
Micron Technology	Randy Wolff, Pavani Jella
Nokia Siemens Networks GmbH[1]	Eckhard Lenski, Flavio Maggioni, Roberto Preatoni, Umberto Gatti, Massimo Ceppi
Panasonic	(Atsuji Ito)
Samtec	(Corey Kimble)

Signal Integrity Software	Barry Katz, Douglas Burns, Mike Steinberger, Walter Katz, Todd Westerhoff*
Sigrity	Sam Chitwood, Sandy Dung, Raymond Chen*, Xianfeng Li*, Tao (Helen) Xu*
STMicroelectronics	Antonio Girardi, Giacomo Bernardi, Roberto Izzi
Synopsys	Ted Mido, Xuefeng Chen*, Changlei Zhang*
Teraspeed Consulting Group	Bob Ross*, Tom Dagostino
Texas Instruments	Otis Gorley, Richard Ward, Bonnie Baker
Toshiba	(Yasumasa Kondo)
Xilinx	Bruce Bandeli, David Banas
ZTE	Songrui Chen*, Xianhui Hu*, Wei Jia*, Dongfeng Sun* Changjun Wang*, Ying Xiong*, Shenglong Yang* Yanfeng Yu*, Xiaojun Zhou*, Shunlin Zhu*
Zuken	Michael Schaeder, Ralf Bruening, John Berrie

OTHER PARTICIPANTS IN 2007

74ze Engineering	Linc Jepson
AcconSys	David Lan*, Suny Li*, Jianfeng Tan*, Jiangtao Wu*, Frank Xiao*
Agere	(Nirav Patel)
Alcatel Shanghai Bell	Wei Li*, Lifan Sun*
Altera	Hui Liu, Zhe Lin, Ravindra Gali, Salman Jiva
Apache Design Solutions	(Ji Zheng)
Applied Telisis, Inc. (ATI)	Vladimar Mandrusov
Cavium Networks	Johann Nittmann
CEC Huada Electronic Design	Weiwei Liu*
China Integrated Circuit	Jingcheng Luo*
ChipX	Jay Hidy, Oren Dvir
Cybernet Systems	Kazuhiki Kusunoki
Dangtang Mobile	Fanjie Meng*, Hongying Li*, Hongwei Wang*
EDN China	Frank Yao*
EFM	Ekkehard Miersch
EMC Technology	Michael Liu*, Feng Lu*, Changzheng Yang*
Enterasys	Robert Haller
Extreme Networks	Kevin Ko
Fluent	(Chetan Desai)
Force10 Networks	Robert Badal
Free Electron Software	Al Davis
GEIA	(Chris Denham)
Gnovo Technologies	Harris Ma*
Hangzhou H3C Technologies	Chunbao Yan*
Hewlett Packard	Shafiq Rahman
Huawei 3Com	Junjun Cui*, Zhenyu Liu*, Jun Mao*, Bao Wang*, Kai Xie*, Haitao Zhang*

Huawei Technologies	ChunXing Huang*, Bob He, Tao Guan*, Peng Hu*, Xiangzhong Jiang*, Meidan Liu*, Haiyan Yu*
IBM	Michael Sorna, Adge Hawes, Kevin Kramer, Wei Wang*
IMECAS	Yunfeng Wang*
Infineon	Christian Sporrer
Integrated Circuit Systems (ICS)	(Dan Clementi)
JEITA	Atsushi Ishikawa
Juniper Networks	Raul Lozano
Leventhal Design	Roy Leventhal
LHWT Microelectronics	Jiahui Wang*
Lynguent	Andrew Levy
Motorola	Hong Chen*, Haiying Jiang*, Daniel Tang*
National Institute of Applied Science (INSA)	Etienne Sicard
National Instruments	Lee Maixman
Netlogic	Eric Hsu
NEC Electronics Corporation	Takeshi Watanabe, Hock Seow, Huy Tran
NESA	Edward Sayre
Northrop Grumman	Dusan Radosevic
Nortel Networks	Jingxin Bian*, Feng Shi*
Nuova Systems	Zhiping Yang, Lin Shen
NVIDA Corporation	Jing (Jane) Zhang*
NXP	H N Sudarshan
Optimal Corporation	Marc Kowalski
Politecnico di Torino	Igor Stievano, Michelangelo Bandinu
Renesas Technology	Takuji Komeda
Samsung	Sang-Soo Park
Sedona International	Joe Socha
Shizu Technology	Zuofu Qi*
Siemens AG [1]	[Eckhard Lenski], Manfred Maurer
Silego	(Joe Froniewski)
Shu Zi Tai He	Chunyu Zhao*
Sun Microelectronics	Leon Yang
Tiburon Design Automation	Patrick O'Halloran
Via Technologies	Jimmy Hsu*
White Electronics Designs	John Perez
Xyratex	Paul Levin, Joseph Chan

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS summits teleconferences are as follows:

Date	Telephone Number	Bridge #	Passcode
September 14, 2007	ASIAN IBIS SUMMIT (JAPAN)		NO TELECONFERENCE
September 21, 2007	1-916-356-2663	4	627-8629

All meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, provide the bridge number and passcode at the automated prompts. If asked by an operator, please request to join the IBIS Open Forum hosted by Michael Mirmak. For international dial-in numbers, please contact Michael Mirmak.

NOTE: "AR" = Action Required.

WELCOME AND KEYNOTE COMMENTS

The IBIS Open Forum Summit was held in Beijing, PRC at the Park Plaza Hotel Beijing. About 101 people representing 34 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda-stds.org/summits/sep07a/

XiangZhong Jiang of Huawei Technologies began the meeting shortly after 9 AM. Mr. Lance Wang assisted with translations. Mr. Jiang commented on the IBIS Summit meetings of the previous two years, and observed that participants have traditionally brought their best papers. He commented that paper quality is continuing to improve and suggested that next year's meeting be held in Shenzhen. He closed by giving his best wishes to the attendees for a successful meeting. Michael Mirmak repeated similar wishes, adding a few logistical announcements.

WANG ALGEBRA AND INTERCONNECTS

Bob Ross, Teraspeed Consulting Group

Bob Ross provided an overview of Wang algebra, a useful extension to standard algebra rules. These involve two extra rules when the same variable is involved: xx=0 and x+x=0. Wang algebra eases simplification of impedance networks, particularly when unknown internal nodes are involved. Matrix problems are particularly affected using Wang algebra. Bob provided an example where it reduced the matrix computations from 18 to 10 terms.

Bob used Wang algebra to illustrate solutions to problems involving the T-coil, an RLC circuit that assumes a constant R value. The t-coil can act as a compensator for capacitive loads in a distributed transmission line system. Usage includes designs by William Hewlett of HP fame. It is also used for phase delay equalization, including in oscilloscopes, plus compensation for bond wires in packages. Wang algebra makes t-coil analysis much easier, due to the assumption of constant equivalent R for the complete circuit.

Todd Westerhoff asked about the order of magnitude in the transmission line examples cited. Bob noted that this is physically large. Todd suggested that compensation may be done as part of the PCB structure or in metallization.

Arpad Muranyi asked about how Wang algebra can actually work, given that the two additional rules are not necessarily always true for an arbitrary system. Bob noted these assumptions are a subset of standard algebra rules that happen "to work out" due to simplifications that commonly occur as the equations are reduced.

IBIS-ATM UPDATE: SERDES MODELING IN IBIS

Todd Westerhoff, Signal Integrity Software (SiSoft)

Todd provided an overview of the work done by the Advanced Technology Modeling (ATM) Task Group within IBIS. Today, serial differential (SerDes) systems are more prevalent, with communications methods being applied to PCB signal integrity analysis. Most people are using a two-step process: first, an analog simulation, then a network computation is done separately. This means characterizing the driver, receiver and interconnect network first, either in time or frequency domain. This is followed by analyzing how the network responds to multiple bits, similar to a DSP, and equalization. Serial links require modeling of TX and RX equalization, prediction of link behavior, analysis of error rates and protection of IP.

The ATM group has been working on developing an interoperable standard for describing SerDes devices. The models are algorithms in binary code, operating on analog information derived from simulation. The interfaces for execution and parameters are also standard, to exchange parameter and waveform information between the model and tool. The two methods described in the proposed standard, INIT and GETWAVE, provide this framework for channel impulse response and continuous waveforms, respectively.

Today, the current version of the standard was taken from an original developed by Cadence and IBM. Many participants contributed. Presentations are on-line, including the draft BIRD and demonstration toolkits are also available. Participants are invited to submit comments, suggestions and test the toolkits.

One participant asked how the two steps are separated in a real situation. Todd clarified that network simulation is performed in an analog sense then processing is performed using algorithmic models and algorithms.

SERIAL LINK ANALYSIS AND PLL MODEL

ChunXing Huang, Huawei Technologies

ChunXing began by noting that serial link simulation technologies lag behind serial link development. SI engineers are struggling with models today to get reliable results. The purpose of simulation in most cases is to evaluate BER performance. Many designers are currently simulating with encrypted models. Areas such as FEC and data coding, plus jitter, DFE design, CDR/jitter at the receiver, etc. are not handled under current analog methods. As a result, encryption causes simulation slowdown, with 40 minutes required to get only 132 bits! The AMI proposal is a welcome advance in this case, and includes parameters for many critical effects, including jitter.

Jitter occurs in many forms, including power noise and phase noise of reference clocks or PLLs. Lab evaluation and final board designs may be significantly different so jitter measurements may be also different and must be simulated accordingly. Jitter sensitivity and jitter transfer function are the key parts of any PLL model. These noise factors are statistically independent. ChunXing showed examples from measurement of sensitivity and transfer functions. PI (power integrity) analysis can be used to create a PLL model and also its PD network, to examine noise effects. Methods of calculation for jitter have been suggested in specifications and industry conferences. ChunXing concluded by suggesting the IBIS community consider adding more support of PLL model jitter parameters in the AMI model standard.

A participant asked about what was missing regarding jitter in the AMI proposal. ChunXing answered that jitter information comes mostly from vendors for ICs, but we need to include values for the whole system, including the PLL models and algorithms, in the standard. System jitter values are missing today in AMI.

A REVIEW OF EXISTING MULTI-GBPS SERIAL CHANNEL ANALYSIS METHODS AND THE EVOLUTION OF THE PROPOSED ATM ALGORITHMIC MODELING STANDARD

Ian Dodd*, Richard Ward** and Sanjeev Gupta*, Agilent Technologies*, Texas Instruments**

Ian reviewed today's methods for analysis and drawing up standards for serial differential systems. Today's IEEE standards address ICs while IBIS addresses PCBs and systems. These may need to be combined in future, as they are arriving at complementary solutions for various parts of systems. Silicon vendor design RX and TX circuits using models of PCB interconnects, correlating to measurements to fine-tune the results. PCB vendors choose IC vendors and technology, laying out the channel and resimulating based on PCB measurements and other data.

IC vendors face a challenge, in that SPICE is preferred for easy modeling of devices. Vendors want to minimize costs and protect IP but SPICE may no longer be appropriate for multi-GHz simulations, and PCB vendors would like tool interoperability and high simulation speeds. Three options therefore remain: circuit-level simulations with IBIS/SPICE transistor-level, etc. with high accuracy but low performance. Second: IBIS/SPICE macromodels for devices, with C, AMS, etc. for more complex behaviors, preserving circuit level data for system and interconnect. Third method: simulate entirely at the system level, with no circuit data, even of interconnect. S-parameters or pulse response characterization would be used alone, instead of circuit-level interconnect descriptions. In addition, circuit and system level co-simulation represents a good hybrid, with examples such as the public-domain StatEye tool. ATM is a good option and start toward fast, interoperable device descriptions. However, it overlooks that most device designers actually create designs using RTL-oriented tools and flows. The standard does not support RTL directly, but requires it to be converted to C and then wrapped with the standard interface. ATM is also missing standard encryption for RTL code. The built-in drivers and receivers as used in StatEye are insufficient for today's complex and often proprietary designs – that is why we need a data exchange standard. Ian concluded by suggesting direct RTL code support in the ATM proposal.

AN OVERVIEW OF HIGH-SPEED SERIAL BUS SIMULATION TECHNOLOGIES

Arpad Muranyi, Vladimir Dmitriev-Zdorov, Mentor Graphics Corp.

Arpad provided a detailed overview of serial-differential analysis techniques. Most simulators and system designs use LTI (linear and time-invariant) assumptions for interface architecture and analysis, using fast algorithms (including superposition and convolution) to get quick worst-case responses. Worst-case eye openings can be obtained through superposition of eye widths of a UI as a single waveform and summing appropriately. Statistical eyes for BER (bit error ratio or rate) use the probability of each cursor combination to calculate the chance of interface failure.

Jitter and crosstalk must also be considered, including whether victims and aggressors are synchronized and including the self-response of the driver. Deterministic jitter can be included using statistical techniques, sometimes using a sinusoidal shape; for simplification, people use two pulse responses for this, but the accuracy is questionable. In a Gaussian distribution of probability, the tails of the distribution are where the eye can get closed down. For a worst-case bit pattern containing 50 pulses, the probability of finding the worst-case eye by applying a long random sequence would be 1 in 2^50 or less than 1 in 1e^15. The true worst-case pattern may occur more or less often depending on the tails of the PDF (probability distribution function).

Convolution-based algorithms are often used, but are limited by the length of the waveform used for the input. Fitted functions can be faster, are independent of waveform length and may have better dynamic range. Arpad suggested that the low-frequency response of a channel viewed in the AC domain can be analyzed to find resonances that may get missed in short, magnified impulse or pulse sequences.

Arpad also summarized equalization, including Finite Impulse Response (FIR) and Infinite Impulse Response (IIR). Both can be used for TX or RX designs. However, he cautioned that a feedback-type equalizer is non-linear compared to IIR and FIR. He concluded with a comparison of eye diagrams and BER bathtub curves for two types of feedback equalization.

MODELING AND SIMULATION FOR MULTI-GIGABIT INTERCONNECT SYSTEM

ShunLin Zhu, WeiDong Hu and Chen SongRui, ZTE Corp.

ShunLin began by noting that behavioral modeling is used increasingly for PCB analysis, but SPICE-level simulation is still popular for device design and analysis. Correlation is absolutely imperative, and simulations today should include probing structures and their loads. Pre-emphasis can be adequately modeled with SPICE macromodels in combination with IBIS, while ICM and S-parameters can be used for interconnects, packages and vias. Field solvers can be used to model board structures, with correlation data from VNAs or TDR. Complete systems can be correlated using PRBS patterns and complete SPICE system descriptions. ShunLin compared eye budgets in terms of Rj, Dj and Tj for two lengths of system interconnect, showing eye templates and diagrams for both. In the examples, deterministic jitter increased most as routing length increased.

POWER DELIVERY SYSTEM DESIGN AUTOMATION

Tao Xu, Sigrity

Tao reviewed how the PDS (power delivery system) of a platform can negatively influence signal quality and timing, noting that current increases and speed increases are driving a greater need for PDS analysis. Better system PDS performance comes from lower overall system input impedance looking “into” the system from the buffer, on the planes and power

delivery network itself (not the buffer). Analysis and cost optimization of a system PD network can be optimized using an automated flow, including physical stackup and layout, decap library, and the electrical data on the initial placement of caps or a target impedance for the network. This Z_target provides an optimization goal for the system and can be used to either reduce overall costs or find the lowest cost for increasing performance. Tao proposed adding Z_target to the IBIS specification, to cover PDS design goals.

In response to questions, Tao noted that the Z11 parameter could be used for deriving the input Z_target. The system expected rise time would define the frequency range or bandwidth, then chip manufacturers can supply power delivery targets for their designs.

IBIS 4.2 FOR DDR2 TIMING ANALYSIS

Tao Guan, Huawei Technologies

Tao began the presentation by noting that techniques like ODT (on-die termination) help memory interfaces address signal integrity issues at high speeds, they also pose problems for modeling. He suggested that today's simulation and modeling methods do not adequately support the kinds of analysis needed to ensure good SI. The key relationships in DDR2 timing analysis include address to command and CK, DQ and DQS plus DQS and CK. Unfortunately, the read and write timing analyses using today's techniques are often negative and therefore meaningless; also, these are time-consuming processes.

The IBIS problems for DDR2 include the fact that IBIS is not programmable and does not process slew rate tables automatically. Using methods suggested at earlier summits, Tao suggests using VHDL-AMS code under IBIS 4.2 to process DDR2 waveforms automatically. This permits fast computation of performance using the very complex DDR2 requirements. He concluded by suggesting that more tools should support VHDL-AMS and added that a SPICE2AMS tool is needed for IC vendors to convert device designs to AMS format.

VALIDATION FOR IBIS MODELS

Lance Wang, XinJun Zhang and Benny Yan, IO Methodology, Inc.

Lance reviewed current literature, noting that several quoted sources mentioned IBIS models available today as being not accurate. This is, in his view, not a specification problem but a model quality problem. The IBIS Quality Task Group has committed resources here, but the most important idea is to validate the models before using them. Lance showed several examples involving V-T tables and C_comp sweeps. While excellent correlation was shown between tools using the same IBIS model containing four V-T tables, correlation became much worse when a V-T table was removed. Sweeps of C_comp showed that some tools were using C_comp data in simulating IBIS models into a purely resistive load. Lance generalized, stating that cross-tool correlation is often needed to validate IBIS model performance, but that this could be too costly and time consuming for IBIS model users and authors. He then described a separate, private effort to provide free validation reports for IBIS models.

IBIS ALGORITHM INCLUDING REACTIVE LOADS

XueFeng Chen, Synopsys

XueFeng noted that IBIS permits V-T tables to use resistive, inductive and/or capacitive loads.

However, tools may not be able to use tables featuring anything other than resistive loads, as the equations to use them along with I-V tables do not have a unique solution for inductive or capacitive components. XueFeng showed a solution to this problem, where two additional differential equations are used and initial conditions are assumed. Correlation was significantly improved against transistor-level behavior.

Arpad Muranyi asked about series capacitors and whether these had been considered in deriving the new V-T table equations. XueFeng responded that this had not been considered.

UNDERSTANDING AND USING ICM MODELS

YuBao Meng, Cadence Design Systems

YuBao provided a brief review of the ICM (IBIS Interconnect Modeling) specification, including its support for both RLGC and S-parameter data. He showed three test cases where ICM can make interconnect modeling convenient: ICM for a package as a separate device in a topology (used as a connector, for example), ICM as an explicit package model, and ICM S-parameters used in either situation. Swathing was also described, as a means of compactly describing interconnects with repetitive coupling behaviors.

USING S-PARAMETERS FOR HIGH-PEFORMANCE SIMULATION

BaoLong Li, Ansoft

BaoLong reviewed S-parameter theory, showing that scattering parameters provide electrical descriptions of passive networks in the frequency domain over an arbitrary bandwidth. S-parameters can be used for direct analysis, or also in a time-domain analysis with reasonable correlation to other methods of description. For power planes and traces routed over non-ideal plane designs in particular, S-parameters can help optimize signal transmissions and reflections, to better target capacitor placement and remove discontinuities.

S-parameters can also be used to perform SSO analysis. However, problems can arise with S-parameters, particularly with non-causality and non-passivity as well as with non-convergence when used in time-domain simulations. State space representations can be used to address many of these problems.

ISSUES COMBINING BUFFER AND INTERCONNECT MODELS

Michael Mirmak, Intel Corp.

Michael summarized the state of today's industry in terms of the different model formats provided for packages, other interconnects and buffers. IBIS has attempted to include all competing buffer modeling formats available today, including Berkeley SPICE, Verilog-A, VHDL-AMS and Verilog-AMS, to ensure that their advantages and disadvantages offset within IBIS. Similarly, package and interconnect formats are proliferating, with ICM being the latest attempt to create a standard, tool-neutral approach to interconnect descriptions. Earlier board and package descriptions included in IBIS now fail, as they do not describe coupling or loss effectively for today's designs.

Tying all these formats together is the latest challenge, as IC vendors need to provide full simulation "decks" or working topologies to their customers to prove their designs in a full

system context. This often means using or supporting only one EDA tool, as no tool and no format can tie all the other buffer, package and interconnect formats together. Michael concluded by reviewing potential universal topology formats. At present, Verilog-A seems most promising but it does not contain a transmission line library or standard element, and does not directly support IBIS or ICM as elements. A standard SPICE, as proposed in an earlier summit, may be the most effective general solution, but much work will be needed to finalize it.

SERDES MODELING: IBIS-AMI EVALUATION TOOLKIT

Todd Westerhoff of Signal Integrity Software (SiSoft)

Due to time constraints, Michael Mirmak directed participants to view this material on their own. The presentation illustrates how to use an IBIS-ATM algorithmic model using a transmitter code example with equalization and sample impulse response waveforms.

IBIS AMI MODEL DEVELOPERS TOOLBOX

Hemant Shah of Cadence Design Systems

Due to time constraints, Michael Mirmak directed participants to view this material on their own. The presentation illustrates how to use an IBIS-ATM algorithmic model using a receiver code example with equalization and sample impulse response waveforms.

CONCLUDING ITEMS

Michael thanked the presenters, co-sponsors and attendees for their support and participation. Bob Ross, Arpad Muranyi and Todd Westerhoff presented Michael with an IBIS statue in observance of his running the meeting. The meeting adjourned at approximately 5:30 PM

NEXT MEETING

The next IBIS Open Forum Summit will be held in Tokyo, Japan on September 14. The next teleconference will be held September 21, 2007 from 8:00 AM to 10:00 AM US Pacific Time. Minutes may be delayed due to summit activities.

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NOTES

IBIS CHAIR: Michael Mirmak (916) 356-4261, Fax: (916) 377-3788
michael.mirmak@intel.com
Server Platform Technical Marketing Engineer, Intel Corporation
FM5-239
1900 Prairie City Rd.
Folsom, CA 95630

VICE CHAIR: Syed Huq (408) 525-3399, Fax: (408) 526-5504
shuq@cisco.com
Manager, Hardware Engineering, Cisco Systems
170 West Tasman Drive

San Jose, CA 95134-1706

SECRETARY: Randy Wolff (208) 363-1764, Fax: (208) 368-3475
rrwolff@micron.com
SI Modeling Manager, Micron Technology, Inc.
8000 S. Federal Way
Mail Stop: 01-711
Boise, ID 83707-0006

LIBRARIAN: Lance Wang (978) 633-3388
lwang@iometh.com
President / CEO, IO Methodology, Inc.
PO Box 2099
Acton, MA 01720

WEBMASTER: Syed Huq (408) 525-3399, Fax: (408) 526-5504
shuq@cisco.com
Manager, Hardware Engineering, Cisco Systems
170 West Tasman Drive
San Jose, CA 95134-1706

POSTMASTER: Bob Ross (503) 246-8048, Fax : (503) 239-4400
bob@teraspeed.com
Staff Scientist, Teraspeed Consulting Group
10238 SW Lancaster Road
Portland, OR 97219

This meeting was conducted in accordance with the GEIA Legal Guides and GEIA Manual of Organization and Procedure.

The following e-mail addresses are used:

majordomo@eda-stds.org
In the body, for the IBIS Open Forum Reflector:
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In the body, for the IBIS Users' Group Reflector:
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ibis-request@eda-stds.org
To join, change, or drop from either or both:
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IBIS Users' Group Reflector (ibis-users@eda-stds.org)
State your request.

ibis-info@eda-stds.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the EIA-IBIS Open Forum as a full Member.

ibis@eda-stds.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda-stds.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda-stds.org

To report ibischk parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda-stds.org/ibis/bugs/ibischk/
http://www.eda-stds.org/ibis/bugs/ibischk/bugform.txt

icm-bug@eda-stds.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda-stds.org/ibis/icm_bugs/
http://www.eda-stds.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda-stds.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda-stds.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda-stds.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eigroup.org/ibis/ibis.htm

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda-stds.org/ibis/directory.html

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GEIA STANDARDS BALLOT VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	July 13, 2007	August 3, 2007	August 24, 2007	September 11, 2007
Advanced Micro Devices	Producer	Inactive	√	√		
Agilent Technologies	User	Inactive	√			√
Ansoft	User	Inactive				√
Apple Computer	User	Inactive				
Applied Simulation Technology	User	Inactive				
Cadence Design Systems	User	Active	√	√	√	√
Cisco Systems	User	Active	√	√	√	√
Ericsson	Producer	Active	√		√	√
Freescale	Producer	Inactive				
Green Streak Programs	General Interest	Inactive				
Hitachi ULSI Systems	Producer	Inactive				√
Intel Corp.	Producer	Active	√	√	√	√
IO Methodology	User	Active	√	√		√
LSI Logic	Producer	Active		√	√	
Mentor Graphics	User	Active	√	√	√	√
Micron Technology	Producer	Inactive	√	√		
Nokia Siemens Networks	Producer	Inactive	√	√		
Panasonic	Producer	Inactive				
Samtec	Producer	Inactive				
Signal Integrity Software	User	Active			√	√
Sigrity	User	Active	√		√	√
STMicroelectronics	Producer	Inactive	√			
Synopsys	User	Inactive				√
Teraspeed Consulting	General Interest	Active	√	√	√	√
Texas Instruments	Producer	Inactive	√			
Toshiba	Producer	Inactive				
Xilinx	Producer	Inactive				
ZTE	User	Inactive				√
Zuken GmbH	User	Inactive				

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH GEIA BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
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