**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER:** 202.2 Draft 5

**ISSUE TITLE:** Electrical Descriptions of Modules

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**DATE ACCEPTED:**

**STATEMENT OF THE ISSUE:**

The industry lacks a method to describe modules that consist of one or more integrated circuits or other modules mounted on a printed circuit board, multi-chip module or substrate that connects them to a system through a set of pins. The following BIRD proposes a new type of file called .emd – Electrical Module Description (EMD) – that addresses this need.

**ANALYSIS PATH/DATA THAT LED TO SPECIFICATION:**

This BIRD has resulted from several years of discussion regarding the need for more flexible descriptions of module interconnects in IBIS. It was decided to avoid a keyword-based approach, in favor of a circuit language approach. IBIS-ISS was developed for this purpose, and a means to instantiate IBIS-ISS models from IBIS became the logical next step.

**SOLUTION REQUIREMENTS:**

The IBIS specification must meet these requirements:

Table 1: Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| * The model maker must be able to provide EMD Models representing modules, using a combination of IBIS-ISS and Touchstone formats.
 |  |
| * Touchstone models without an IBIS-ISS wrapper circuit must be supported.
 |  |
| * An EMD Model may connect one signal\_name or any combination of signal\_names in one [Begin EMD].
 | Coupled electrical paths are supported. |
| * IBIS component pin terminals associated with I/O pins must be assignable to EMD Model terminals directly by pin name.
 |  |
| * EMD pin terminals associated with POWER and GND rail pins must be assignable to EMD Model terminals directly by pin name, or indirectly by [Pin] signal\_name or bus\_label.
 |  |
| * The model maker must be able to provide alternative EMD Models for any given set of pins.
 | For example, for a given pin pair it must be possible to provide both coupled and uncoupled models, high and low bandwidth models, or both IBIS-ISS and Touchstone models. |
| * The EDA tool and model user must be able to locate all EMD Models that include a specified set of pins it must analyze.
 | Simulation netlisting begins with a list of pins that must be simulated. |
| * The EDA tool and model user must be able to determine all the pins that a given EMD Model includes.
 | Once a model is chosen, it may add more pins to the simulation. |
| * The EDA tool and model user must be able to determine how to terminate any terminals of an EMD Model not necessary for an analysis.
 | May need to handle Touchstone and IBIS-ISS models differently. |
| * The model user must have useful information needed to make the choice between alternative EMD Models that differ only in characteristics other than the model format and the set of pins included.
 | For example: coupled/uncoupled, low/high bandwidth. This will be used to choose which alternative model set to use. |
| * The model user must be informed which pins of an EMD Model have been modeled with coupling to other pins, sufficient to represent the victim pins and all the aggressor pins in a crosstalk simulation.
 |  |

**BACKGROUND INFORMATION/HISTORY:**

STATEMENT OF THE RESOLVED SPECIFICATIONS:

**Under Section 3, First Paragraph**

REPLACE

Unless noted otherwise, this section contains general syntax rules and guidelines for IBIS file formats .ibs (Sections 4, 5, 6 and 12), .pkg (Section 7), .ebd (Section 8), .ims (Section 11), and where applicable, .ami (Sections 10.3 through 10.11) and parameter passing files (Section 6.3).

WITH (adding .emd, .ems):

Unless noted otherwise, this section contains general syntax rules and guidelines for IBIS file formats .ibs (Sections 4, 5, 6 and 12), .pkg (Section 7), .ebd (Section 8), .ims (Section 11), .emd (Section 12), .ems (Section 13), and where applicable, .ami (Sections 10.3 through 10.11) and parameter passing files (Section 6.3).

**ADD to Section 3.3 Keyword Hierarchy:**

.emd FILE

 ├── File Header Section

 │ ├── **[IBIS Ver]**

 │ ├── **[Comment Char]**

 │ ├── **[File Name]**

 │ ├── **[File Rev]**

 │ ├── **[Date]**

 │ ├── **[Source]**

 │ ├── **[Notes]**

 │ ├── **[Disclaimer]**

 │ └── **[Copyright]**

 │

 ├── **[Begin EMD]**

 │ ├── **[Manufacturer]**

 │ ├── **[Description]**

 │ ├── **[Number of EMD Pins]**

 │ ├── **[EMD Pin List]** signal\_name, signal\_type

 │ │ │bus\_label

 │ │ └── **[End EMD Pin List]**

 │ │

 │ ├── **[EMD Parts]**

 │ │ └── **[End EMD Parts]**

 │ │

 │ ├── **[EMD Designator List]**

 │ │ └── **[End EMD Designator List]**

 │ │

 │ ├── **[Designator Pin List]** signal\_name, signal\_type

 │ │ │ bus\_label

 │ │ └── **[End Designator Pin List]**

 │ │

 │ ├── **[Voltage List]**

 │ │ └── **[End Voltage List]**

 │ │

 │ ├── **[EMD Group]**

 │ │ └── **[End EMD Group]**

 │ │

 │ └── **[End EMD]**

 │

 ├── **[EMD Set]**

 │ ├── **[Manufacturer]**

 │ ├── **[Description]**

 │ ├── **[EMD Model]** Param, File\_TS, File\_IBIS-ISS,

 │ │ │ Unused\_port\_termination,

 │ │ │ Number\_of\_terminals

 │ │ └── **[End EMD Model]**

 │ │

 │ └── **[End EMD Set]**

 │

 └── **[End]**

.ems FILE

 ├── File Header Section

 │ ├── **[IBIS Ver]**

 │ ├── **[Comment Char]**

 │ ├── **[File Name]**

 │ ├── **[File Rev]**

 │ ├── **[Date]**

 │ ├── **[Source]**

 │ ├── **[Notes]**

 │ ├── **[Disclaimer]**

 │ └── **[Copyright]**

 │

 ├── **[EMD Set]**

 │ ├── **[Manufacturer]**

 │ ├── **[Description]**

 │ ├── **[EMD Model]** Param, File\_TS, File\_IBIS-ISS,

 │ │ │ Unused\_port\_termination,

 │ │ │ Number\_of\_terminals

 │ │ └── **[End EMD Model]**

 │ │

 │ └── **[End EMD Set]**

 │

 └── **[End]**

**In Section 4:**

REPLACE

*Keyword:* [File Name]

*Required:* Yes

*Description:* Specifies the file name of the file containing this keyword.

*Usage Rules:* The file name shall conform to the rules in item 3 of Section **Error! Reference source not found.**.2, "SYNTAX RULES". In addition, the file name shall use the extension “ibs”, “pkg”, “ebd”, or “ims”. The file name shall be the actual name of the file.

*Example:*

[File Name] ver6\_1.ibs

*Keyword:* [File Rev]

*Required:* Yes

*Description:* Tracks the revision level of a particular .ibs, .pkg, .ebd, or .ims file.

*Usage Rules:* Revision level is set at the discretion of the engineer defining the file. The following guidelines are recommended:

0.x silicon and file in development

1.x pre-silicon file data from silicon model only

2.x file correlated to actual silicon measurements

3.x mature product, no more changes likely

*Example:*

[File Rev] 1.0 | Used for .ibs file variations

WITH (adding .emd, .ems)

*Keyword:* [File Name]

*Required:* Yes

*Description:* Specifies the file name of the file containing this keyword.

*Usage Rules:* The file name shall conform to the rules in item 3 of Section **Error! Reference source not found.**.2, "SYNTAX RULES". In addition, the file name shall use the extension “ibs”, “pkg”, “ebd”, “ims”, “emd”, or “ems”. The file name shall be the actual name of the file.

*Example:*

[File Name] ver7\_1.ibs

*Keyword:* [File Rev]

*Required:* Yes

*Description:* Tracks the revision level of a particular .ibs, .pkg, .ebd, .ims, .emd, or .ems file.

*Usage Rules:* Revision level is set at the discretion of the engineer defining the file. The following guidelines are recommended:

0.x silicon and file in development

1.x pre-silicon file data from silicon model only

2.x file correlated to actual silicon measurements

3.x mature product, no more changes likely

*Example:*

[File Rev] 1.0 | Used for IBIS file variations

**In Section 6.3.6 :**

REPLACE

file formats except .ami (e.g., .ibs, .pkg, .ebd and .ims)

WITH (pages 118, 119, 139, 140)

file formats except .ami (e.g., .ibs, .pkg, .ebd, .ims, .emd, and .ems)

**Move Section 12 to Section 14 and Add a New Section 12:**

**12 ELECTRICAL MODULE DESCRIPTION (EMD)**

**INTRODUCTION**

 “Module” is a generic term describing a printed circuit board (PCB), multi-chip module (MCM), stacked die component, interposer, or substrate which can contain components or other modules, and which can connect to another board or module through a set of user-visible pins. For example, a DIMM module is a module-level component that is used to attach several DRAM components on the PCB to another module through edge connector pins. The electrical connectivity of such a board or module-level component is described through an “Electrical Module Description”. An [EMD Model] defines an electrical model of the interconnect between the external pin(s) of the module (referred to elsewhere as “EMD pins”) and the pin(s) of the designator(s) in the module (referred to elsewhere as “designator pins”).  A designator name or set of names (e.g., U23, U24) is associated with distinct part names; this association is defined using the [EMD Designator List] keyword.  Each part name is associated with a component in an IBIS (.ibs) file or a module in an EMD (.emd) file; this association is defined using the [EMD Parts] keyword.  For designators, the user-visible designator pins are listed under the [Designator Pin List] keyword.  Other details are described later.

I/O pins in the [EMD Pin List] and the Designator Pin List that have the same signal\_name are considered “connected” by the content of the [EMD Model]. Rail pins in the EMD Pin List and the Designator Pin List that have the same signal\_name (or, as applicable, bus\_label) are considered connected. This assumption is due to the expectation that some EMD files will be generated automatically from computer aided design (CAD) layout databases. Each pin in a CAD database is assigned with a CAD “net” (short for “network”) name, and when two pins are assigned with the same CAD net name, they are considered connected. Normally, the signal\_name of EMD pins and designator pins will be the same as their assigned CAD net name in the layout database. An exception to this is when there are series terminations. In this case the model maker can choose to either:

1. Combine two CAD nets into an “extended net”. All the pins in the two CAD nets will use the extended net name as their signal\_name in the EMD file. The termination resistor or capacitor would be included in the EMD Models for this extended net. An extended net is defined as the list of EMD and designator pins associated with a common path through an EMD Model.
2. Create separate EMD Models for each CAD net. The termination component must be assigned a designator in this case.

What is and is not included in an EMD Model is defined by its boundaries, referred to here as interfaces. Interfaces exist at the EMD Pin List and Designator Pin List levels.

Terminals are the connection points to IBIS-ISS terminals, Touchstone ports, IBIS Pins, or other EMD Pins defined in each EMD Model. Terminal lines describe the IBIS-ISS terminal or Touchstone port to which each terminal of an EMD Model is connected. Terminals exist at [EMD Pin List] and [Designator Pin List] interfaces.

**EMD Files**

s

Usage Rules:

A .emd file is intended to be a stand-alone file, not referenced by or included in any .ibs, .ebd, or .pkg file. Electrical Module Descriptions are stored in a file whose name is <stem>.emd, where <stem> must conform to the naming rules given in Section **Error! Reference source not found.** of this specification. The emd extension is mandatory.

Contents:

A .emd file is structured like a standard .ibs file. It must contain the following keywords, as defined in IBIS: [IBIS Ver], [File Name], [File Rev], and [End]. It may also contain the following optional keywords: [Comment Char], [Date], [Source], [Notes], [Disclaimer], and [Copyright].

The actual module description is contained between the keywords [Begin EMD] and [End EMD], and includes the keywords listed below:

.emd file keywords

[Begin EMD]

[Manufacturer]

[Description]

 [Number Of EMD Pins]

[EMD Pin List]

[End EMD Pin List]

      [EMD Parts]

[End EMD Parts]

      [EMD Designator List]

[End EMD Designator List]

 [Designator Pin List]

[End Designator Pin List]

[Voltage List]

[End Voltage List]

[EMD Group]

[End EMD Group]

[End EMD]

[EMD Set] [EMD Set] keywords permitted within a .emd file and covered later

[Manufacturer]

[Description]

      [EMD Model]

      [End EMD Model]

[End EMD Set]

**KEYWORD DEFINITIONS**

 module

*Keyword:* [Manufacturer]

*Required:* Yes

*Description:* Declares the manufacturer of the module that uses this .emd file.

*Usage Rules:* Following the keyword is the manufacturer’s name. It must not exceed 40 characters and can include blank characters. Each manufacturer must use a consistent name in all .emd files.

*Example:*

[Manufacturer] Quality SIMM Corp.

*Keyword:* [Description]

*Required:* No

*Description:* Provides a concise explanation of what kind of interconnect the EMD represents.

*Usage Rules:* The text shall fit on a single line and may contain spaces.

*Example:*

[Description] 6-Pin Quad Ceramic Flat Pack

*Keyword:* [Number Of EMD Pins]

*Required:* Yes

*Description:* Defines the number of EMD pins, which shall match the number of pins found in the [EMD Pin List] keyword. EMD pins are any externally accessible electrical connection to the module.

*Usage Rules:* The field must be a positive integer. The [Number Of EMD Pins] keyword must be positioned before the [EMD Pin List] keyword.

*Example:*

[Number Of EMD Pins] 128

*Keyword:* [EMD Pin List]

*Required:* Yes

*Description:* Defines the pin names of the user accessible pins. It also defines which pins are connected to power and ground.

*Sub-Params:* signal\_name, signal\_type, bus\_label

*Usage Rules:* The [EMD Pin List] keyword shall be followed by the subparameter names “signal\_name”, “signal\_type”, and “bus\_label”, serving as column headings. The keyword and the list of its subparameters shall be followed by as many rows of information as the number of EMD pins declared by the preceding [Number Of EMD Pins] keyword. Each row may contain up to four columns of information.

The first two columns are required on each row for each pin type.

The first column lists the pin name (in the data book this can also be called pin number). Each pin\_name entry must be unique, i.e., duplicate pin names are not permitted. Pin names must be the alphanumeric external pin names of the module. The pin\_name entry shall not exceed eight characters in length. All non-rail pins (generically referred to as I/O pins) are required to be listed.

The second column (signal\_name) lists the name of the signal connected to that pin. The signal\_name entries are not required to be unique for each row. Also, these signal\_name entries may be different from the signal\_names found under the designator .ibs [Component] or the designator .emd [Begin EMD] keywords. This allows the interchange of attached components or attached electrical module descriptions with standardized pin\_name positions but with different manufacturer naming conventions. All EMD pins and designator pins that have the same signal\_name are considered to be part of the same electrical net. The signal\_name entry may also be used to signify the primary connection to other I/O pins (necessary for Aggressor\_Only described later).

I/O pins shall consist of exactly two columns containing the pin\_name and signal\_name entries. No signal\_type or bus\_label entry is permitted for I/O pins.

The third column (signal\_type) is required for rail pins and no-connect pins. The allowed values for this third column (as defined in Section 3.2) are:

POWER - reserved model name, used with power supply pins

GND - reserved model name, used with ground pins

NC - reserved model name, used with no-connect pins

“NC” is a legal signal\_type and indicates that the pin is a “no-connect”. As described in Section 3.2 the reserved words “GND”, “POWER”, and “NC” are case-insensitive.

The fourth column (bus\_label) is optional for rail pins (signal\_type POWER or GND). The bus\_label entry is a name assigned to a subset of the pins with a rail signal\_name. As its name implies, bus\_label entries are not required to be unique for each row. However, all pins that have the same bus\_label must have the same signal\_name. If the bus\_label column is not specified for signal\_type POWER or GND, then the bus\_label shall be assumed to be the signal\_name.

Multiple rail pins may be merged into a single [EMD Model] terminal using the terminal line syntax of the [EMD Model] keyword. This merged terminal combines all the rail pins with the same signal\_name on the same interface, or all of the rail pins with the same bus\_label on the same interface. In this case, all the pins that are merged into a single terminal are “shorted”.

*Example:*

| A SIMM Module Example:

|

[Begin EMD] 16X8\_SIMM

[Manufacturer] Quality SIMM Corp.

[Number Of Pins] 6

[EMD Pin List] signal\_name signal\_type bus\_label

A1 GND GND

A2 DQ1 | I/O pin

A3 DQ2 | I/O pin

A4 POWER5 POWER Power5x

A5 RFU NC

A6 POWER3.3 POWER

[End EMD Pin List]

*Keyword:* **[End EMD Pin List]**

*Required:* Yes

*Description:* Indicates the end of the data after [EMD Pin List].

*Example:*

[End EMD Pin List]

*Keyword:* **[**EMD Parts]

*Required:* No

*Description:* Maps an EMD part\_name to an IBIS component or EMD module.

*Usage Rules:* The [EMD Parts] keyword shall be followed by a list of all the EMD parts (also called part numbers or part names in industry).Each EMD part\_name entry in the list is followed by the file reference of the .ibs or .emd file containing the electrical description of the component or board, then the name of the component itself as given by the .ibs or .emd file’s [Component] or [Begin EMD] keyword respectively.  Official names of parts is recommended, but not required. The referenced .ibs or .emd files shall exist in the same directory as the calling .emd file or shall exist in a relative path under this directory.

A .emd file that describes a part can itself reference other EMD modules. No more than six levels of hierarchy for nested .emd files are permitted. A .emd file shall not reference itself directly or indirectly.

The EMD part\_name entry, file reference, and component/module name terms are separated by white space. The EMD part\_name entry is limited to forty characters.

A part\_name entry shall be listed only once.

NAs in the file reference and component/module name columns are permitted if the part has functionality outside of the scope of the IBIS specification, such as certain analog parts. The NA in the file reference column indicates that the part model is not fully available. However, its designator shall be included under the [EMD Designator List] keyword, and its pinout shall be included as [Designator Pin List] keyword entries described below.

*Other Notes:* It is permitted to use a .ibs file or .emd file and a component or module name to show the part pinout and to document some known rails and digital I/O pins that are supported by the IBIS specification. Pins whose functions are not supported by the IBIS specification could be documented as “NC” pins or with Terminator models within these .ibs or .emd files.

A [Notes] section or a separate readme file should document these unknown parts or parts where certain pins cannot be modeled in IBIS. Some EDA tools may deal with these special cases in a tool-specific manner.

The [EMD Parts] keyword may be omitted if there are no EMD parts on the EMD module, such as in the case of a backplane or loopback board.

*Example:*

[EMD Parts]

|

| part\_name file\_reference component/module name

Processor pp100.ibs Processor

Memory\_16X8 simm.emd 16X8\_SIMM

74LS244 ls244.ibs NoName\_74LS244

Res\_10K r10K.ibs My\_10K\_Pullup

|

ABC NA NA | Undocumented Parts

BCD NA NA | without files

|

C555 timer.ibs X555 | Timer with digital control

|

[End EMD Parts]

*Keyword:* **[End EMD** Parts**]**

*Required:* Yes, if [EMD Parts] is present

*Description:* Indicates the end of the data after [EMD Parts].

*Example:*

[End EMD Parts]

*Keyword:* **[**EMD Designator List]

*Required:* Yes, if [EMD Parts] is present

*Description:* Maps an EMD designator to an IBIS or EMD part name.

*Usage Rules:* The [EMD Designator List] keyword must be followed by a list of all the EMD designators (also called reference designators in industry). Each EMD designator is followed by a part name.

For the context in thisElectrical Module Description section, a “designator” shall be the first column in the data following [EMD Designator List].

The EMD designator and part name are separated by white space.

The EMD designator is limited to ten characters. “\*” is an illegal designator name.

*Example:*

[EMD Designator List]

|

| EMD Designator Part Name

u23 Processor

u24 Memory\_16X8

u25 74LS244a

u26 Res\_10K

[End EMD Designator List]

*Keyword:* **[End EMD Designator List]**

*Required:* Yes, if [EMD Designator List] is present

*Description:* Indicates the end of the data after [EMD Designator List].

*Example:*

[End EMD Designator List]

*Keyword:* [Designator Pin List]

*Required:* Yes, if [EMD Designator List] is present

*Description:* Defines the pin names of the designator pins. It also defines which designator pins are connected to power or ground. Designators are defined in the [EMD Designator List] section and can be instances of either a .ibs [Component] or a .emd [Begin EMD].

*Sub-Params:* signal\_name, signal\_type, bus\_label

*Usage Rules:* The [Designator Pin List] keyword shall be followed by the subparameter names “signal\_name”, “signal\_type”, and “bus\_label”, serving as column headings. The keyword and the list of its subparameters shall be followed by as many rows of information as the combined number of pins found in all of the designators listed under the [EMD Designator List] keyword. All pin\_name pins for each designator are required to be listed. Each row may contain up to four columns of information.

The first two columns are required on each row for each pin type.

The first column must contain the alphanumeric external pin\_names of the designator. The pin\_name entry shall be preceded by the reference designator followed by a “.” (e.g., U2.DQ1). Each pin\_name entry must be unique, i.e., duplicate pin names are not permitted. The pin\_name entry shall not exceed eight characters in length.

The second column (signal\_name) lists the name of the signal connected to that pin. The signal\_name entries are not required to be unique for each row. Also, these signal\_name entries may be different from the signal\_names found under the designator .ibs [Component] or the designator .emd [Begin EMD] keywords. This allows the interchange of attached components or attached electrical module descriptions with standardized pin\_name positions but with different manufacturer naming conventions. All EMD pins and designator pins that have the same signal\_name are considered to be part of the same electrical net.

I/O pin entries shall consist of exactly two columns containing the pin\_name and signal\_name entries. No signal\_type or bus\_label entry is permitted for I/O pins. The signal\_name entry may also be used to signify the primary connection to other I/O pins (necessary for Aggressor\_Only described later).

The third column (signal\_type) is required for rail pins. The allowed values for this third column (as defined in Section 3.2) are:

POWER - reserved model name, used with power supply pins

GND - reserved model name, used with ground pins

As described in Section 3.2 the reserved words “GND” and “POWER” are case-insensitive.

The fourth column (bus\_label) is optional for rail pins (signal\_type POWER or GND). The bus\_label entry is a name assigned to a subset of the pins with a rail signal\_name. As its name implies, bus\_label entries are not required to be unique for each row. However, all pins that have the same bus\_label must have the same signal\_name. If the bus\_label column is not specified for signal\_type POWER or GND, then the bus\_label shall be assumed to be the signal\_name.

Multiple rail pins may be merged into a single [EMD Model] terminal using the terminal line syntax of the [EMD Model] keyword. This merged terminal combines all the rail pins with the same signal\_name on the same interface, or all of the rail pins with the same bus\_label on the same interface. In this case, all the pins that are merged into a single terminal are “shorted”.

*Example:*

| A SIMM Module Example:

|

[Begin EMD] 16X8\_SIMM

[Manufacturer] Quality SIMM Corp.

[Number Of EMD Pins] 6

[EMD Pin List] signal\_name signal\_type bus\_label

A1 VSS GND

A2 DQ1 | I/O pin

A3 DQ2 | I/O pin

A4 VDD POWER VDD1

A5 VDD POWER VDD2

A6 VDDQ POWER

[End EMD Pin List]

[Designator Pin List] signal\_name signal\_type bus\_label

U1.11 VSS GND

U1.12 DQ1 | I/O pin

U1.13 DQ2 | I/O pin

U1.14 VDD POWER VDD1

U2.21 VDD POWER VDD2

U2.22 DQ1 | I/O pin

U2.23 DQ2 | I/O pin

U2.24 VDDQ POWER

[End Designator Pin List]

*Keyword:* **[End Designator Pin List]**

*Required:* Yes, if [Designator Pin List] is present

*Description:* Indicates the end of the data after [Designator Pin List].

*Example:*

[End Designator Pin List]

*Keyword:* [Voltage List]

*Required:* No

*Description:* Defines the signal\_names or bus\_labels that are rail signals, as well as their voltage values.

*Usage Rules:* Under the [Voltage List] keyword are four columns:

The first column lists the voltage rail name of a signal\_name or a bus\_label found within EMD Pin List or Designator Pin List.

The second column, V(typ), lists the typ value of the voltage. This entry is required.

The third column, V(min), lists the min (by magnitude) value of the voltage. If missing, ‘NA’ is entered, and the default value is V(typ).

The fourth column, V(max), lists the max (by magnitude) value of the voltage. If missing, ‘NA’ is entered, and the default value is V(typ).

Not all voltage rail names of signal\_names or bus\_labels found within EMD Pin List or Designator Pin List are required to be listed.

*Other Notes:* This keyword can be used in several ways:

* Provides information about expected voltage source values at EMD Pin List and Designator Pin List interfaces for any or all the rail signals. The EDA tool can override these values. This might occur in the following cases:
	+ With a SPICE netlist that provides its own sources
	+ If V(min) and V(max) values are not supplied (as might occur with a SPICE netlist and its sources)
	+ With [Model] corner setting using the typ, min, and max sources that are declared within the [Model] keyword
* Declares external sources at the EMD Pin List and/or Designator Pin List interfaces for the named voltages.

Because the [Voltage List] entries may be incomplete or because V(min) and/or V(max) values may be omitted, combinations of the above options are permitted.

In simulation, [Voltage List] entries shall be selected along with the corresponding corner values in [Model] entries. That is, V(typ) values should be used with typ corner conditions, V(min) with min corner conditions, and V(max) with max corner conditions.

In a power aware simulation, voltages will be supplied by the EDA tool at the EMD pins from voltage sources in the board or module that uses the EMD.

*Example:*

[Voltage List]

| V(name) V(typ) V(min) V(max)

VSS 0.0 0.0 0.0

VDD 1.2 1.1 1.3

[End Voltage List]

*Keyword:* [**End Voltage List**]

*Required:* Yes

*Description:* Indicates the end of the data after [Voltage List].

*Example:*

[End Voltage List]

*Keyword:* [EMD Group]

*Required:* Yes

*Description:*  [EMD Group] has a single argument, which is the name of the associated EMD Group. The length of the EMD Group name shall not exceed 40 characters. Blank characters are not allowed. The [EMD Group]/[End EMD Group] keyword pair is hierarchically scoped by the [Begin EMD]keyword. The [EMD Group] keyword is used to define a list of [EMD Set]s by name that shall be used together to define EMD Models to be used in a simulation. A simulation may contain EMD Models from the EMD Sets listed in only one EMD Group.

*Usage Rules:* [Begin EMD] must contain one or more [EMD Group] keywords (identified by a name). Each [EMD Group] must contain at least one [EMD Set] name. EMD Sets contain EMD Models used to describe EMD pin or IBIS designator pin connections to IBIS-ISS subcircuits or n-port networks described by Touchstone files.

EMD Sets that exist for the module shall be listed in one or more EMD Groups. An EMD Group is required even if it references only one EMD Set.

The section under the [EMD Group] keyword shall have two entries per line, with each line identifying one EMD Set associated with the module. The entries shall be separated by at least one white space. The first entry lists the EMD Set name (up to 40 characters long). The second entry is the file reference of the file containing the EMD Set and shall have the extension “ems”. This file reference shall conform to the rules given in Section 3, ‘GENERAL SYNTAX RULES AND GUIDELINES’. If the EMD Set is in the same .ibs file as [Begin EMD], then the second entry shall be “NA”.

The files containing the EMD Sets with the “ems” extension shall be located in the same directory as the .emd file or in a specified directory under the .emd file as determined by the directory path according to the file name rules given in Section 3, ’GENERAL SYNTAX RULES AND GUIDELINES’ (i.e., a file reference containing a relative path to a directory below that of the referencing .emd file is permitted). An EMD Set with matching name shall be found in the stated location for each EMD Set named in the [EMD Group] keyword.

Each EMD Set name and its file\_reference may only appear once under each [EMD Group] keyword for a given designator.

Refer to Section 13.6 for connection rules and limitations on the permissible EMD Set links under each [EMD Group] keyword and after some more terms and rules related to [EMD Set] and [EMD Model] keywords are defined.

*Examples:*

| Example 1

|

[EMD Group] Full\_ISS\_PDN\_1

| EMD Set file\_reference

Full\_ISS\_PDN\_1 NA | The [EMD Set] is

 | present in the .emd file for

 | all pins

[End EMD Group]

|

| Example 2

|

[EMD Group] Full\_ISS\_PDN\_sn\_2

| EMD Set file\_reference

Full\_ISS\_PDN\_sn\_2 NA | The [EMD Set] is

 | present in the .emd file for

 | all I/O pins and PDN

[End EMD Group]

*Keyword:* **[End EMD Group]**

*Required:* Yes, for each instance of the [EMD Group] keyword

*Description:* Indicates the end of the data for one [EMD Group].

*Example:*

[End EMD Group]

*Keyword:* [End EMD]

*Required:* Yes

*Description:* Marks the end of an electrical module description.

*Usage Rules:* This keyword shall be placed at the end of each complete electrical module description.

*Example:*

[End EMD]

**13 EMD SET AND EMD MODEL DESCRIPTION**

**13.1 EMD SET KEYWORD DESCRIPTION**

*Keyword:* [EMD Set]

*Required:* Yes

*Description:* Used to contain EMD Models

*Usage Rules:* [EMD Set] has a single argument, which is the name of the EMD Set. The length of the EMD Set name shall not exceed 40 characters. Blank characters are not allowed. The [EMD Set]/[End EMD Set] keyword pair is hierarchically equivalent in scope to [Begin EMD].

The section under the [EMD Set] keyword may contain a [Manufacturer] keyword section and [Description] keyword section and shall contain one or more EMD Models. See the section [EMD Model] for a description of the content of each EMD Model.

An EMD Set contains a list of EMD Models that have a logical association such as:

* All signals in a bus (e.g., DDR4, or PCIe)
* Full Power Delivery Network (PDN) structures from EMD pins to designator pins
* Full PDN structures from EMD pins to EMD pins
* All I/O structures between EMD pins and designator pins
* I/O structures from designator pins to designator pins
* Combinations of I/O and PDN structures
* Coupled models
* Touchstone electrical models
* Decoupling capacitor models
* IBIS-ISS electrical models

*Example:*

[EMD Set] Signal\_Integrity

[Manufacturer] Acme Packaging, Inc.

[Description] This set contains one model for each I/O buffer

[EMD Model] DQ1

…

[End EMD Model]

[EMD Model] DQ2

…

[End EMD Model]

[EMD Model] DQS

…

[End EMD Model]

[End EMD Set]

*Keyword:* [Manufacturer]

*Required:* No

*Description:* Declares the manufacturer of the module that uses this .emd file.

*Usage Rules:* Following the keyword is the manufacturer’s name. It must not exceed 40 characters and can include blank characters. Each manufacturer must use a consistent name in all .emd files.

*Example:*

[Manufacturer] Quality SIMM Corp.

*Keyword:* [Description]

*Required:* No

*Description:* Provides a concise yet easily human-readable description of what kind of interconnect the [EMD Set] represents.

*Usage Rules:* The description shall fit on a single line and may contain spaces.

*Example:*

[Description] 6-Pin Quad Ceramic Flat Pack

*Keyword:* [**End EMD Set**]

*Required:* Yes, for each instance of the [EMD Set] keyword.

*Description:* Indicates the end of the EMD Set data.

*Example:*

[End EMD Set]

**13.2 GENERAL EMD SET AND EMD MODEL FILE SYNTAX REQUIREMENTS**

One or more EMD Sets may be included in a separate EMD Set file, using a file name with the extension “ems”, or within the .emd file. The [EMD Set] keyword can contain the optional [Manufacturer] and [Description] keywords and one or more [EMD Model] keywords and the [EMD Model] associated subparameters, as listed in Table 40.

TableError! Reference source not found. 40 – EMD Set and EMD Model Keywords and Subparameters

| **Keyword or Subparameter** | **Notes** |
| --- | --- |
| [EMD Set] |  |
| [Manufacturer] | (note 1) |
| [Description] | (note 1) |
| [EMD Model] | (note 2) |
| Param |  |
| File\_TS | (note 3) |
| File\_IBIS-ISS | (note 3) |
| Unused\_port\_termination | (note 4) |
| Number\_of\_terminals | (note 5) |
| <terminal line> | (note 6) |
| [End EMD Model] | (note 7) |
| [End EMD Set] | (note 8) |
| Note 1 [Manufacturer] and [Description] are each optional keywords within any [EMD Set].Note 2 At least one [EMD Model] is required for each [EMD Set].Note 3 One of either the File\_TS or File\_IBIS-ISS subparameters is required.Note 4 This subparameter shall be followed by the “=” character and a numeric value (integers and reals are acceptable), with both optionally surrounded by whitespace.Note 5 This subparameter shall be followed by the “=” character and an integer value, with both optionally surrounded by whitespace.Note 6 See Section 13.3 below.Note 7 Required when the [EMD Model] keyword is used.Note 8 Required when the [EMD Set] keyword is used. |

When EMD Set definitions occur within a .emd file, their scope is “local”— they are known only within that .emd file and no other .emd file.

Usage Rules for the .ems file:

EMD Models are stored in a file whose file name uses the format:

<stem>.ems

The <stem> provided shall adhere to the rules given for the [File Name] keyword. Use the “ems” extension to identify files containing EMD Models. The .ems file shall contain the [IBIS Ver], [File Name], [File Rev], and the [End] keywords. Optional elements include the [Date], [Source], [Notes], [Disclaimer], [Copyright], and [Comment Char] keywords. All these keywords and associated subparameters follow the same rules as those for a normal .ibs file.

**13.3 GENERAL EMD MODEL KEYWORD DESCRIPTION**

*Keyword:* [EMD Model]

*Required:* Yes

*Description:* Marks the beginning of the definition of the electrical model of the interconnect between the external pin(s) of the module and the pin(s) of the designator(s) in the module.

*Sub-Params:* Unused\_port\_termination, Param, File\_TS, File\_IBIS-ISS, Number\_of\_terminals

*Usage Rules:* [EMD Model] has a single argument, which is the name of the associated EMD Model. The length of the EMD Model name shall not exceed 40 characters. Blank characters are not allowed. The [EMD Model]/[End EMD Model] keyword pair is hierarchically scoped by the [EMD Set]/[End EMD Set] keywords.

The [EMD Model]/[End EMD Model] section defines both the association between a Touchstone file or IBIS-ISS subcircuit and an EMD Model, as well as defining the terminals and terminal usage for the EMD Model in the context of the given [Begin EMD].

An [EMD Model] may contain terminals from one or more interfaces including those listed in the [EMD Pin List] and/or those listed in the [Designator Pin List].

An [EMD Model] may contain terminals in the following combinations:

* one or more rails only
* one or more I/O signals
* one or more rails and one or more I/O signals
* one or more rails at the EMD Pin List interface only
* one or more rails at the Designator Pin List interface only

The following subparameters are defined:

Param

File\_IBIS-ISS

File\_TS

Unused\_port\_termination

Number\_of\_terminals = <value>

In addition to these subparameters, the [EMD Model]/[End EMD Model] section may contain lines describing terminals and their connections. No specific subparameter name or other string is used to identify terminal lines.

Unless noted below, no EMD Model subparameter requires the presence of any other subparameter.

Param rules:

The subparameter Param is optional and only legal with the File\_IBIS-ISS subparameter documented below. Param is illegal with the File\_TS subparameter documented below. Param shall be followed by three arguments: an unquoted string argument giving the name of the parameter to be passed into the IBIS-ISS subcircuit, a reserved word for the parameter format, and one numerical value or one string value (surrounded by double quotes) for the parameter value to be passed into the IBIS-ISS subcircuit.

The numerical value rules follow the scaling conventions in Section 3.2, “SYNTAX RULES”. The EDA tool is responsible for translating IBIS specified parameters into IBIS-ISS parameters. For example, 1 megaohm, would be represented as 1M in Param value according to the Section 3 rules, but would be converted by the EDA tool to case-insensitive 1meg (1X is not recommended) or 1E6 for IBIS-ISS use. Quoted string parameters in IBIS are converted to the string parameter syntax in IBIS-ISS subcircuits. For example, the Param value "typ.s2p" would be converted to str('typ.s2p') in IBIS-ISS subcircuits.

*Examples:*

| Param name format value

Param abc Value 2m | 2E-3 in IBIS

Param def Value 4k | 4E3 in IBIS

Param ts\_file Value "typ.s2p" | file name string passed

 | into IBIS-ISS

File\_IBIS-ISS rules:

Either File\_IBIS-ISS or File\_TS is required for a [EMD Model]/[End EMD Model] group*.* The File\_IBIS-ISS subparameter is followed by two unquoted string arguments consisting of the file\_reference and circuit\_name (.subckt name) for an IBIS-ISS file. The IBIS-ISS file under file\_reference shall be located in the same directory as the referencing .emd file or .ems file or in a specified directory under the referencing file as determined by the directory path (i.e., a file reference containing a relative path to a directory below that of the referencing .emd or .ems file is permitted).

*Example:*

| file\_type file\_reference circuit\_name(.subckt name)

File\_IBIS-ISS net.iss netlist\_typ

File\_TS rules:

Either File\_TS or File\_IBIS-ISS is required for a [EMD Model]/[End EMD Model] group.File\_TS is followed by one unquoted string argument, which is the file\_reference for a Touchstone file. The Touchstone file under file\_reference shall be located in the same directory as the referencing .emd file or .ems file or in a specified directory under the referencing file as determined by the directory path (i.e., a file reference containing a relative path to a directory below that of the referencing .emd or .ems file is permitted).

*Example:*

| file\_type file\_reference

File\_TS typ.s8p

Unused\_port\_termination rules:

The Unused\_port\_termination subparameter is required under this condition:

File\_TS is used and the number of terminal lines (described below) is less than N+1 (where N is the number of ports in the Touchstone file)

Unused\_port\_termination is illegal under these conditions:

File\_IBIS-ISS is used

File\_TS is used, and the number of terminal lines is N+1

If required, only one Unused\_port\_termination subparameter may appear for a given [EMD Model] keyword.

The Unused\_port\_termination subparameter is followed by white space and one of these arguments:

Open

Reference

Resistance

“Open” declares that the unused ports remain unterminated (open-circuited).

“Reference” declares that the EDA tool terminates all unused ports with resistors whose resistance values are equal to the reference impedances provided in the Touchstone file for the respective unused ports, and all connected to the model’s reference terminal.

“Resistance” declares that the EDA tool terminates all unused ports with resistors, all having the same value, and all connected to the model’s reference terminal. The “Resistance” entry is followed by a third column entry with the (non-negative) numerical resistance value.

*Examples:*

Unused\_port\_termination Open

Unused\_port\_termination Reference

Unused\_port\_termination Resistance 43.5

Number\_of\_terminals rules:

The Number\_of\_terminals subparameter is required and defines the number of terminals associated with the EMD Model. The subparameter name shall be followed by a single integer argument on the same line. The argument shall be separated from the subparameter name by the “=” character. The subparameter name, “=” character, and argument may optionally be separated by whitespace.

Only one Number\_of\_terminals subparameter may appear for a given [EMD Model] keyword. The Number\_of\_terminals subparameter shall appear before any terminal lines and after all other subparameters for a given EMD Model.

For File\_IBIS-ISS, the Number\_of\_terminals value shall be equal to the number of subcircuit terminals for an IBIS-ISS subcircuit. Because an IBIS-ISS subcircuit requires at least one terminal the Number\_of\_terminals value shall be 1 or greater. The IBIS-ISS subcircuit terminals shall not contain an ideal reference node (SPICE node 0 or its synonyms).

For File\_TS, the Number\_of\_terminals value shall be a value equal to N+1 (where N is the number of ports in the Touchstone file). Because a Touchstone file requires at least one port, the Number\_of\_terminals value shall be 2 or greater.

*Example:*

Number\_of\_terminals = 3

Terminal line rules:

The terminal lines shall appear after the Number\_of\_terminals subparameter and before the [End EMD Model] keyword.

Terminal lines are of the following form, with each identifier separated by whitespace:

 <Terminal\_number> <Terminal\_type> <Terminal\_type\_qualifier> <Qualifier\_entry> [Aggressor\_Only]

Terminal\_number

The Terminal\_number is the identifier for a specific terminal. The value shall be 1 or greater and less than or equal to the Number\_of\_terminals. The same Terminal\_number shall not appear more than once for a given EMD Model.

For File\_IBIS-ISS, the Terminal\_number entry shall match the IBIS-ISS terminal (node) position. The Terminal\_number entries may be listed in any order as long as there are no duplicate entries. Each IBIS-ISS terminal shall have a terminal line entry.

For File\_TS, the Terminal\_number entry shall match the Touchstone file port number or reference terminal line, as shown below. The Terminal\_number entries may be listed in any order as long as there are no duplicate entries. The terminal line for Terminal\_number N+1 is required as a reference terminal for each port and shall be connected to a rail terminal or A\_gnd in the EMD Model. At least one other terminal line entry is required.

* Terminal\_number Port
* 1                     1
* 2                          2
* …
* N                        N
* N+1 Reference terminal for the Touchstone file

For Touchstone files, each unused port and its corresponding Terminal\_number shall be terminated in simulation with a resistor whose value corresponds to the Unused\_port\_termination subparameter entry. The resistor is connected to the model’s reference terminal.

Terminal\_type
The Terminal\_type is a string that identifies whether the terminal is a reference, supply or I/O terminal and whether the terminal is connected to an EMD pin or designator pin. Note that “I/O” in this context is a synonym for “signal”, as opposed to “supply” or “rail”; it is not intended to imply model type as used in the “Model\_type” subparameter.

Terminal\_type A\_gnd defines a connection to the simulator global reference node.  The A\_gnd node can be used at any interface.

Terminal\_type A\_gnd is not required under File\_TS or File\_IBIS-ISS.

If present under File\_TS, Terminal\_type A\_gnd may be used only once on the N+1th terminal line.

If present under File\_IBIS-ISS, Terminal\_type A\_gnd may be used any number of times on any of the terminal lines.

Furthermore, if the terminal is connected to a buffer supply rail, the Terminal\_type identifies to which specific buffer rail the terminal is connected. The Terminal\_type shall be one of the following:

* Pin\_I/O
* Pin\_Rail
* A\_gnd

Terminal\_type\_qualifier
Terminal\_type\_qualifier is a string that identifies the association between a terminal and a specific pin\_name, signal\_name or bus\_label in the [EMD Pin List], or specific pin\_name, signal\_name, or bus\_label in the [Designator Pin List].

Qualifier\_entry
The <Qualifier\_entry>, shown in angle brackets, is the name required for the following Terminal\_type\_qualifiers:

pin\_name <pin\_name\_entry>

signal\_name <signal\_name\_entry>

bus\_label <bus\_label\_entry>

Aggressor\_OnlyThe Aggressor\_Only entry is optional and is indicated by the string “Aggressor\_Only” without the quotation marks. Assigning Aggressor\_Only to a pin assigns the Aggressor\_Only properties to all pins of the same signal\_name listed in the [EMD Pin List] and [Designator Pin List] keywords.

Any \*\_I/O Terminal\_type without the Aggressor\_Only column may be considered an aggressor or a victim.

Multi-line EMD Models may describe only a subset of a coupled structure (e.g., a 64-line bus may be described by a four-line EMD Model). As a result, while the interconnects at the edges of the EMD Model may induce crosstalk onto other interconnects nearby, being on the edge of the EMD Model, they may not themselves experience the full crosstalk impact that the corresponding interconnect experiences in the real, full structure.

Crosstalk simulations use coupled interconnect models consisting of nets, or extended nets that may span packages, EMDs, boards, and connectors. If any terminal in any net or extended net in the coupled interconnect model is marked Aggressor\_Only, then the crosstalk contributions included in the simulation results reported for this net or extended net will be incomplete.

**13.4 TERMINAL\_TYPE ASSOCIATIONS FOR EMD AND DESIGNATOR PINS**

Terminal lines describe the IBIS-ISS terminal or Touchstone port to which each terminal of an EMD Model is connected. The arrangement of the terminal line entries (columns) is described below.

* The first column, Terminal\_number, contains an integer between 1 and the Number\_of\_terminals that describes the ordinal (positional) number of the IBIS-ISS node in the EMD Model subcircuit or Touchstone file port. The second column is Terminal\_type, the third column is Terminal\_type\_qualifier, the fourth column is Qualifier\_entry, and there is an optional fifth column “Aggressor\_Only”.
* The second column, Terminal\_type is:
	+ For I/O connections
		- Terminal\_type must be Pin\_I/O
		- Terminal\_type\_qualifier shall be pin\_name
			* EMD Pins shall be a pin\_name in the [EMD Pin List] list
			* Designator Pins shall be in the form from the [Designator Pin List]:
				+ <designator>.< pin\_name>
	+ For rail connections
		- Terminal\_type shall be Pin\_Rail
		- Terminal\_type\_qualifier shall be one of the following:
			* pin\_name
				+ Qualifier\_entry shall be a rail pin\_name in the [EMD Pin List] or [Designator Pin List] and with signal\_type POWER or GND
			* signal\_name
				+ Qualifier\_entry shall be a rail signal\_name in the [EMD Pin List] or of the form <designator\_name>.<signal\_name> entry from the [Designator Pin List]
				+ For [Designator Pin List] entries, the signal\_name values can be assigned so that they can be connected with the same signal\_name entries on the [EMD Pin List]. The signal\_name entries do not have to match those referenced under the [Component] or [Begin EMD] keywords.
				+ \*.<signal\_name> shall represent all of the [Designator Pin List] <signal\_name> entries at all [Designator Pin List] interfaces shorted together.
			* bus\_label
				+ Qualifier\_entry shall be a rail bus\_label in the [EMD Pin List] or [Designator Pin List]
				+ The bus\_label entry can be assigned to both the [EMD Pin List] and [Designator Pin List] entries to support a subset of connections that might be connected with a common signal\_name. For example, left-side routing and right-side routing might be isolated from each other.
				+ \*.<bus\_label> shall represent all of the [Designator Pin List] <bus\_label> entries at all [Designator Pin List] interfaces shorted together.
		- At any interface
			* Terminal\_type A\_gnd is available at any interface and without any Terminal\_type qualifier

Table 41 summarizes the rules described above and applies to terminals associated with the [EMD Pin List] keyword and with the [Designator Pin List] keyword.

Table 41 – Allowed Terminal\_type Associations1

| **Terminal\_type** | **Terminal\_type\_qualifier** | **Aggressor\_Only** |
| --- | --- | --- |
| **pin\_name** | **signal\_name** | **bus\_label** |
| Pin\_I/O | X |  |  | A |
| Pin\_Rail | Y | Y | Y |  |
| Pin\_Rail |  | \*.Y2 | \*.Y2 |  |
| A\_gnd |  |  |  |  |

Notes:

1. In the table, “X” refers to I/O pin names. “Y” indicates POWER and GND terminals. The letter “A” designates "Aggressor\_Only".
2. “\*.Y” indicates that all of the “Y” named POWER and GND terminals on each of the [Designator Pin List] interfaces are shorted together

There are at least three kinds of connectivity that can relate signal\_names, bus\_labels and/or terminals. These are described below.

For Rail terminals:

On one interface, terminals with the same signal\_name may be reduced to a single terminal for modeling purposes with the syntax:

<terminal number> Pin\_rail signal\_name <entry> or

<terminal number> Pin\_rail signal\_name <designator.entry>

On one interface, terminals with the same bus\_label may be reduced to a single terminal for modeling purposes with the syntax:

<terminal number> Pin\_rail bus\_label <entry> or

<terminal number> Pin\_rail bus\_label <designator.entry>

Electrical connections could exist between individual pin\_names, but these rail pins are modeled as if they are connected by shorts and are merged into one terminal.

For designator interfaces only, involving rails:

For *all* designator interfaces, terminals with the same signal\_name may be reduced to a single terminal for modeling purposes with the syntax:

<terminal number> Pin\_rail signal\_name <\*.entry>

For *all* designator interfaces, terminals with the same bus\_label may be reduced to a single terminal for modeling purposes with the syntax:

<terminal number> Pin\_rail bus\_label <\*.entry>

This syntax excludes rail terminals at the [EMD Pin List] interface. There may exist electrical connections between all of the \*.<name> terminals. The connections are not necessarily physical shorts on any one interface or between any of the interfaces.

Multiple applications exist for EMD Models focused on rail terminals. For example, an EMD Model with only rail terminals and two interfaces (no I/O terminals) can be used for a PDN (note that a). Also, an EMD Model with only rail terminals (no I/O terminals) and only one interface is permitted for applications such as for modeling rail decoupling circuits.

For I/O terminals:

Terminals at the same interface or at any designator interface that have the same signal\_name are considered “connected” in the same electrical net (named by the signal\_name entry).  The terminals need to be documented in the [EMD Model] keyword and their electrical connections are described by IBIS-ISS or Touchstone data.  Connections between these terminals are usually NOT shorts. The common signal\_name provides for a way to document net name connection between different components or modules at terminals that may have different pin\_names.  For example:

1 Pin\_I/O  pin\_name  A1     | signal\_name is DQ0

2 Pin\_I/O  pin\_name  U1.25  | signal\_name is DQ0

3 Pin\_I/O  pin\_name  U2.32  | signal\_name is DQ0

4 Pin\_I/O  pin\_name  U3.32  | signal\_name is DQ0

The common signal\_name in the [EMD Pin List] and/or [Designator Pin List] indicates that the four terminals are in the same net. Their electrical “connections” are described by the electrical content in the IBIS-ISS or Touchstone file data connected to terminals 1, 2, 3, and 4.

For I/O terminals with extended nets:

Tbetween nets of different names across an IBIS series component

**13.5 RDIMM EXAMPLE ILLUSTRATING SYNTAX AND NET OPTIONS**

**13.5.1 RDIMM Figures for Examples in 13.5.2 thru 13.5.4**

Figure X shows a DDR4 Registered DIMM containing DRAM components labeled by designators U1, U2, U4, U5 (front side) and U7-U11 (back side, not seen) and a Register component labeled by designator U3.

Also shown is pre-register net A07 connecting from an EMD pin to a designator pin of designator U3 and post-register net BA07 connecting from a designator pin of designator U3 to designator pins of designators U4, U5, U7, and U8 as well as termination resistor RN13 connecting to the VTT rail.



Figure X

Figure Y (Example 1), a zoomed in area of Figure X, shows an example of an extended net. The extended net A07 can be modeled in two ways:

1. One EMD Model defining only terminals for EMD pin 211 and designator pin U3.W1. The EMD Model contains the complete signal path of net A07, the series resistor R123, and net A07r (referenced in the A07.iss file with the subcircuit named “A07\_1”, as shown in Example 1).
2. One EMD Model or multiple EMD Models contained with an EMD Set that include terminals for EMD pin 211 and designator pin U3.W1 and two terminals for the pins of the series resistor. The resistor would be assigned a designator (R123) referencing an IBIS component (see Examples 2, 3). The connection between net A07 and net A07r through R123 might be determined automatically in some EDA tools or entered manually. Alternatively, net A07 and net A07r can be treated as two independent nets.



Figure Y

Figure Z (Examples 2, 3), a zoomed in area of Figure X, shows an example of an internal net. The post-register net BA07 connects from the register’s designator pin U3.B11 to the DDR4 DRAMs’ designator pins U4.M8, U5.M8, U7.M8, and U8.M8 as well as to one designator pin of the termination resistor RN13. RN13 terminates the signal to the VTT rail.



Figure Z

**13.5.2 Example 1 (R123 and RN13 Embedded in A07\_1 and BA07\_1)**

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| EMD Syntax Example 1 (Net A07 with Embedded Resistors)

| Using DDR4 RDIMM Example

[Begin EMD] DDR4\_RDIMM\_1

[Number of EMD Pins] 4

[EMD Pin List] signal\_name signal\_type bus\_label

203 VSS GND

211    A07

212   VDD         POWER VDD1

223 VTT POWER

[End EMD Pin List]

[EMD Parts]

DDR4\_Reg\_253b register.ibs DDR4\_Register

DDR4\_x8\_78b dram.ibs DDR4\_8Gb\_x8

[End EMD Parts]

[EMD Designator List]

U3 DDR4\_Reg\_253b

U4 DDR4\_x8\_78b

U5 DDR4\_x8\_78b

U7 DDR4\_x8\_78b

U8 DDR4\_x8\_78b

[End EMD Designator List]

[Designator Pin List] signal\_name signal\_type bus\_label

U3.B9 VDD POWER VDD1

U3.B11 BA07

U3.B12 VSS GND

U3.V3 VDD POWER VDD1

U3.W1 A07

U3.W3 VSS GND

|

U4.K9 VSS GND

U4.M8 BA07

U4.N9 VDD POWER VDD1

|

U5.K9 VSS GND

U5.M8 BA07

U5.N9 VDD POWER VDD1

|

U7.K9 VSS GND

U7.M8 BA07

U7.N9 VDD POWER VDD1

|

U8.K9 VSS GND

U8.M8 BA07

U8.N9 VDD POWER VDD1

[End Designator Pin List]

[Voltage List]

VDD 1.200 1.140 1.260

VSS 0.000 0.000 0.000

VTT 0.600 0.570 0.630

[End Voltage List]

[EMD Group] Addr\_07\_Group\_1

Addr\_07\_1 NA

[End EMD Group]

[End EMD]

[EMD Set] Addr\_07\_1

[EMD Model] A07\_1

File\_IBIS-ISS A07.iss A07\_1

Number\_of\_terminals = 6

1 Pin\_I/O pin\_name 211

2 Pin\_I/O pin\_name U3.W1 | Connection from 211 to U3.W1 includes

 | Series Resistor modeled in A07.iss A07\_1

3 Pin\_Rail bus\_label VDD1

4 Pin\_Rail signal\_name VSS

5 Pin\_Rail bus\_label U3.VDD1

6 Pin\_Rail bus\_label U3.VSS

[End EMD Model]

[EMD Model] BA07\_1

File\_IBIS-ISS A07.iss BA07\_1

Number\_of\_terminals = 19

1 Pin\_I/O pin\_name U3.B11

2 Pin\_Rail bus\_label U3.VDD1

3 Pin\_Rail signal\_name U3.VSS

4 Pin\_I/O pin\_name U4.M8

5 Pin\_Rail bus\_label U4.VDD1

6 Pin\_Rail signal\_name U4.VSS

7 Pin\_I/O pin\_name U5.M8

8 Pin\_Rail bus\_label U5.VDD1

9 Pin\_Rail signal\_name U5.VSS

10 Pin\_I/O pin\_name U7.M8

11 Pin\_Rail bus\_label U7.VDD1

12 Pin\_Rail signal\_name U7.VSS

13 Pin\_I/O pin\_name U8.M8 | Termination Resistor to VTT

 | included in A07.iss BA07\_1

14 Pin\_Rail bus\_label U8.VDD1

15 Pin\_Rail signal\_name U8.VSS

17 Pin\_Rail bus\_label VDD1

18 Pin\_Rail signal\_name VTT

19 Pin\_Rail signal\_name VSS

[End EMD Model]

[End EMD Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**13.5.3 Example 2 (R123 and RN13 modeled as separate IBIS components in A07\_2, BA07\_2)**

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| EMD Syntax Example 2 (External Resistors)

| Using DDR4 RDIMM Example

[Begin EMD] DDR4\_RDIMM\_2

[Number of EMD Pins] 4

[EMD Pin List] signal\_name signal\_type bus\_label

203 VSS GND

211    A07         |Net A07 Connection

212   VDD         POWER VDD1

223 VTT POWER

[End EMD Pin List]

[EMD Parts]

DDR4\_Reg\_253b register.ibs DDR4\_Register

DDR4\_x8\_78b dram.ibs DDR4\_8Gb\_x8

510-500874 resistors.ibs RES\_22ohms

510-501618 resistors.ibs RPACK4\_33ohms

[End EMD Parts]

[EMD Designator List]

U3 DDR4\_Reg\_253b

U4 DDR4\_x8\_78b

U5 DDR4\_x8\_78b

U7 DDR4\_x8\_78b

U8 DDR4\_x8\_78b

R123 510-500874

RN13 510-501618

[End EMD Designator List]

[Designator Pin List] signal\_name signal\_type bus\_label

U3.B9 VDD POWER VDD1

U3.B11 BA07

U3.B12 VSS GND

U3.V3 VDD POWER VDD1

U3.W1 A07r | Net A07r Terminal

U3.W3 VSS GND

|

U4.K9 VSS GND

U4.M8 BA07

U4.N9 VDD POWER VDD1

|

U5.K9 VSS GND

U5.M8 BA07

U5.N9 VDD POWER VDD1

|

U7.K9 VSS GND

U7.M8 BA07

U7.N9 VDD POWER VDD1

|

U8.K9 VSS GND

U8.M8 BA07

U8.N9 VDD POWER VDD1

|

R123.1 A07 | Net A07 Terminal

R123.2 A07r | Net A07r Terminal

RN13.2 VTT POWER

RN13.7 BA07

[End Designator Pin List]

[Voltage List]

VDD 1.200 1.140 1.260

VSS 0.000 0.000 0.000

VTT 0.600 0.570 0.630

[End Voltage List]

[EMD Group] Addr\_07\_Group\_2

Addr\_07\_2 NA

[End EMD Group]

[End EMD]

[EMD Set] Addr\_07\_2

[EMD Model] A07\_2

File\_IBIS-ISS A07.iss A07\_2

Number\_of\_terminals = 8

1 Pin\_I/O pin\_name 211 | Net A07 Terminal and Connection

2 Pin\_I/O pin\_name R123.1 | Net A07 Terminal and Connection

3 Pin\_I/O pin\_name R123.2 | Net A07r Terminal and Connection

4 Pin\_I/O pin\_name U3.W1 | Net A07r Terminal and Connection

5 Pin\_Rail bus\_label VDD1

6 Pin\_Rail signal\_name VSS

7 Pin\_Rail bus\_label U3.VDD1

8 Pin\_Rail signal\_name U3.VSS

[End EMD Model]

[EMD Model] BA07\_2

File\_IBIS-ISS A07.iss BA07\_2

Number\_of\_terminals = 19

1 Pin\_I/O pin\_name U3.B11

2 Pin\_Rail bus\_label U3.VDD1

3 Pin\_Rail signal\_name U3.VSS

4 Pin\_I/O pin\_name U4.M8

5 Pin\_Rail bus\_label U4.VDD1

6 Pin\_Rail signal\_name U4.VSS

7 Pin\_I/O pin\_name U5.M8

8 Pin\_Rail bus\_label U5.VDD1

9 Pin\_Rail signal\_name U5.VSS

10 Pin\_I/O pin\_name U7.M8

11 Pin\_Rail bus\_label U7.VDD1

12 Pin\_Rail signal\_name U7.VSS

13 Pin\_I/O pin\_name U8.M8

14 Pin\_Rail bus\_label U8.VDD1

15 Pin\_Rail signal\_name U8.VSS

16 Pin\_I/O pin\_name RN13.7

17 Pin\_Rail bus\_label VDD1

18 Pin\_Rail signal\_name RN13.VTT

19 Pin\_Rail signal\_name VSS

[End EMD Model]

[End EMD Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**13.5.4 Example 3 (R123 IBIS Model Terminals split into two [EMD Model]s, POWER Rails in a Separate [EMD Model]**

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| EMD Syntax Example 3 (External Resistors, Separate A07, A07R, and POWER

| Models)

| Using DDR4 RDIMM Example

|

[Begin EMD] DDR4\_RDIMM\_3

[Number of EMD Pins] 4

[EMD Pin List] signal\_name signal\_type bus\_label

203 VSS GND

211    A07

212   VDD         POWER VDD1

223 VTT POWER

[End EMD Pin List]

[EMD Parts]

DDR4\_Reg\_253b register.ibs DDR4\_Register

DDR4\_x8\_78b dram.ibs DDR4\_8Gb\_x8

510-500874 resistors.ibs RES\_22ohms

510-501618 resistors.ibs RPACK4\_33ohms

[End EMD Parts]

[EMD Designator List]

U3 DDR4\_Reg\_253b

U4 DDR4\_x8\_78b

U5 DDR4\_x8\_78b

U7 DDR4\_x8\_78b

U8 DDR4\_x8\_78b

R123 510-500874

RN13 510-501618

[End EMD Designator List]

[Designator Pin List] signal\_name signal\_type bus\_label

U3.B9 VDD POWER VDD1

U3.B11 BA07

U3.B12 VSS GND

U3.V3 VDD POWER VDD1

U3.W1 A07r | Net A07r Terminal

U3.W3 VSS GND

U4.K9 VSS GND

U4.M8 BA07

U4.N9 VDD POWER VDD1

U5.K9 VSS GND

U5.M8 BA07

U5.N9 VDD POWER VDD1

U7.K9 VSS GND

U7.M8 BA07

U7.N9 VDD POWER VDD1

U8.K9 VSS GND

U8.M8 BA07

U8.N9 VDD POWER VDD1

R123.1 A07 | Net A07 Terminal

R123.2 A07r | Net A07r Terminal

RN13.2 VTT POWER

RN13.7 BA07

[End Designator Pin List]

[Voltage List]

VDD 1.200 1.140 1.260

VSS 0.000 0.000 0.000

VTT 0.600 0.570 0.630

[End Voltage List]

[EMD Group] Addr\_07\_Group\_3

Addr\_07\_3 NA

RIGHT\_SIDE\_POWER NA

[End EMD Group]

[End EMD]

[EMD Set] Addr\_07\_3

[EMD Model] A07\_3

File\_IBIS-ISS A07.iss A07\_3

Number\_of\_terminals = 3

1 Pin\_I/O pin\_name 211

2 Pin\_I/O pin\_name R123.1 | Net A07 Terminals and Connection

 | Series Resistor is in two [EMD Model]s

3 Pin\_Rail signal\_name VSS

[End EMD Model]

|

[EMD Model] A07R\_3

File\_IBIS-ISS A07.iss A07R\_3

Number\_of\_terminals = 3

1 Pin\_I/O pin\_name R123.2 | Net A07r Terminal and Connection

2 Pin\_I/O pin\_name U3.W1 | Net A07r Terminal and Connection

3 Pin\_Rail signal\_name VSS

[End EMD Model]

|

[EMD Model] BA07\_3

File\_IBIS-ISS A07.iss BA07\_3

Number\_of\_terminals = 13

1 Pin\_I/O pin\_name U3.B11

2 Pin\_Rail signal\_name U3.VSS

3 Pin\_I/O pin\_name U4.M8

4 Pin\_Rail signal\_name U4.VSS

5 Pin\_I/O pin\_name U5.M8

6 Pin\_Rail signal\_name U5.VSS

7 Pin\_I/O pin\_name U7.M8

8 Pin\_Rail signal\_name U7.VSS

9 Pin\_I/O pin\_name U8.M8

10 Pin\_Rail signal\_name U8.VSS

11 Pin\_I/O pin\_name RN13.7

12 Pin\_Rail signal\_name RN13.VTT

13 Pin\_Rail signal\_name VSS

[End EMD Model]

[End EMD Set]

[EMD Set] RIGHT\_SIDE\_POWER

[EMD Model] RIGHT\_SIDE\_VDD1\_VTT\_VSS

File\_IBIS-ISS rdimm\_power.iss RIGHT\_SIDE\_VDD1\_VTT\_VSS

Number\_of\_terminals = 14

1 Pin\_Rail bus\_label VDD1

2 Pin\_Rail signal\_name VSS

3 Pin\_Rail signal\_name VTT

4 Pin\_Rail bus\_label U3.VDD1

5 Pin\_Rail signal\_name U3.VSS

6 Pin\_Rail bus\_label U4.VDD1

7 Pin\_Rail signal\_name U4.VSS

8 Pin\_Rail bus\_label U5.VDD1

9 Pin\_Rail signal\_name U5.VSS

10 Pin\_Rail bus\_label U7.VDD1

11 Pin\_Rail signal\_name U7.VSS

12 Pin\_Rail bus\_label U8.VDD1

13 Pin\_Rail signal\_name U8.VSS

14 Pin\_Rail signal\_name RN13.VTT

[End EMD Model]

[End EMD Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**13.6 CONNECTION RULES FOR EMD GROUP, EMD SET, AND EMD MODEL**

At the [EMD Group] level, the connections between the referenced [EMD Set]s (and their encapsulated [EMD Model]s are determined by the following rules:

1. I/O pins (Pin\_I/O terminals by pin\_name entries)
	1. Without Aggressor\_Only:
		1. I/O terminals may exist with or without rail terminals
		2. Within each [EMD Model], pin\_name entries (as listed in the [EMD Pin List] keyword) shall be distinct for I/O pins
		3. Within each [EMD Model], <designator>.<pin\_name> entries (as listed in the [Designator Pin List] keyword) shall be distinct for I/O pins
		4. At any one interface and for all [EMD Model]s referenced by all [EMD Set]s under an [EMD Group], no duplicate pin\_name entries are permitted for I/O pins
		5. Electrical connections between I/O pins are based on the content of the referenced electrical models (\*.iss or Touchstone files)
		6. Net connections are indicated by identical signal\_name entries available from the [EMD Pin List] and/or [Designator Pin List] entries. For example, Pin\_I/O pin\_name 211 and Pin\_I/O pin\_name U3.W1 are considered connected through the IBIS-ISS subcircuit because they both share the same signal\_name, A07 in Example X (Example 1)
		7. The logical and electrical connections can span several interfaces. In Example X, Pin\_I/O pin\_name U3.W1, Pin\_I/O pin\_name U4.W1, etc. share the same signal\_name BA07 and are therefore in the same net
	2. With Aggressor\_Only:
		1. I/O terminals may exist with or without rail terminals
		2. To permit selection of nets within an [EMD Group], identical pin\_name entries are permitted in different [EMD Model] keywords if there is no overlap of pin\_name entries at the same interface without Aggressor\_Only. For example, “Pin\_I/O pin\_name 211” and “Pin\_I/O pin\_name 211 Aggressor\_Only” can exist under different [EMD Model] keywords but will not be used together in simulation
		3. The complete I/O net for a given signal\_name entry is deemed Aggressor\_Only if one or more of the pin\_names in the net has an Aggressor\_Only column entry
		4. At least one net shall exist without Aggressor\_Only
2. Rail (Pin\_Rail terminals) connections by pin\_name, signal\_name, bus\_label
	1. Within an [EMD Group] and for all referenced [EMD Set] keywords and their encapsulated [EMD Model] keywords, identically-named rail terminals shall be considered connected based on these rules:
		1. Rail terminals may exist with or without I/O terminals
		2. At an EMD Pin List interface, identical Pin\_Rail pin\_name, bus\_label or signal\_name entries in different [EMD Model]s shall be considered shorted
		3. At a Designator Pin List interface, identical Pin\_Rail pin\_name, bus\_label, or signal\_name entries in different [EMD Model]s shall be considered shorted
		4. For each [EMD Model] and at any one interface, there shall not be any overlap of Pin\_Rail pin\_name, bus\_label and signal\_name entries:
			1. A pin\_name entry shall not overlap with a bus\_label entry
			2. A pin\_name entry shall not overlap with a signal\_name entry
			3. A bus\_label entry shall not overlap with a signal\_name entry
		5. For all [EMD Model]s and at any one interface, where Pin\_Rail pin\_name, bus\_label and/or signal\_name entries in different [EMD Model]s overlap:
			1. A pin\_name entry shall be shorted with a corresponding bus\_label entry
			2. A pin\_name entry shall be shorted with a corresponding signal\_name entry
			3. A bus\_label entry shall be shorted with a corresponding signal\_name entry
	2. Within an [EMD Group] and for all referenced [EMD Set] keywords and their encapsulated [EMD Model] keywords, Pin\_Rail terminals are considered merged into a single terminal across designator interfaces (not the EMD interface) based on these rules:
		1. Pin\_Rail signal\_name \*.<signal\_name> shorts all connections with signal\_name <signal\_name> for all designator interfaces (not the EMD interface)
		2. Pin\_Rail bus\_label \*.<bus\_label> shorts all connections with bus\_label <bus\_label> for all designator interfaces (not the EMD interface)
		3. No corresponding rule for pin\_name entries exists since connected rail pin\_names can differ at different interfaces
	3. Simulator Global Reference:
		1. Terminal\_type A\_gnd can be used for a simulator global reference in any EMD Model
		2. All simulator global references are shorted

**13.7 ADDITIONAL EMD MODEL EXAMPLES**

*Examples:*

The example below for a simplified DIMM includes pins at the EMD interface and at the designator interfaces of two memory components. Three EMD Groups provide EMD Model options including one option with no crosstalk and two options with crosstalk included. The EMD Groups with crosstalk included show use of IBIS-ISS or Touchstone files, and the rail connections are modeled in separate EMD Sets that are included in each EMD Group. The rail terminals are connected by either bus\_label or signal\_name. Bus\_labels are used to split the VDD rail into VDD1 and VDD2 buses. While only one VSS rail is shown, separate VSS rails could exist (for example, VSS1 and VSS2) and would be included by using bus\_label syntax.

[Begin EMD] DIMM

[Number of EMD Pins] 9

[EMD Pin List] signal\_name signal\_type bus\_label

A1 DQ0

A2 DQ1

A3 DQ2

A4 DQ3

P1 VDD POWER VDD1

P2 VDD POWER VDD2

G1 VSS GND

[End EMD Pin List]

[EMD Parts]

ACME\_MEM mem.ibs MEMx4

[End EMD Parts]

[EMD Designator List]

U1 ACME\_MEM

U2 ACME\_MEM

[End EMD Designator List]

[Designator Pin List] signal\_name signal\_type bus\_label

U1.1 VDD POWER VDD1

U1.2 VDD POWER VDD2

U1.3 VSS GND

U1.4 VSS GND

U1.5 DQ0

U1.6 DQ1

U1.7 DQ2

U1.8 DQ3

|

U2.1 VDD POWER VDD1

U2.2 VDD POWER VDD2

U2.3 VSS GND

U2.4 VSS GND

U2.5 DQ0

U2.6 DQ1

U2.7 DQ2

U2.8 DQ3

[End Designator Pin List]

| EMD Group has no crosstalk modeled and includes the

| rails in the same IBIS-ISS subcircuit

[EMD Group] All\_DQs\_No\_Coupling\_Rails

All\_DQs\_Uncoupled NA

[End EMD Group]

| EMD Group models crosstalk with IBIS-ISS subcircuits

[EMD Group] All\_DQs\_Aggressor\_Options\_ISS

All\_DQs\_Crosstalk\_ISS NA

Rails\_ISS NA

[End EMD Group]

| EMD Group models crosstalk with Touchstone files

[EMD Group] All\_DQs\_Aggressor\_Options\_TS

All\_DQs\_Crosstalk\_TS NA

Rails\_TS NA

[End EMD Group]

[End EMD] | End of [Begin EMD]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* EMD Sets \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

[EMD Set] All\_DQs\_Uncoupled

[EMD Model] DQ0\_3

File\_IBIS-ISS DQ.iss DQ

Number\_of\_terminals = 20

1 Pin\_I/O pin\_name A1 | DQ0

2 Pin\_I/O pin\_name A2 | DQ1

3 Pin\_I/O pin\_name A3 | DQ2

4 Pin\_I/O pin\_name A4 | DQ3

5 Pin\_Rail signal\_name VDD | EMD Pins P1 and P2

6 Pin\_Rail signal\_name VSS | EMD Pin G1

|

7 Pin\_I/O pin\_name U1.5 | DQ0

8 Pin\_I/O pin\_name U1.6 | DQ1

9 Pin\_I/O pin\_name U1.7 | DQ2

10 Pin\_I/O pin\_name U1.8 | DQ3

11 Pin\_Rail bus\_label U1.VDD1 | U1 Pin 1

12 Pin\_Rail bus\_label U1.VDD2 | U1 Pin 2

13 Pin\_Rail signal\_name U1.VSS | U1 Pins 3 and 4

|

14 Pin\_I/O pin\_name U2.5 | DQ0

15 Pin\_I/O pin\_name U2.6 | DQ1

16 Pin\_I/O pin\_name U2.7 | DQ2

17 Pin\_I/O pin\_name U2.8 | DQ3

18 Pin\_Rail bus\_label U2.VDD1 | U2 Pin 1

19 Pin\_Rail bus\_label U2.VDD2 | U2 Pin 2

20 Pin\_Rail signal\_name U2.VSS | U2 Pins 3 and 4

[End EMD Model]

[End EMD Set]

[EMD Set] All\_DQs\_Crosstalk\_ISS

| EMD Model includes all crosstalk contributions for DQ1.

| Crosstalk contributions are incomplete for other nets

| marked as Aggressor\_Only.

[EMD Model] DQ1\_Victim

File\_IBIS-ISS DQ.iss DQ1\_Victim

Number\_of\_terminals = 15

1 Pin\_I/O pin\_name A1 Aggressor\_Only | DQ0

2 Pin\_I/O pin\_name A2 | DQ1

3 Pin\_I/O pin\_name A3 Aggressor\_Only | DQ2

4 Pin\_I/O pin\_name A4 Aggressor\_Only | DQ3

5 Pin\_Rail signal\_name VSS

|

6 Pin\_I/O pin\_name U1.5 | DQ0

7 Pin\_I/O pin\_name U1.6 | DQ1

8 Pin\_I/O pin\_name U1.7 | DQ2

9 Pin\_I/O pin\_name U1.8 | DQ3

10 Pin\_Rail signal\_name U1.VSS | U1 Pins 3 and 4

|

11 Pin\_I/O pin\_name U2.5 | DQ0

12 Pin\_I/O pin\_name U2.6 | DQ1

13 Pin\_I/O pin\_name U2.7 | DQ2

14 Pin\_I/O pin\_name U2.8 | DQ3

15 Pin\_Rail signal\_name U2.VSS | U2 Pins 3 and 4

[End EMD Model]

| EMD Model includes all crosstalk contributions for DQ2.

| Crosstalk contributions are incomplete for other nets

| marked as Aggressor\_Only.

[EMD Model] DQ2\_Victim

File\_IBIS-ISS DQ.iss DQ2\_Victim

Number\_of\_terminals = 15

1 Pin\_I/O pin\_name A1 Aggressor\_Only | DQ0

2 Pin\_I/O pin\_name A2 Aggressor\_Only | DQ1

3 Pin\_I/O pin\_name A3 | DQ2

4 Pin\_I/O pin\_name A4 Aggressor\_Only | DQ3

5 Pin\_Rail signal\_name VSS

|

6 Pin\_I/O pin\_name U1.5 | DQ0

7 Pin\_I/O pin\_name U1.6 | DQ1

8 Pin\_I/O pin\_name U1.7 | DQ2

9 Pin\_I/O pin\_name U1.8 | DQ3

10 Pin\_Rail signal\_name U1.VSS | U1 Pins 3 and 4

|

11 Pin\_I/O pin\_name U2.5 | DQ0

12 Pin\_I/O pin\_name U2.6 | DQ1

13 Pin\_I/O pin\_name U2.7 | DQ2

14 Pin\_I/O pin\_name U2.8 | DQ3

15 Pin\_Rail signal\_name U2.VSS | U2 Pins 3 and 4

[End EMD Model]

[End EMD Set]

[EMD Set] Rails\_ISS

[EMD Model] Power\_Rails

File\_IBIS-ISS Power\_Rails.iss Rails

Number\_of\_terminals = 8

1 Pin\_Rail signal\_name VDD | EMD Pins P1 and P2

2 Pin\_Rail signal\_name VSS | EMD Pin G1

|

3 Pin\_Rail bus\_label U1.VDD1 | U1 Pin 1

4 Pin\_Rail bus\_label U1.VDD2 | U1 Pin 2

5 Pin\_Rail signal\_name U1.VSS | U1 Pins 3 and 4

|

6 Pin\_Rail bus\_label U2.VDD1 | U2 Pin 1

7 Pin\_Rail bus\_label U2.VDD2 | U2 Pin 2

8 Pin\_Rail signal\_name U2.VSS | U2 Pins 3 and 4

[End EMD Model]

[End EMD Set]

[EMD Set] All\_DQs\_Crosstalk\_TS

| EMD Model includes all crosstalk contributions for DQ1.

| Crosstalk contributions are incomplete for other nets

| marked as Aggressor\_Only.

[EMD Model] DQ1\_Victim

File\_TS DQ1\_Victim.ts

Unused\_port\_termination Reference

Number\_of\_terminals = 25

1 Pin\_I/O pin\_name A1 Aggressor\_Only | DQ0

3 Pin\_I/O pin\_name A2 | DQ1

5 Pin\_I/O pin\_name A3 Aggressor\_Only | DQ2

7 Pin\_I/O pin\_name A4 Aggressor\_Only | DQ3

|

9 Pin\_I/O pin\_name U1.5 | DQ0

11 Pin\_I/O pin\_name U1.6 | DQ1

13 Pin\_I/O pin\_name U1.7 | DQ2

15 Pin\_I/O pin\_name U1.8 | DQ3

|

17 Pin\_I/O pin\_name U2.5 | DQ0

19 Pin\_I/O pin\_name U2.6 | DQ1

21 Pin\_I/O pin\_name U2.7 | DQ2

23 Pin\_I/O pin\_name U2.8 | DQ3

|

25 A\_gnd | Reference for all ports

[End EMD Model]

| EMD Model includes all crosstalk contributions for DQ2.

| Crosstalk contributions are incomplete for other nets

| marked as Aggressor\_Only.

[EMD Model] DQ2\_Victim

File\_TS DQ2\_Victim.ts

Unused\_port\_termination Reference

Number\_of\_terminals = 25

1 Pin\_I/O pin\_name A1 Aggressor\_Only | DQ0

3 Pin\_I/O pin\_name A2 Aggressor\_Only | DQ1

5 Pin\_I/O pin\_name A3 | DQ2

7 Pin\_I/O pin\_name A4 Aggressor\_Only | DQ3

|

9 Pin\_I/O pin\_name U1.5 | DQ0

11 Pin\_I/O pin\_name U1.6 | DQ1

13 Pin\_I/O pin\_name U1.7 | DQ2

15 Pin\_I/O pin\_name U1.8 | DQ3

|

17 Pin\_I/O pin\_name U2.5 | DQ0

19 Pin\_I/O pin\_name U2.6 | DQ1

21 Pin\_I/O pin\_name U2.7 | DQ2

23 Pin\_I/O pin\_name U2.8 | DQ3

|

25 A\_gnd | Reference for all ports

[End EMD Model]

[End EMD Set]

[EMD Set] Rails\_TS

[EMD Model] Power\_Rails

File\_TS Power\_Rails\_TS.s8p

Number\_of\_terminals = 9

1 Pin\_Rail signal\_name VDD | EMD Pins P1 and P2

2 Pin\_Rail signal\_name VSS | EMD Pin G1

|

3 Pin\_Rail bus\_label U1.VDD1 | U1 Pin 1

4 Pin\_Rail bus\_label U1.VDD2 | U1 Pin 2

5 Pin\_Rail signal\_name U1.VSS | U1 Pins 3 and 4

|

6 Pin\_Rail bus\_label U2.VDD1 | U2 Pin 1

7 Pin\_Rail bus\_label U2.VDD2 | U2 Pin 2

8 Pin\_Rail signal\_name U2.VSS | U2 Pins 3 and 4

|

9 A\_gnd | Reference for all ports

[End EMD Model]

[End EMD Set]

*Keyword:* [End EMD Model]

*Required:* Yes

*Description:* Marks the end of an EMD Model.

*Usage Rules:* This keyword must come at the end of each complete electrical EMD Model.

*Example:*

[End EMD Model]