Effective Signal Integrity Analysis using IBIS Models

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2000 High-Performance System Design Conference

Abstract

IBIS models are being widely used in various SI(Signal Integrity) analyses across the Industry. Cisco Systems, Inc uses IBIS models in both pre-layout and post-layout analysis of high-speed networking products.
This paper will go over the evolution of IBIS to its present form. It will highlight some of the common pitfalls made in IBIS model generation and provide detailed solutions to prevent them. Discussions on various shareware available for model validation will also be made.
The paper will also share a methodology used at Cisco Systems, Inc to verify IBIS models along with some tips on Library management and future IBIS directions.

Authors/Speakers

Syed B. Huq

Current Activities

Syed B. Huq is a Signal Integrity Engineer and Technical Leader working for Cisco System, Inc's ELB Signal Integrity/Packaging Design Technology Group. He is involved with SI analysis/simulations of ATM and Gigabit Ethernet products and various ASIC related Signal Integrity efforts. Syed Huq is leading the team involved with reviewing and verifying the IBIS models for Cisco's SI Library. In his current role Syed is also responsible for managing the transistor level HSPICE library.

Background

Syed received his BSEE from Southern Illinois University and has been working in the electronic industry for over 12 years in Test, Product, Applications, and Signal Integrity Engineering.
Syed was the former vice-chair of the ANSI/EIA-656 IBIS committee and is an active participant representing Cisco to the IBIS forum.
In his previous responsibility, Syed Huq was directly involved in implementing and executing the IBIS program for various product groups at National Semiconductor Corporation.

Slide1

Effective Signal Integrity Analysis using IBIS Models

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Slide2

Agenda

- What is IBIS
- The Golden Triangle
- History
- Parameters that are required and Why
- Problems & Solutions to common issues
- Model Validation
- Having a requirement specification
- IBIS Library
- Future directions of IBIS
- Conclusions

This presentation will cover some of the common pitfalls made in IBIS model generation and provide solutions to prevent them.
A step by step approach to model validation will be highlighted along with some tips on Library management and future IBIS directions.

Slide3

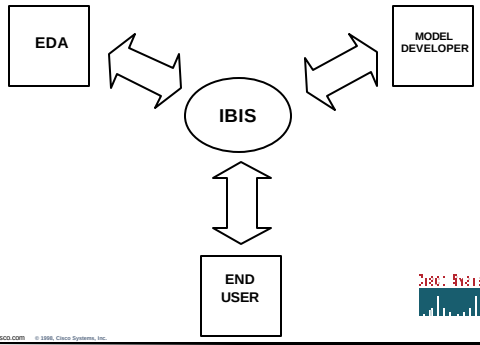
What is IBIS:

- **I/O Buffer Information Specification is a fast and accurate Behavioral method of modeling I/O buffers based on V/I curve data derived from measurements or full circuit simulation.**
- **Uses a standardized software parsable format to create the Behavioral Information needed to model Analog characteristics of IC's.**
- **Can be used by almost any Analog Simulators/EDA tools in the Industry.**

Majority of all IBIS models is generated through SPICE translation. At the same time, there are various models that are generated through actual measurements of Silicon. In addition, measurements are often used to refine/validate/improve existing models, previously generated from SPICE.
Regardless of source, the model must pass the Parser Test to make sure syntactically the model meets the IBIS specification.
Almost any Analog simulator or EDA tool vendor, SPICE based or non-SPICE based, supports the IBIS standard today. Some of these simulators use the model in its native format, while others translate the model into its proprietary modeling format.

Slide4

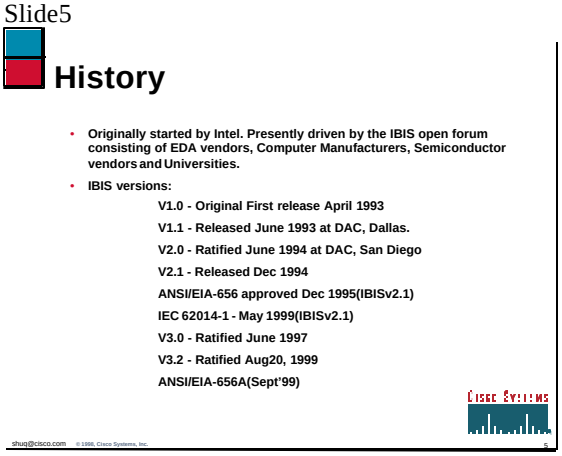
The Golden Triangle



IBIS as a specification is primarily interpreted by three major segments of the Industry. The IBIS spec needs to be understood by the EDA community who is supporting the tools, the Model developer who develops the models, and the user community who is the consumer of the models. The EDA Industry needs to support all

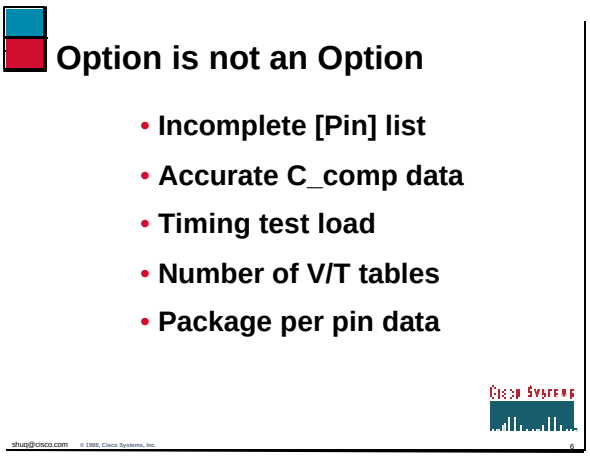
the features in the specification. Some simulators support portions of the specification, while others may support all.
The end users need to do specific types of simulation analysis that the tool may not support (or the model may not contain the data).
A model provider may leave out various 'optional' parameters and create a simplistic model not knowing how an end customer uses such a model.
These three-way synergy is critical in generating to supporting and simulating an IBIS model.
This article will to point out some very basic IBISv2.1 features that should be considered as 'must have'. A good SI simulation can only be performed if these blocks work together. **So join the IBIS forum and be an active participant. You can't beat the end result.**

Slide5



IBIS specifications are continually being refined by the committee. With the advances in technology, various characteristics of the I/O buffer behaviors are being added to the IBIS specification to handle them in system level Signal Integrity Analysis. It is always beneficial to know what each version of the specification has enhanced.
IBIS specifications technical discussions are held through monthly teleconferences. Summit meetings are also held a few times throughout the year. DesignCon(Jan-Feb), Design Automation and Test in Europe(DATE Mar), Design Automation Conference(DAC June), PCB Design East(Sept)are the most notable ones.
It is through these technical discussions that BIRDs(Buffer Issue Resolution Documents)are proposed, discussed and eventually voted for approval into the standard.

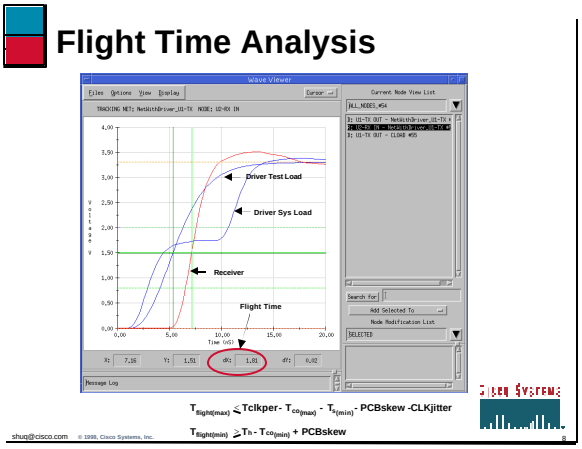
Slide6



IBIS today is at v3.2(1999). Most of the discussions here is for IBISv2.1 since the bulk of the models generated today are v2.1. In order to be backward compatible to the previous versions, new features are added as OPTIONAL parameters.
Model providers often misinterpret this as being 'NOT REQUIRED'. But the features were added in the first place because it's very much required!
This article will try to highlight the bare minimum for standard CMOS devices. Consult with your customers for other features that may be required.
IBIS has always been a component-centric model as opposed to structural(SPICE) models, which are more buffer-centric. At the same time, IBIS is mostly used on board level SI Analysis. The user translates the PCB database to generate transmission line models of the board traces. Then IBIS models are tied to the proper Drivers and Receivers on the board. The end user then can drive any pins of the device connected to whatever net on the board to run a simulation. This becomes a problem if the model has an incomplete set of pins.
I have come across many model where the same C_comp was used for all Typ, Min and Max or only the Typ value was provided. C_comp is a key parameter particularly for Receiver Inputs and should be characterized and provided in the model. C_comp defines the silicon die capacitance and does not account for package capacitance.

Slide7 [None]

Slide8



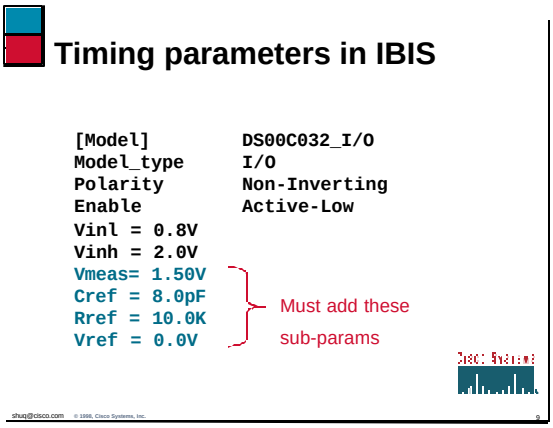
For Common CLK applications, Flight time analysis is a key factor of SI simulations. $T_{flight(max)}$ determines how far apart you can place two component without violating timing budget while $T_{flight(min)}$ determines how close to place the two components.

In order to do this, the simulator needs to know the manufacturers test load conditions under which T_{co}(Clk-to-out)is guaranteed. These test loads can be different from vendor to vendor. Once the test load is defined in the IBIS model, the simulator can derive the time it takes to reach the voltage measure point under the test load condition. The simulator then subtracts this test load delay from actual system load delay in order to report the correct flight time from the Driver to the Receiver.

For XTK(Viewlogic)users, this is called TIME_TO_VM. The time it takes to reach the voltage measure point. Without the test load, this TIME_TO_VM cannot be calculated by the simulator. TIME_TO_VM is automatically calculated when the IBIS model is translated to XTK(using ibis2xtk).

This timing analysis cannot be performed if the test load conditions are not provided in the IBIS model.

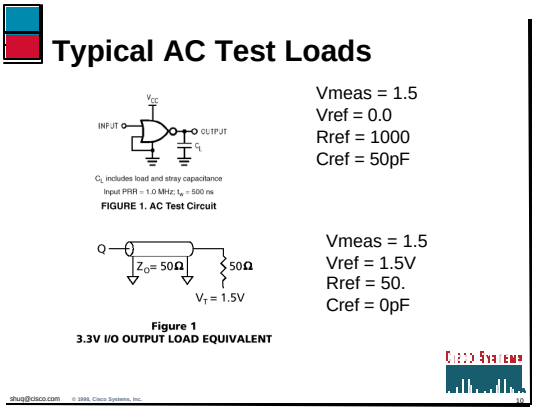
Slide9



The four parameters shown above are the timing test load and they should be added for the Output, 3-state, I/O models etc

Model providers do not need to run any simulations or analysis to obtain these timing test loads. Just pick them off the datasheet AC test load conditions.

Slide10



Two typical datasheet test loads are shown. The first figure shows a capacitive load to GND. This value of C_L was 50pF for a logic device. This load is represented by Cref. Since there is no Rref, it is assumed to be high-impedance.

The second figure illustrates a different test load for a Memory device and the IBIS test load description is shown on the right.

Vmeas = Output Voltage measure point. Typically Vdd/2

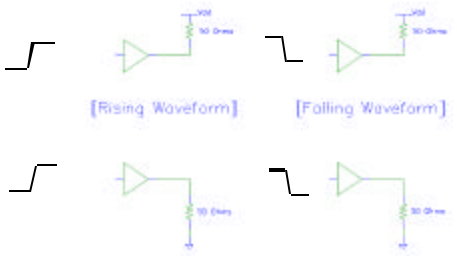
Vref = Test load pullup or pulldown reference voltage

Rref = Test load resistive value

Cref = Test load capacitive value

Slide11

Four V/T table



V/T table data contains the switching characteristics over time. The IBIS specification supports 100 waveform tables per model keyword. But, many times model developers look at the examples in an IBIS specification to understand the loading conditions they should apply. Since only two examples are shown, they end up providing exactly two V/T tables under the same loading conditions as the examples in the specification.

The ideal case is to provide 4 V/T tables: 2 for the Rising waveform and 2 for the Falling waveform. The combination of all these 4 V/T tables truly captures the turn-on and turn-off of the P-channel and N-channel transistors.

Slide12

V/T waveform Data

[Rising Waveform]
R_fixture = 50.000
V_fixture = 3.30
V_fixture_min = 3.00
V_fixture_max = 3.60
C_fixture = 0pF
L_fixture = 0nH

[Falling Waveform]
R_fixture = 50.000
V_fixture = 3.30
V_fixture_min = 3.0
V_fixture_max = 3.60
C_fixture = 0pF
L_fixture = 0nH

[Rising Waveform]
R_fixture = 50.000
V_fixture = 0.00
C_fixture = 0pF
L_fixture = 0nH

[Falling Waveform]
R_fixture = 50.000
V_fixture = 0.00
C_fixture = 0pF
L_fixture = 0nH

- For a SPICE translated model, the *_fixture values are zero.
- For a Measurement based model, use proper *_fixture values

Some simulators are sensitive in using these V/T tables. If all the sub parameters are not provided, they may resort back to the Ramp numbers and throw away the V/T tables. Consult with your EDA vendor for multiple V/T support.

V/T tables ensure accurate modeling of the switching behavior of I/O buffers.

So, you may ask, How do I generate these V/T tables for my valued customers ?

Slide13

s2ibis2 syntax for V/T

- Add these four lines in .s2i file for V/T simulation

```
[Model] 520PD_G
[Model type] I/O
[polarity] Non-Inverting
[Enable] Active-High
[Vinh] 2.0
[Vinl] 0.8
[Vmeas] 1.5
[Vref] 0.0
[Rref] 10000
[Cref] 30.0
[Model file] typ.mod min.mod max.mod
[Rising waveform] 50 0.0 NA NA NA NA NA NA
[Rising waveform] 50 3.3 NA NA NA NA NA NA
[Falling waveform] 50 0.0 NA NA NA NA NA NA
[Falling waveform] 50 3.3 NA NA NA NA NA NA
```

s2ibis2 uses the .s2i file as the control inputs for SPICE to IBIS translation.

By adding the syntax mentioned above, the model developer can easily create the 4 V/T table data in the model.

The first two fields define the Load Resistance and Load Voltage. In this example, the load used was tied 50 Ohms to GND and 50 Ohms to Vdd for all the Rising and Falling waveforms.

Consult the s2ibis2.txt documentation for detailed explanation of the syntax.

Slide14

Package/Pin data

[Pin]	signal_name	model_name	R_pin	L_pin	C_pin
1	AGND	GND	50.0m	2.52n	0.24p
2	RCLK_R/F	DS92LV1210_CTL	50.0m	1.96n	0.30p
3	REFCLK	DS92LV1210_CTL	50.0m	1.45n	0.20p
4	AVCC	POWER	50.0m	1.14n	0.14p
5	RI+	DS92LV1210_RI	50.0m	1.15n	0.05p
6	RI-	DS92LV1210_RI	50.0m	1.18n	0.08p
7	PWRDN*	DS92LV1210_CTL	50.0m	0.87n	0.07p
8	REN	DS92LV1210_CTL	50.0m	0.87n	0.07p
9	RCLK	DS92LV1210_ROUT	50.0m	1.18n	0.08p
10	LOCK*	DS92LV1210_ROUT	50.0m	1.15n	0.05p
11	AVCC	GND	50.0m	1.14n	0.14p
12	AGND	GND	50.0m	1.45n	0.20p
13	AGND	GND	50.0m	1.96n	0.30p
14	DGND	GND	50.0m	2.52n	0.24p
15	ROUT9	DS92LV1210_ROUT	50.0m	2.52n	0.24p
16	ROUT8	DS92LV1210_ROUT	50.0m	1.96n	0.30p
17	ROUT7	DS92LV1210_ROUT	50.0m	1.45n	0.20p
18	ROUT6	DS92LV1210_ROUT	50.0m	1.14n	0.14p
19	ROUT5	DS92LV1210_ROUT	50.0m	1.15n	0.05p
20	DGND	GND	50.0m	1.18n	0.08p
21	DVCC	POWER	50.0m	0.87n	0.07p
22	DGND	GND	50.0m	0.87n	0.07p
23	DVCC	POWER	50.0m	1.18n	0.08p
24	ROUT4	DS92LV1210_ROUT	50.0m	1.15n	0.05p
25	ROUT3	DS92LV1210_ROUT	50.0m	1.14n	0.14p
26	ROUT2	DS92LV1210_ROUT	50.0m	1.45n	0.20p
27	ROUT1	DS92LV1210_ROUT	50.0m	1.96n	0.30p
28	ROUT0	DS92LV1210_ROUT	50.0m	2.52n	0.24p

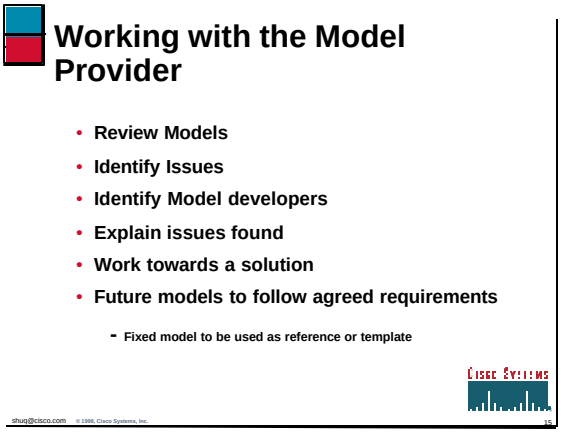
[Diff_pin]	inv_pin	vdiff	tdelay_typ	tdelay_min	tdelay_max
The '+' pin is Diff_pin and the '-' pin is the inv_pin					
5	6	0.1	0	0	0

The per-pin package numbers are the self-resistance, self-inductance and self-capacitance. Most companies involved in packaging generate package matrix with all the self and mutual numbers. They may be reluctant to give out the mutual numbers but at a bare minimum, the self-numbers should be provided.

Unfortunately only lumped values are provided through R_pkg, L_pkg and C_pkg.

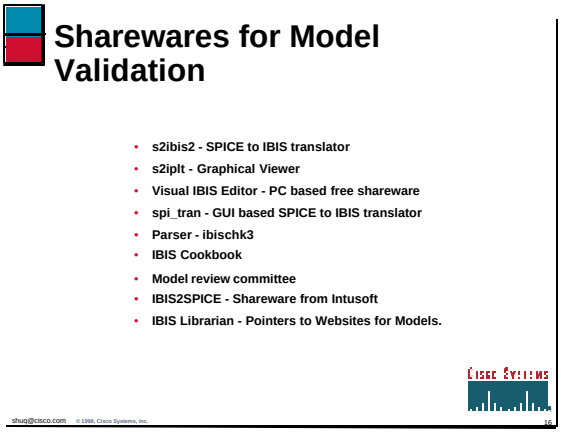
Accurate package parasitic can have an impact on high-speed Signal Integrity Analysis. IBIS also allows very detailed package modeling through 'filename.**pkg**' file. [Resistance Matrix], [Inductance Matrix] and [Capacitance Matrix] can be defined within the package model.
I have never seen one and most likely they are available through NDA(Non Disclosure Agreement).

Slide15



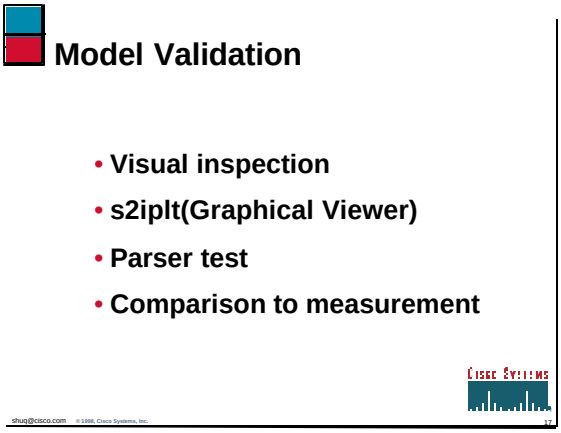
Some vendors are very responsive and work as a team to help their customers. Vendors who value the business, always respond co-operatively to provide solutions in a timely manner.
In many cases IBIS models are generated on a request basis. That is too late!
As soon as the SPICE models are 'frozen' for a specific design, an IBIS model should be generated through SPICE translation. Once Silicon is available, the IBIS model should be refined to represent real world behavior.

Slide 16



The IBIS community provides various kinds of tools from its website for FREE:
s2ibis2: This shareware from NCSU translates SPICE models to IBIS. Various commercial and non-commercial SPICE engines are supported.
s2iplt: This is also another utility provided with the s2ibis2 tool from NCSU. This Perl script uses GNUplot to graphically plot the V/I and V/T tables.
Visual IBIS Editor: Hyperlynx provides a shareware that can help develop and test IBIS models on a PC platform. Graphical viewer, parser test and other functions are available.
spi_tran: Cadence provides this shareware which is a Java based GUI for easy input of all the SPICE-to-IBIS parameters required for s2ibis2 translation.
Parser: The IBIS parser(ibischk3)is available for FREE download from the IBIS website and supports multiple OS's and computing platforms.
IBIS Cookbook: Detailed descriptions of IBIS model development with all sorts of tips are available through the cookbook.
Model Review Committee: A committee comprising of various EDA vendors can review your IBIS model and provide confidential feedback to the developers. This support is FREE and available only to model developers.
IBIS2SPICE: Intusoft provides a shareware that can take an IBIS model and translate back to SPICE.
IBIS Librarian: The official EIA IBIS Librarian can create a link to your IBIS model website from the EIA IBIS webpage. Contact the librarian with your company's URL.

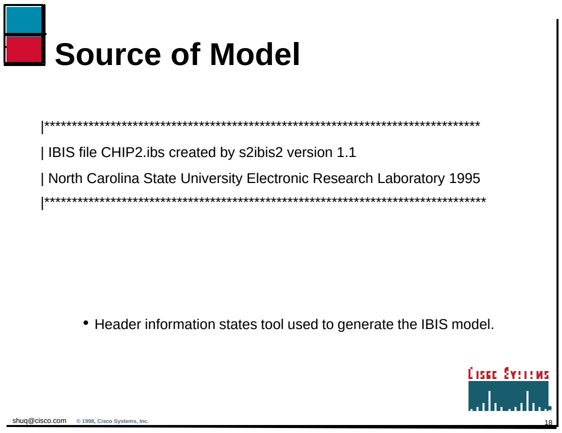
Slide17



A series of steps needs to be followed in validating a model. Most models are available

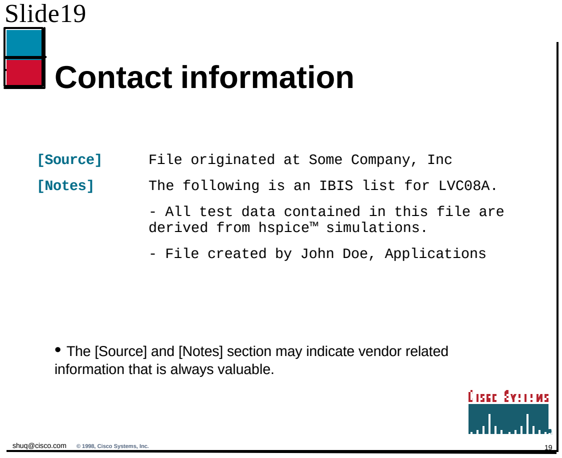
for download through the web or available through contracting services.
The next couple of sections will walk the user through a number of steps in validating an IBIS model.

Slide18


Source of Model
|***
| IBIS file CHIP2.ibs created by s2ibis2 version 1.1
| North Carolina State University Electronic Research Laboratory 1995
|***
• Header information states tool used to generate the IBIS model.
shuq@cisco.com © 1998, Cisco Systems, Inc.
18

It is a useful piece of information to understand if the model was generated through SPICE translation or measurement. Typically if the s2ibis2 tool was used, a header appears at the top of the IBIS model stating the version and name of the translator.

Slide19


Contact information
[Source] File originated at Some Company, Inc
[Notes] The following is an IBIS list for LVC08A.
- All test data contained in this file are derived from hspice™ simulations.
- File created by John Doe, Applications
• The [Source] and [Notes] section may indicate vendor related information that is always valuable.
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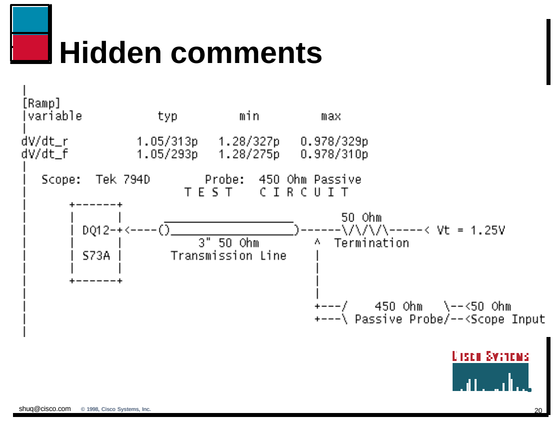
19

The [Source] and [Notes] section of the IBIS model can contain some very useful information. Often times they are not used effectively by the model developers. These sections may contain contact information, process geometry used for the particular device, versions of SPICE used, website information etc.

Slide20


Hidden comments
[Ramp]
|variable typ min max
dV/dt_r 1.05/313p 1.28/327p 0.978/329p
dV/dt_f 1.05/293p 1.28/275p 0.978/310p
| Scope: Tek 794D Probe: 450 Ohm Passive
T E S T C I R C U I T
DQ12
S73A
50 Ohm
Vt = 1.25V
3" 50 Ohm
Transmission Line
Termination
450 Ohm
50 Ohm
Passive Probe
Scope Input
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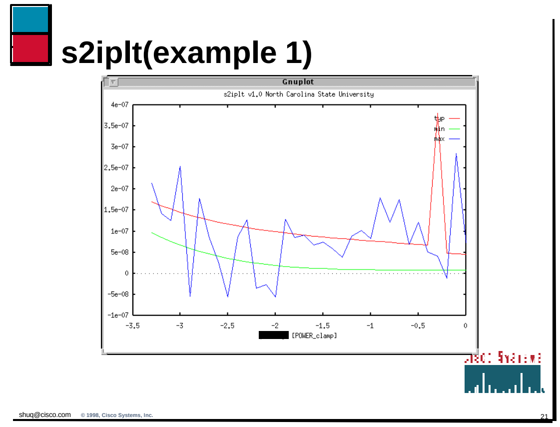
20

IBIS uses the "|"(Pipe)character as a comment. Since the model is an ASCII file, the model developer can attach various pieces of information for the user and these are enclosed as comments so it does not interfere with the model.
This may not be evident unless the user opens the file and scrolls through them. Above is an example of a vendor who provided the complete AC Test Circuit conditions under which the [Ramp] data was derived.
Other types of information can also be found. There could be detailed information or choices of parameters some of which are enabled(not commented out) while others are available but disabled(by using the comment character).
Model users should scan through the IBIS model file to see if such comments are there or not.

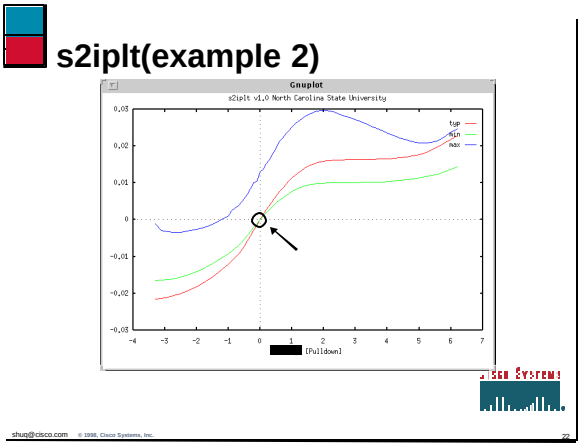
Slide21



It is highly recommended to plot out the V/I and V/T curves. A graphical view can show various strange details that you may miss in the ASCII file.

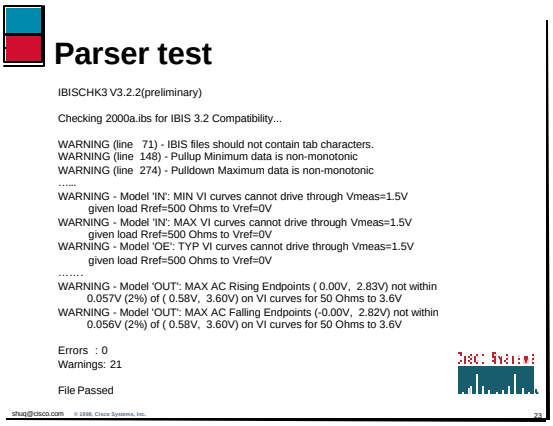
This is a [Power Clamp] data of a model. The vendor never bothered to view the data before distributing the model. While the scale shows very little current, this sort of non-monotonic data can throw off some simulators.
For V/T data, graphical viewing of the switching waveform is critical. Some weak buffers may not be able to drive 50 Ohm(heavy load)and you may see a 'flat' line over the entire sweep range.

Slide22



Somehow one of the process corner(max)never go through the 0,0 point of the [Pulldown] curve. Most likely an offsetting error and this should be checked out.
Sometimes a SPICE simulation may not converge over the full IBIS specified sweep range. In that case the user tweaks the sweep range
to the point it converges and then extrapolates the data to the end point.
All the Typ, Min and Max tables need to span the proper voltage ranges(since each is referenced to it's own Vdd value). Since [Pullup] V/I tables are offset by Vdd, this becomes a critical step.
Many other instances of 'strange' data can be shared but the importance of plotting out the data is very critical.
This is a valuable step for both the Model developer and the end user.

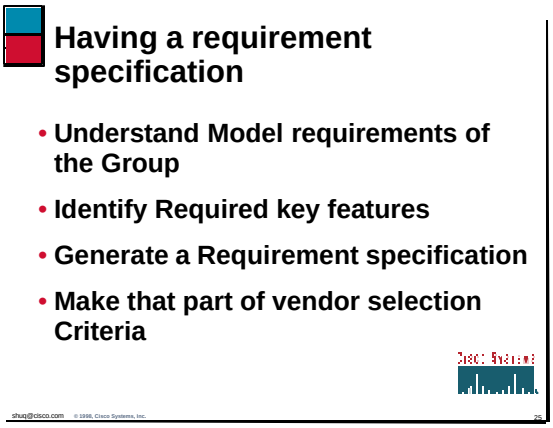
Slide23



It is surprising that quite a number of models are not parsed through the parser test. This FREE parser is available on multiple OS platform from the IBIS website.
A parser test checks if the ASCII model file syntactically conforms to the specification. It is highly recommended by the IBIS committee to run ibischk3(ver3.2) even if the generated model is IBISv2.1 or below.
The Parser flags WARNING and ERROR messages with line#s and descriptive information.

Slide 24 – Unavailable at time of print

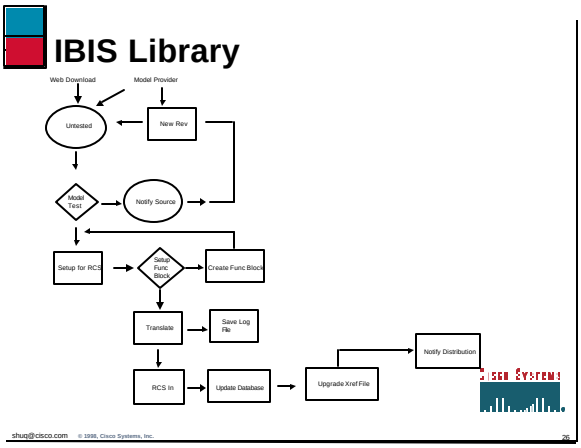
Slide25



There are instances where a user is unable to obtain a model or there is a lack of response from the model developer. This situation forces the end user to develop a 'Requirement Specification', which eventually ties to a Purchase Order.

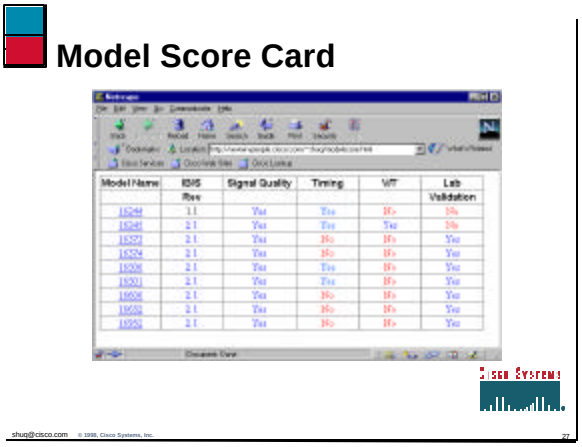
If the vendors fail to provide models, they are dropped from the preferred vendor list or in some cases not chosen for business.
Various items shared in this paper can be compiled into such a 'Requirement Specification'. Such a specification can be continually refined to meet the Analysis needs by making use of advanced features of the IBIS specification.

Slide26



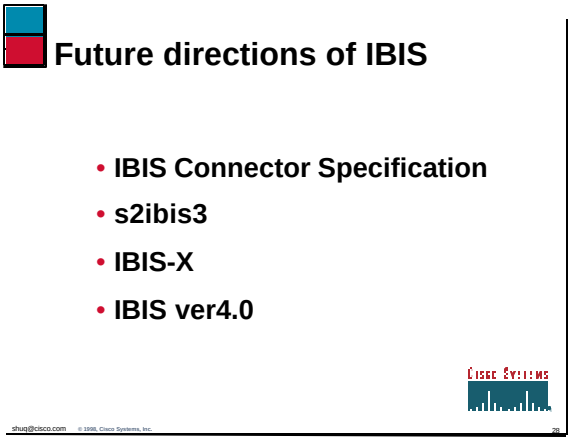
A typical IBIS library management scheme is illustrated above. Model validation, revision control and proper database management is key to having an effective library.

Slide27



Once a good model library is in place. A web based library search can easily be implemented. There could be a 'Model Score Card' feature that allows the model user to understand the quality of the model and what type of Analysis should be attempted with the current version available in the Library. This could also indicate if it's an un-validated model(no measurement data) etc.

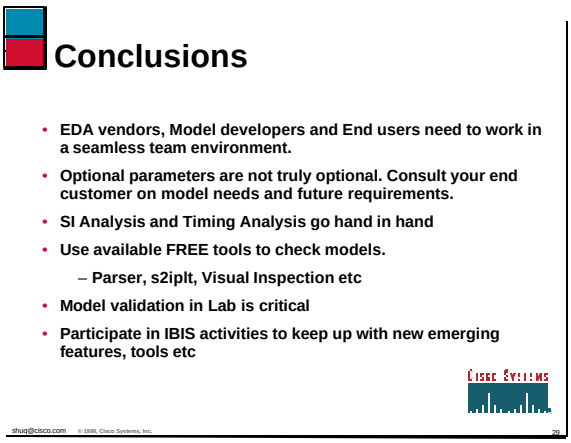
Slide28



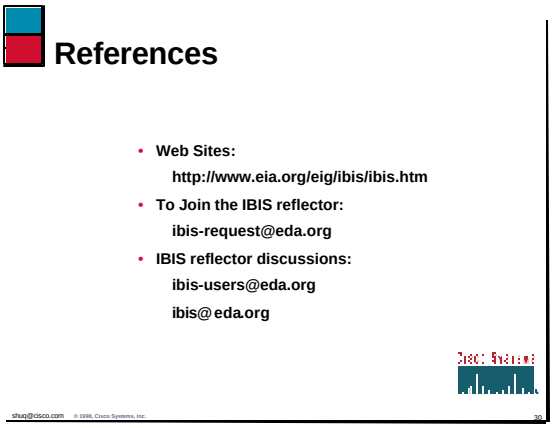
IBIS Connector Specification:
An IBIS subcommittee worked on creating a very detailed specification on Connector modeling. This specification is available for download from the IBIS website.
s2ibis3 project:
Another IBIS subcommittee worked on creating a project requirement specification to generate the next generation of SPICE-to-IBIS translator. Funding and contracting of this project is underway.
IBIS - The next generation:
Various levels of technical discussions are going on regarding IBIS and the next level of the specification.

For more detailed and updated information, visit the website or the IBIS teleconference.

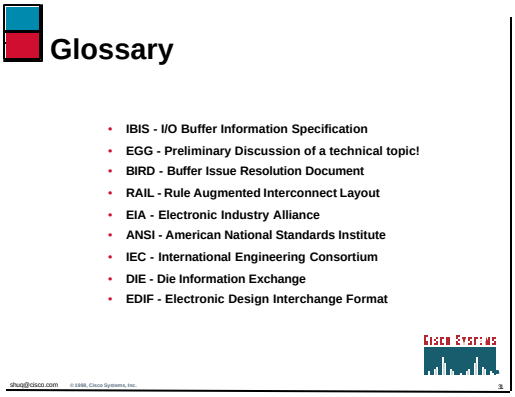
Slide29



Slide30



Slide31



The IBIS website contains a lot of information including:

Articles: Recent articles in Electronic Design, EDN, and various other seminars regarding IBIS are presented here.
FAQ's: Frequently Asked Questions about IBIS as well as s2ibis are available
Models: There is about 13 links to semiconductor companies providing IBIS models from their web site today. If you wish your site to be referenced, inform the webmaster.
FREE Tools: Helpful tools to generate IBIS model are listed. This includes cookbook, parser, s2ibis2, s2iplt etc
Specification: All IBIS specifications are available here
Support: Reflection information as well as Model Review Services.
Virtual member poster: Links to IBIS member company websites are available through this virtual poster page.
Roster Listing: Contact information including name, phone, fax, E-mail and website(if any)are shown here for both member and non-members of ANSI/EIA-656
More tools and helpful utilities will be made available from this site in the near future.
Upcoming Events: Calendar of events related to IBIS.

And many more..