

IBIS “Gate Modulation Effect” Proposal

The level 1 equation of a MOS is the following:

$$y = \{[2(v_{gs}-0.6)x - x^2]u(v_{gs}-x-0.6) + (v_{gs}-0.6)^2u(x-v_{gs}+0.6)\}u(v_{gs}-0.6)$$

it describes the Id-Vds characteristic, parameterised by Vgs voltage (Fig.1). These characteristics are related to a 0.6V threshold voltage.

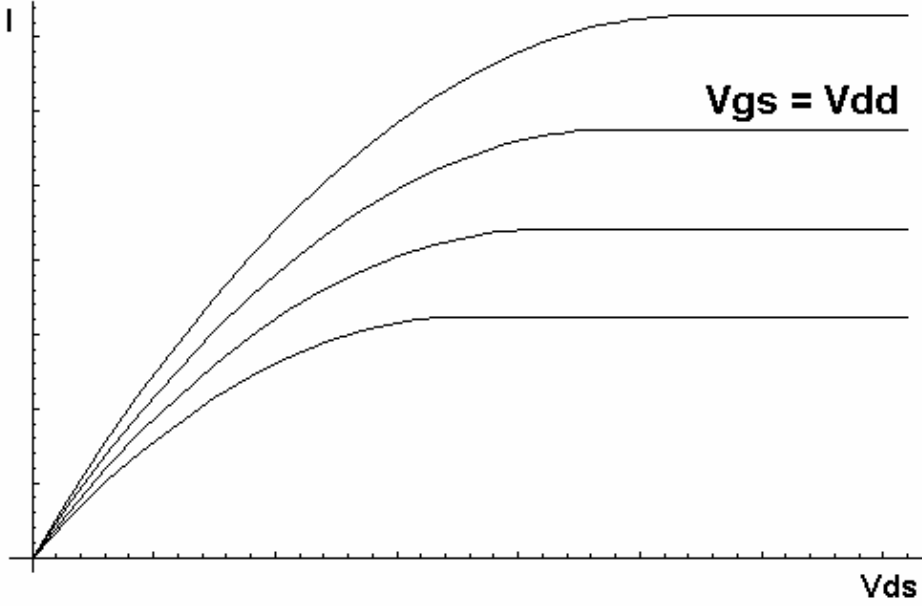


Fig. 1

To overcome the IBIS “Vgs modulation effect” criticality, we have considered the two following coefficients:

$$k_{ssn-pulldown} = \frac{I(v_{gs}, v_{ds})}{I(v_{gs}=v_{dd}, v_{ds})}$$

$$k_{ssn-pullup} = \frac{I(v_{sg}, v_{sd})}{I(v_{sg}=v_{dd}, v_{sd})}$$

in order to modulate the Id value when the Vgs changes respect to the nominal value (Vgs=Vdd) reported in the IBIS file.

Therefore, the equation of the effective current (Ieff) is the following

$$I_{eff} = K_{ssn}(V_{gs}, V_{ds}) * I_{std}$$

where Istd is the standard current for Vgs=Vdd.

The equation of the Kssn coefficient, based on the level 1 MOS equation, is the following:

$$k_{ssn-pulldown} = \frac{[2(v_{gs} - 0.6)x - x^2]u(v_{gs} - x - 0.6) + (v_{gs} - 0.6)^2u(x - v_{gs} + 0.6)}{[2.4x - x^2]u(v_{gs} - x - 0.6) + (1.2)^2u(x - v_{gs} + 0.6)}$$

For a fixed value of the V_{ds} , sweeping the V_{gs} and collecting the related I_d values in a table, it is easy to calculate the correspondent values of the K_{ssn} coefficient.

Looking at the MOS characteristic we understand that we should extract a lot of tables, by fixed steps of the V_{ds} changes.

Nevertheless, considering the graphic of the SSN coefficient (Fig.2), based on the MOS level 1 equation, you can note that when the MOS is in the saturation zone, the K_{ssn} coefficient is independent from the V_{ds} , therefore it suggests us that one table can be used to describe correctly the V_{gs} modulation effect in the saturation zone.

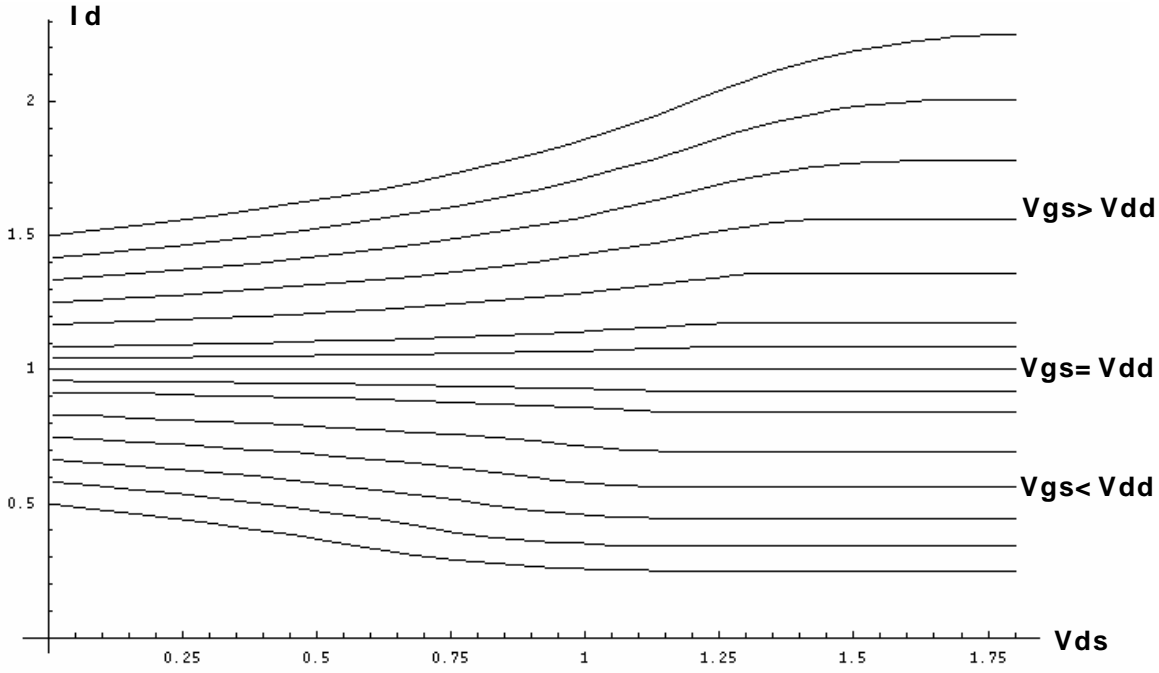


Fig. 2

This hypothesis is also justified considering that during the first bouncing the V_{gs} decrease, the MOS saturation zone is larger, therefore the K_{ssn} coefficient is independent from V_{ds} in a larger region. We have chosen to extract the V_{gs} - I_d table for $V_{ds}=V_{dd}$.

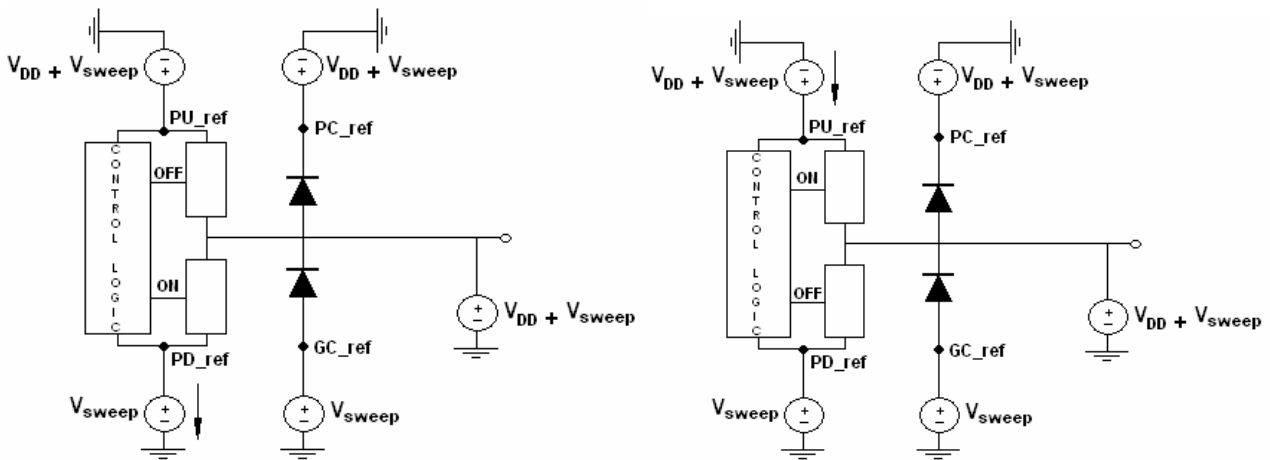


Fig. 3

Firstly, we had considered the two circuits shown in the figure 3 for extracting the tables of Pullup and Pulldown, respectively. The V_{sweep} range is $[-V_{\text{DD}}, +V_{\text{DD}}]$ in the both case.

Afterwards, we have found out that these circuits are not correct when the control logic is powered by the same supply of the final stage, in this case the behaviour of the control logic and its driving capability to final stage is not modelled correctly. In fact, if a bouncing occurs on the gnd node, it will propagate to the V_{DD} node by the V_{DD} -Gnd capacitance and it will be in phase with the gnd noise, but the magnitude will be lower.

Therefore, it is not correct to apply the same V_{sweep} to both gnd and vdd nodes because during the dynamic of bouncing the noise amplitude will be different.

To avoid this problem we have considered the modified circuits reported in the figure 4.

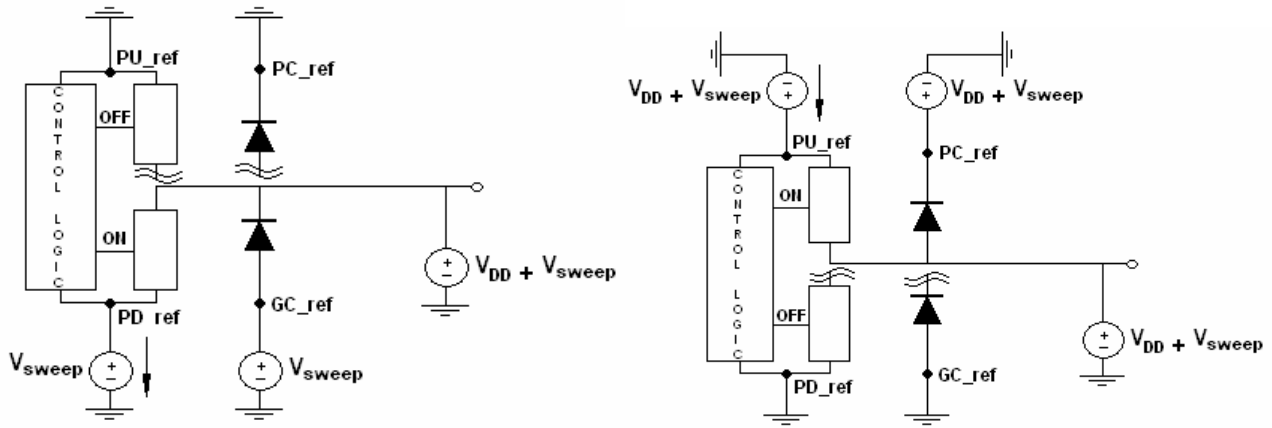


Fig. 4

We have implemented the SSN coefficients in the VHDL-AMS language, starting from the VHDL-AMS IBIS description proposed by Muranyi.

In the figure 5 and 6 are shown the results of the simultaneous switching output (16 output buffers of a Flash memory) for rise and fall transition.

The matching between IBIS and SPICE are very well for output signal and for the power and ground bouncing.

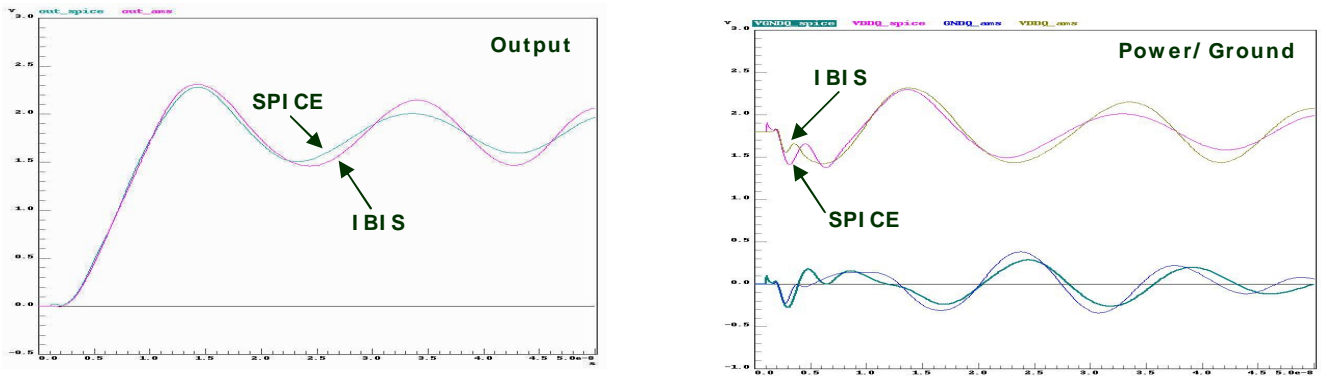


Fig. 5

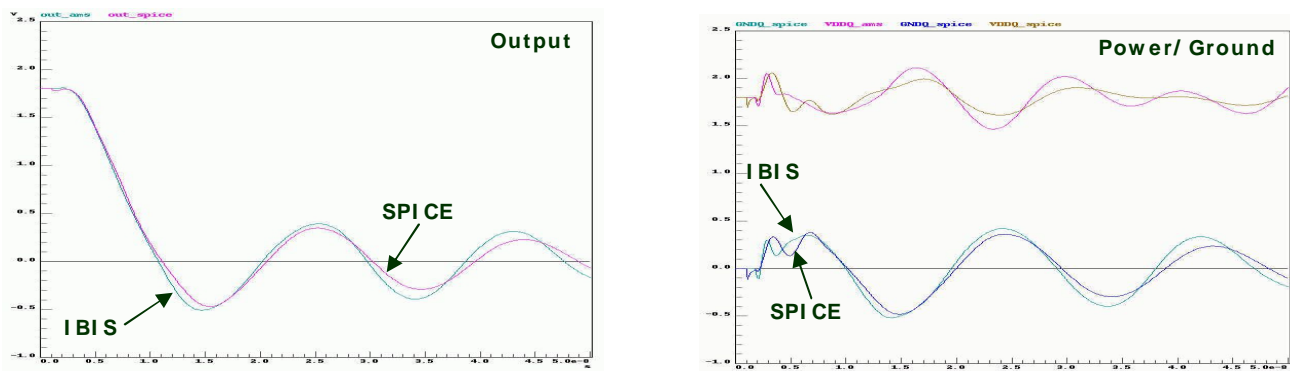


Fig. 6

Nowadays we are also analysing a solution with two tables, one in the saturation zone and one in the linear zone, for taking into account the “V_{gs} modulation effect” when the operating point is in the linear zone.

We are considering the interpolation diagram shown in the figure 7, where K1 and K2 are the K_{ssn} coefficients in the linear and saturation zone respectively; V2 is the voltage for which starts the saturation zone (V_{gs}-V_{th}) and V1 is an estimated voltage where the linear zone starts. The transition between the two zones (the knee zone) is interpolated linearly.

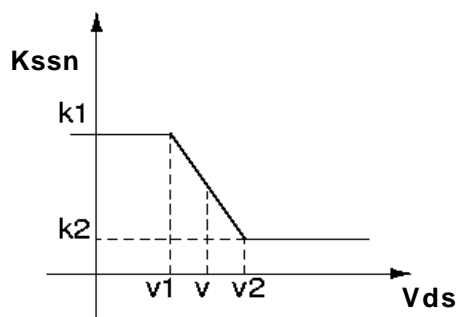


Fig. 7

The simulations of the two tables’ implementation are on going.

For any comment and/or feedback, please contact

Antonio Girardi
Memory Products Group
CAD Group Leader
IBIS Modeling & Signal Integrity Analysis
STMicroelectronics
Tel: +39-081-2381239
antonio.girardi@st.com