Quiet line experiment

IBIS Open Forum Teleconference

October 7, 2005

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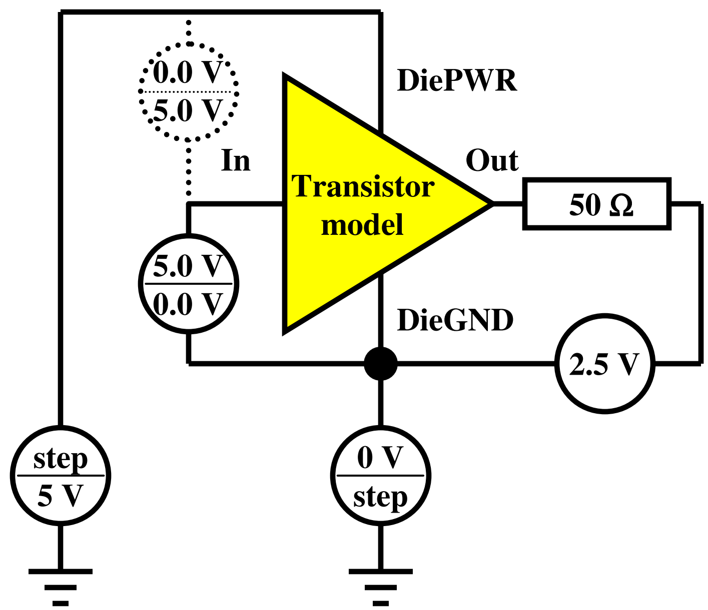
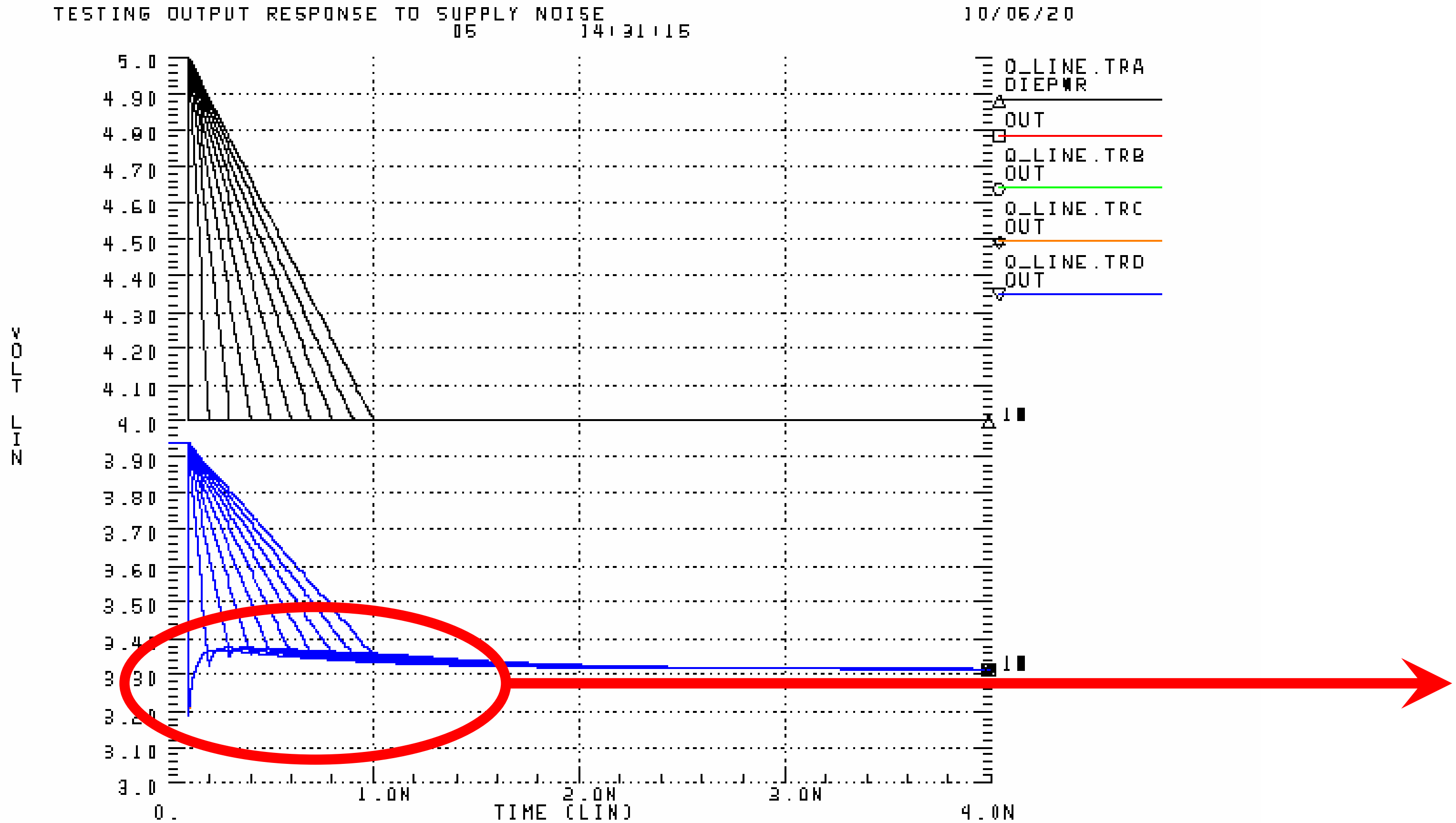
Simulation circuit using "IBIS class" transistor model



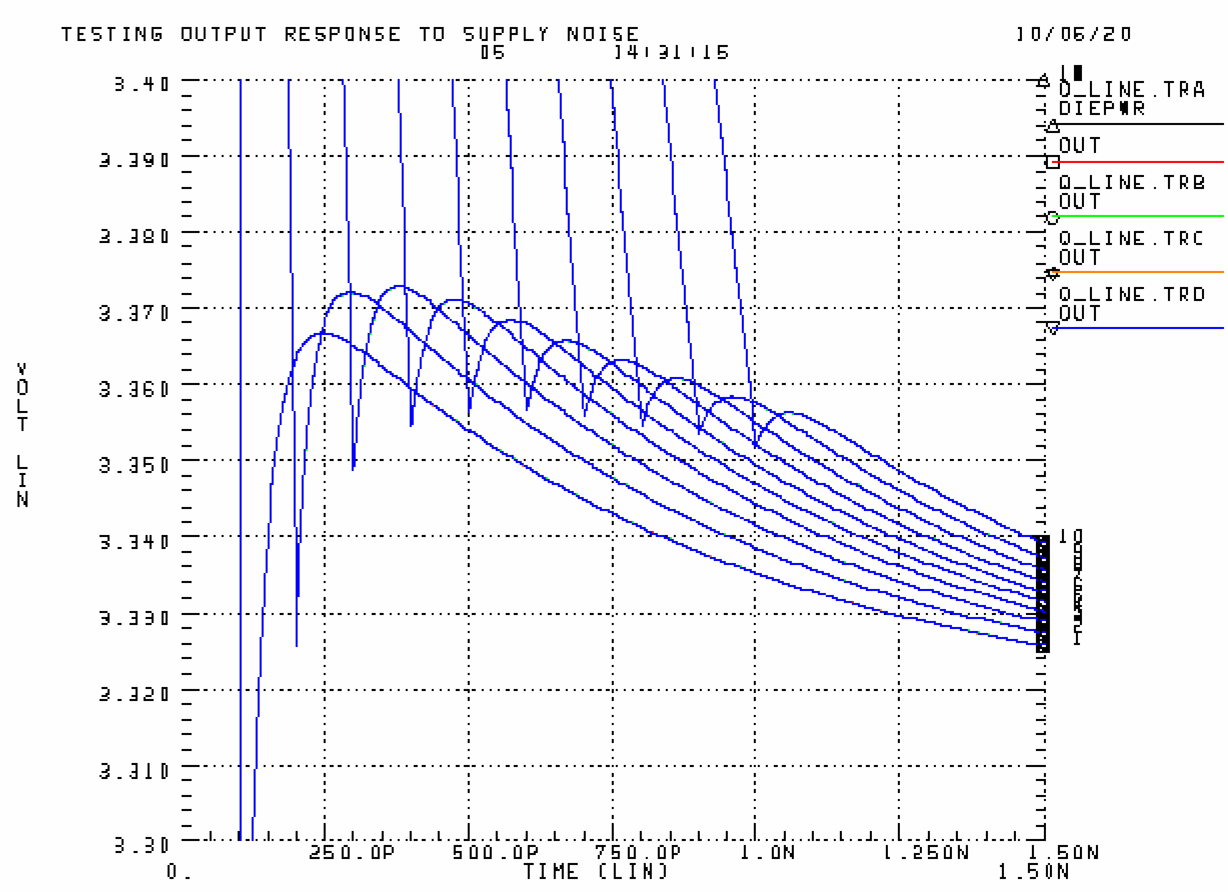
HSPICE simulation file

```
Testing Output Response to Supply Noise
**********************************************************************
.OPTIONS POST=1 POST_VERSION=9007 PROBE  ACCURATE  RMAX=0.5
.TRAN 1.0ps  4.0ns  SWEEP  Tpoint  LIN  10  101e-12 1001e-12
.LIB  'Process.lib'  Typ
**********************************************************************
.PROBE
+ DiePWR = V(DiePWR,DieGND)
+ DieGND = V(DieGND)
+ Out    = V(Out,DieGND)
**********************************************************************
.param Tpoint = 101ps
*
*Vvcc  DiePWR  0  DC= 5.0
Vvcc  DiePWR  0  PWL
+  0.0        5.0
+  0.1ns      5.0
+  Tpoint     4.0
+ 10.0ns      4.0
*
Vgnd  DiePGND  0   DC= 0.0
*Vgnd  DieGND  0   PWL
*+  0.0        0.0
*+  0.1ns      0.0
*+  Tpoint     1.0
*+ 10.0ns      1.0
*
Vin   In      DieGND  DC= 5.0
*Vin   DiePWR  In      DC= 0.0
**********************************************************************
X0  In  Out  DiePWR  DiePWR  DieGND  DieGND  DieGND  IO_buf
*   in  out   pu      pc      pd      gc      en
*
Rload  Out  Vtt     R=  50.0
Vload  Vtt  DieGND  DC=  2.5
**********************************************************************
.END
**********************************************************************
```

The four configurations give identical results (high state)



Zooming in to see the details…



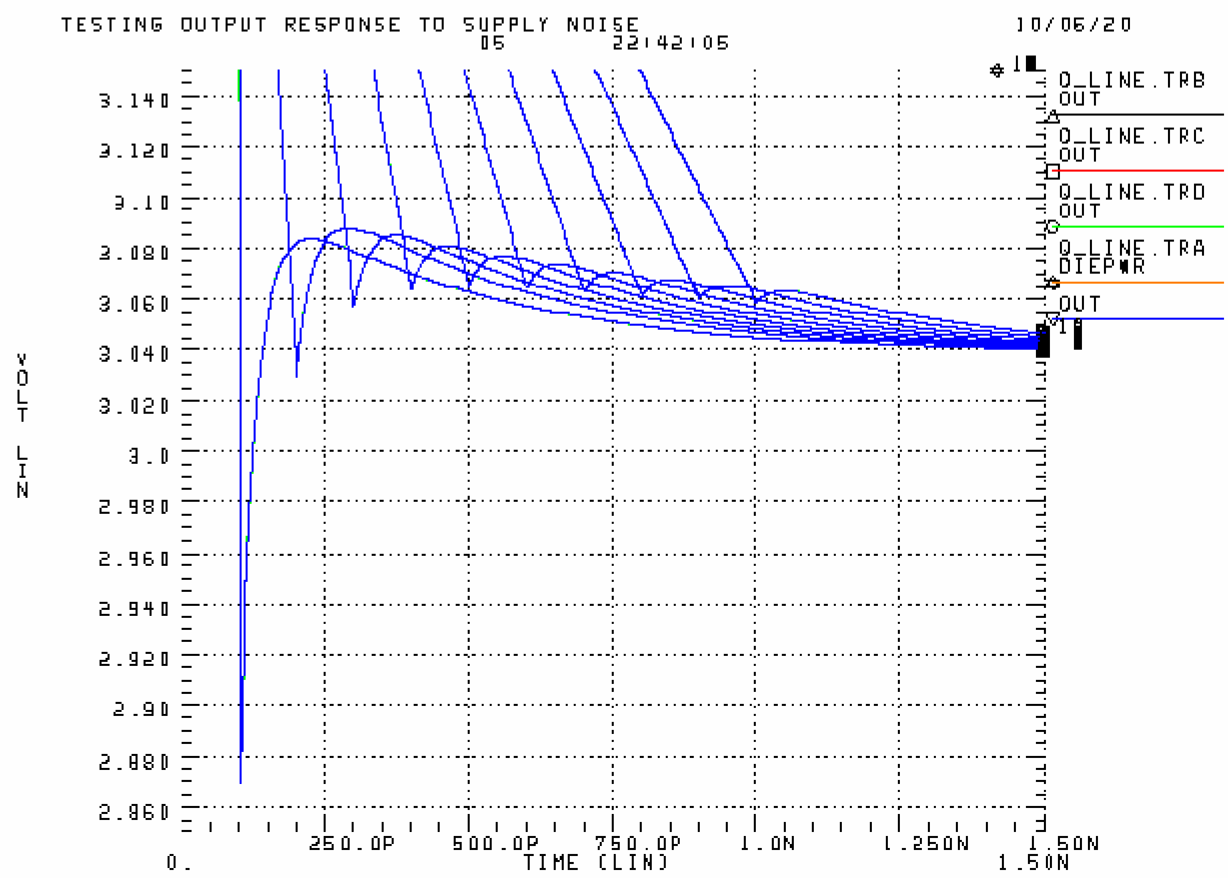
Make the PU and PD asymmetric

```
*****************************************************************************
.SUBCKT  IO_buf  d_in pad DiePWR p_clamp DieGND g_clamp enable
*****************************************************************************
X1  enable  en_b           DiePWR  DieGND  INVERTER
X2  d_in    en_b    pre_p1 DiePWR  DieGND  NAND2
X3  d_in    enable  pre_n1 DiePWR  DieGND  NOR2
X4  pre_p1  pre_p2         DiePWR  DieGND  INVERTER  mult_p=2  mult_n=2
X5  pre_n1  pre_n2         DiePWR  DieGND  INVERTER  mult_p=2  mult_n=2
X6  pre_p2  pre_p2  gate_p DiePWR  DieGND  NAND2     mult_p=4  mult_n=2
X7  pre_n2  pre_n2  gate_n DiePWR  DieGND  NOR2      mult_p=2  mult_n=4
*
Mp  pad gate_p DiePWR  p_clamp  PMOS  L=0.800U W=43.40U NRD=0.0897 NRS=0.0737
+                                AS=434.0P AD=217.0P PS=106.8U PD=53.40U
+                                M=12
Mn  pad gate_n DieGND g_clamp   NMOS  L=0.800U W=43.40U NRD=0.0897 NRS=0.0714
+                                AS=434.0P AD=217.0P PS=106.8U PD=53.40U
+                                M=6
*C1  pre_p2  DieGND  C=0.07pF
*C2  pre_n2  DieGND  C=0.07pF
*C3  gate_p  DieGND  C=0.04pF
*C4  gate_n  DieGND  C=0.03pF
*
R1  pad     rcv_in  R=200
*C5  rcv_in  DieGND  C=0.2pF
X8  rcv_in  rcv_out        DiePWR  DieGND  INVERTER
*
```

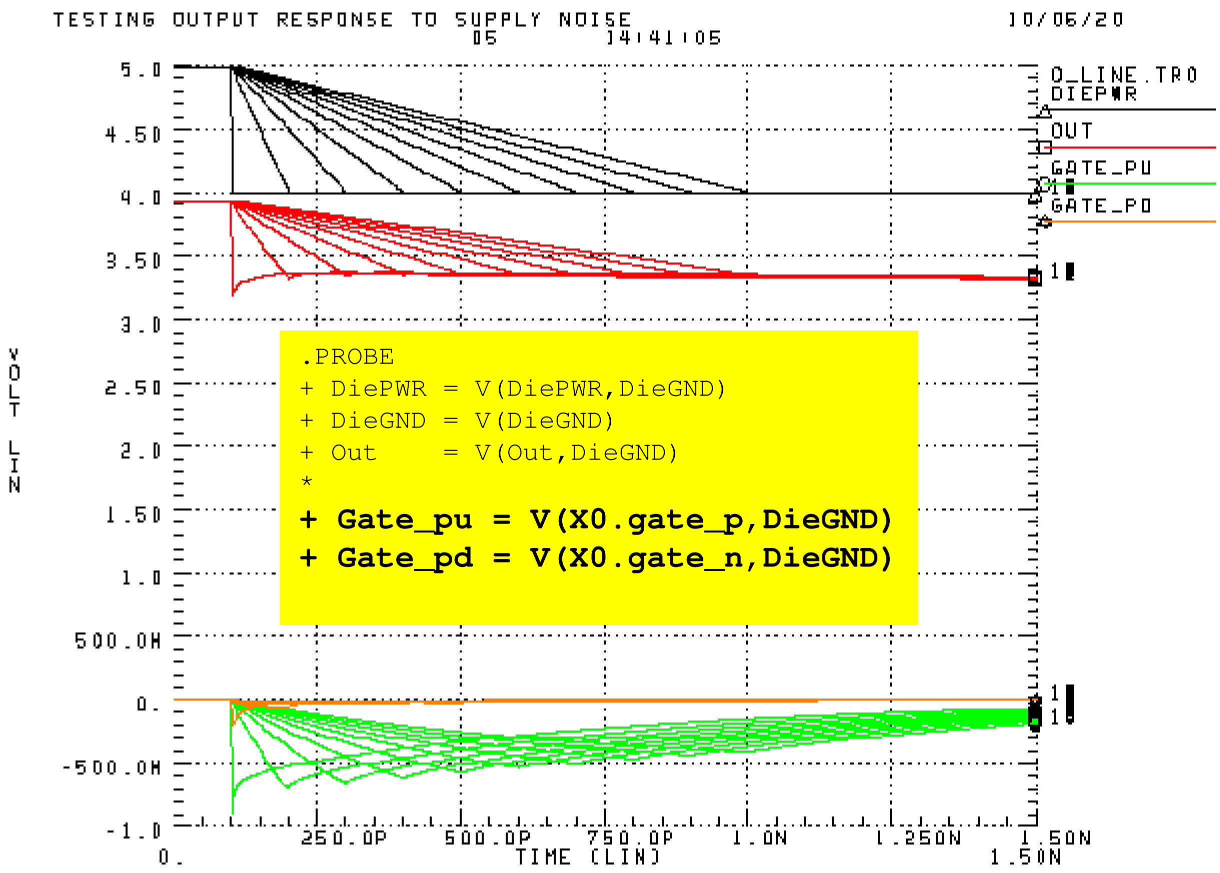
Chaged to M=6 to make PU and PD asymmetric

Adding or removing these capacitors doesn’t make the agreement between the four conditions any weaker

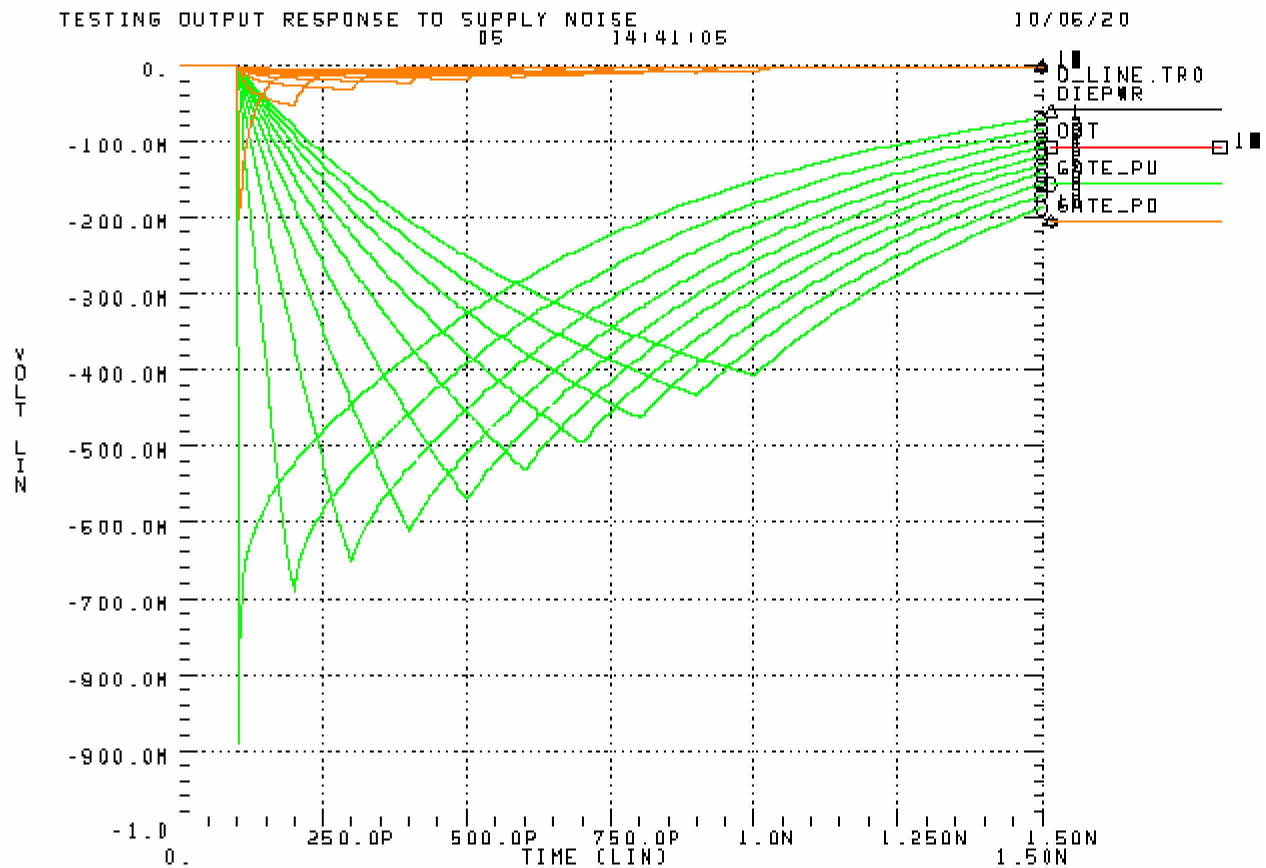
PU reduced to half the strength - High state



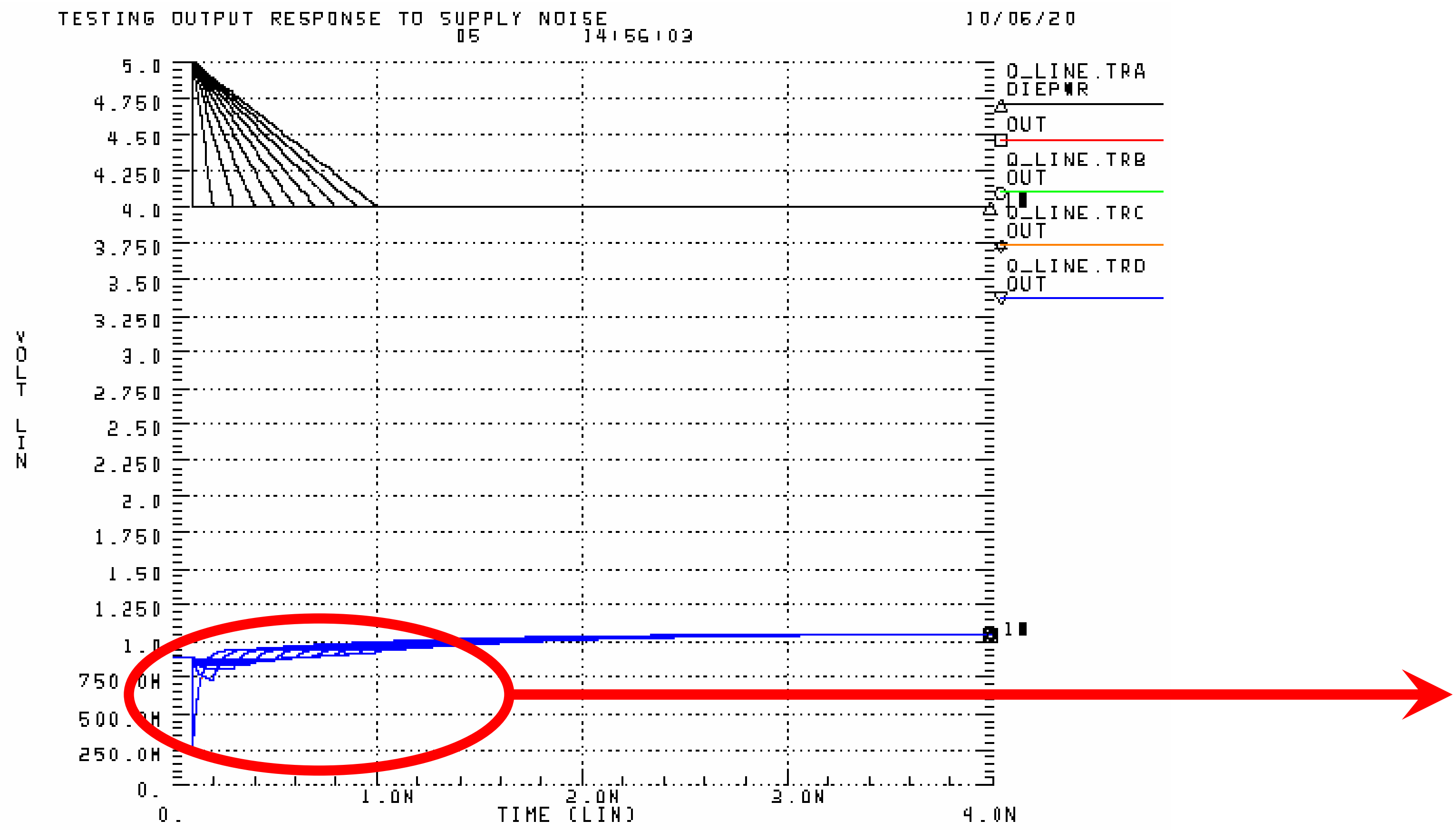
Gate voltage of the output transistors



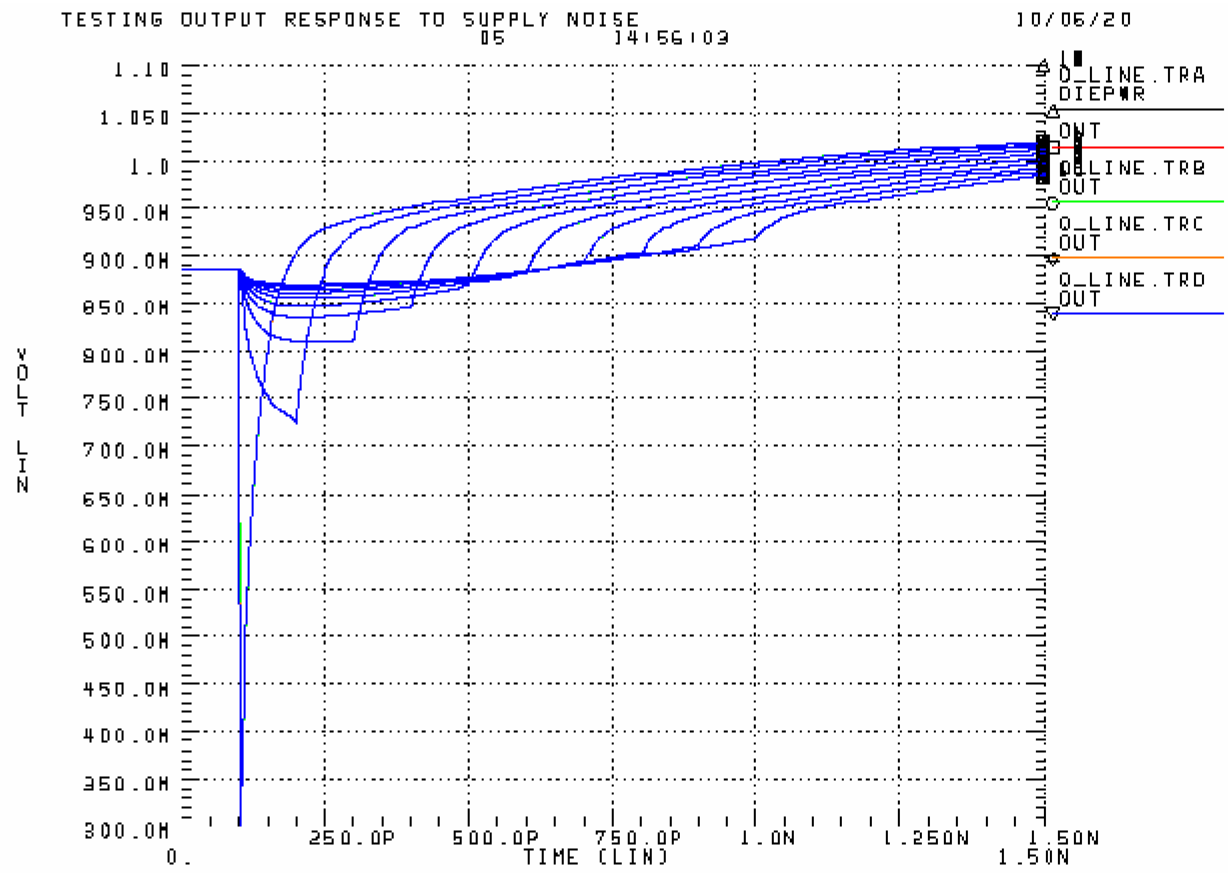
Zooming in to see the details…



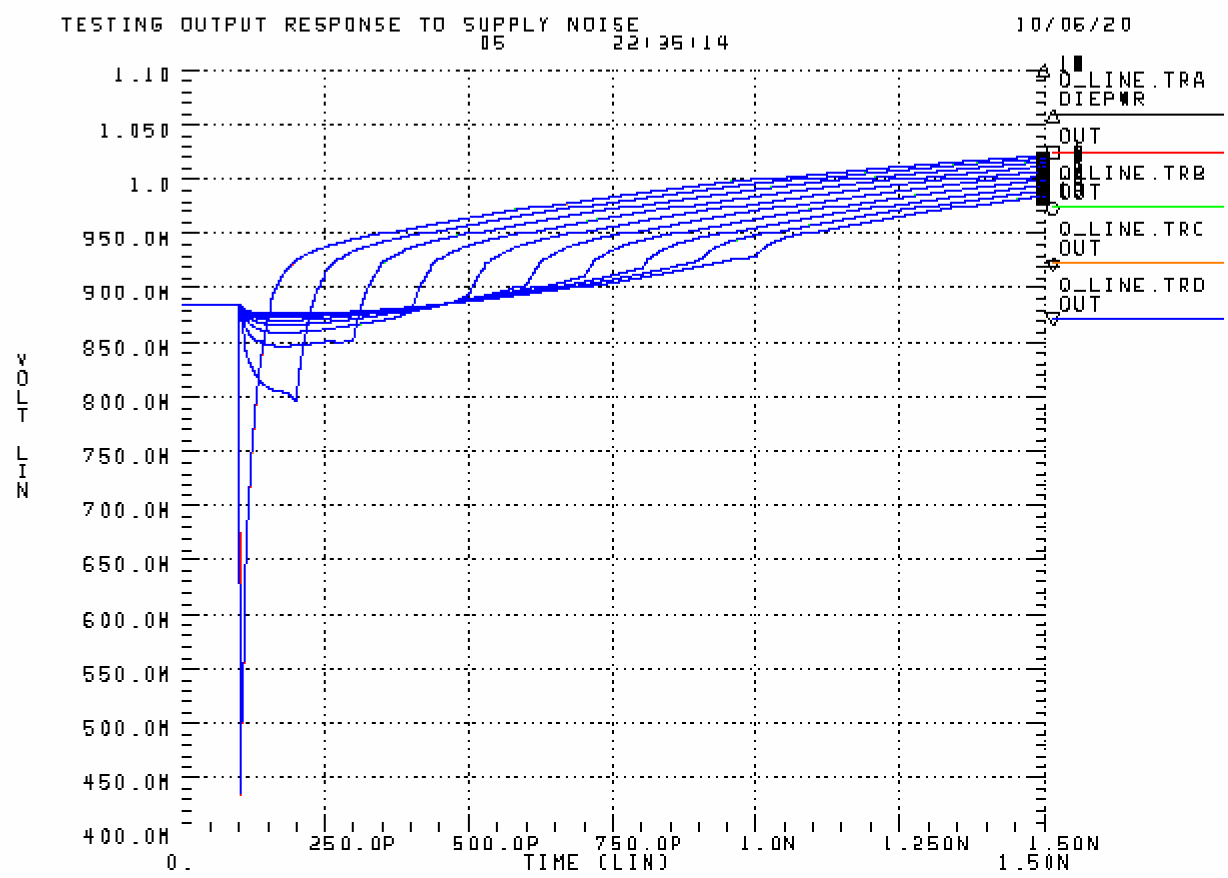
The four configurations give identical results (low state)



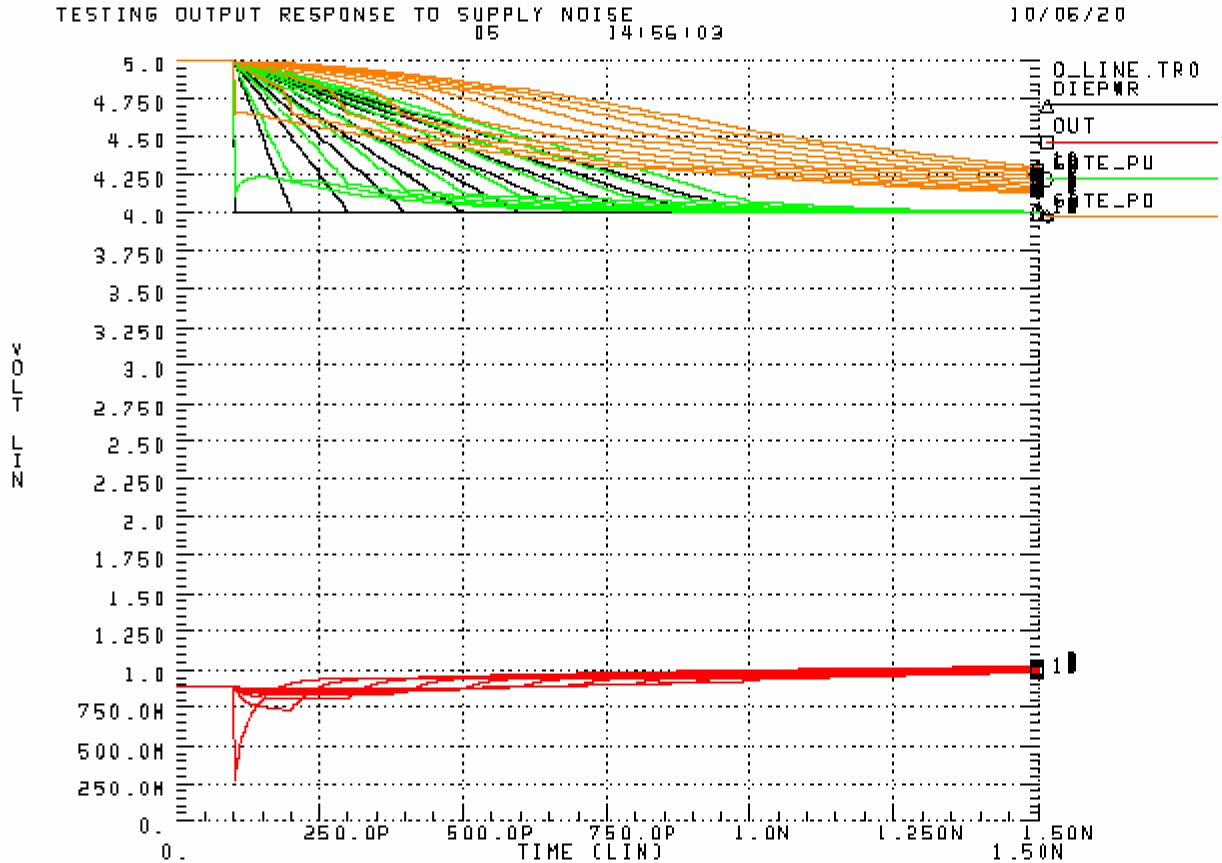
Zooming in to see the details…



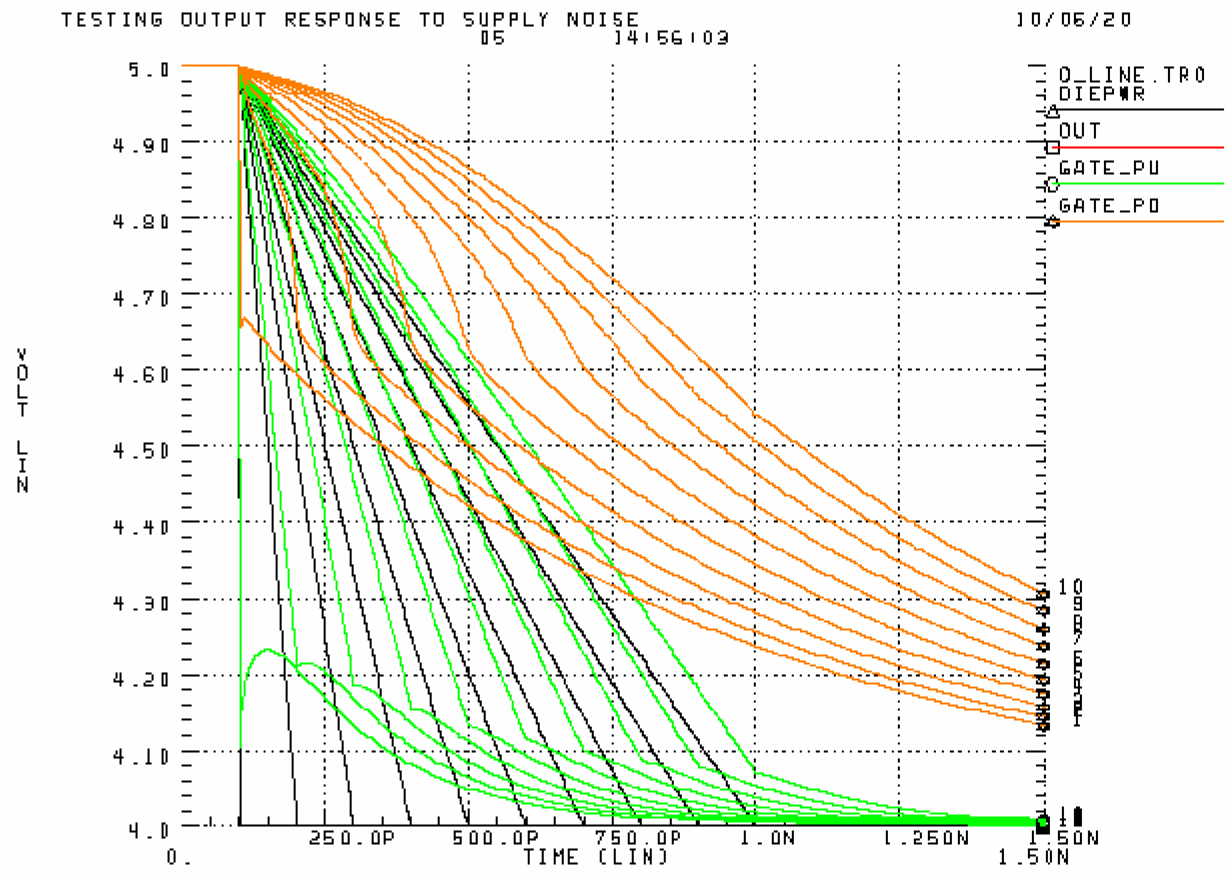
PU reduced to half the strength - Low state



Gate voltage of the output transistors



Zooming in to see the details…



Conclusions

- **Whether we are modulating the top or bottom supply voltage *DOES NOT MATTER***
- **Due to internal RC effects the gate voltage of the output transistors will not be able to follow rapid supply voltage variations instantaneously**
- **The gate modulation effect cannot be modeled by DC measurements alone**
- **We have to find a good way to describe these AC effects in a general way before BIRD97/98 can be completed**

Part II: Gate modulation and BIRD 97/98

IBIS Futures Teleconference

June 1, 2006

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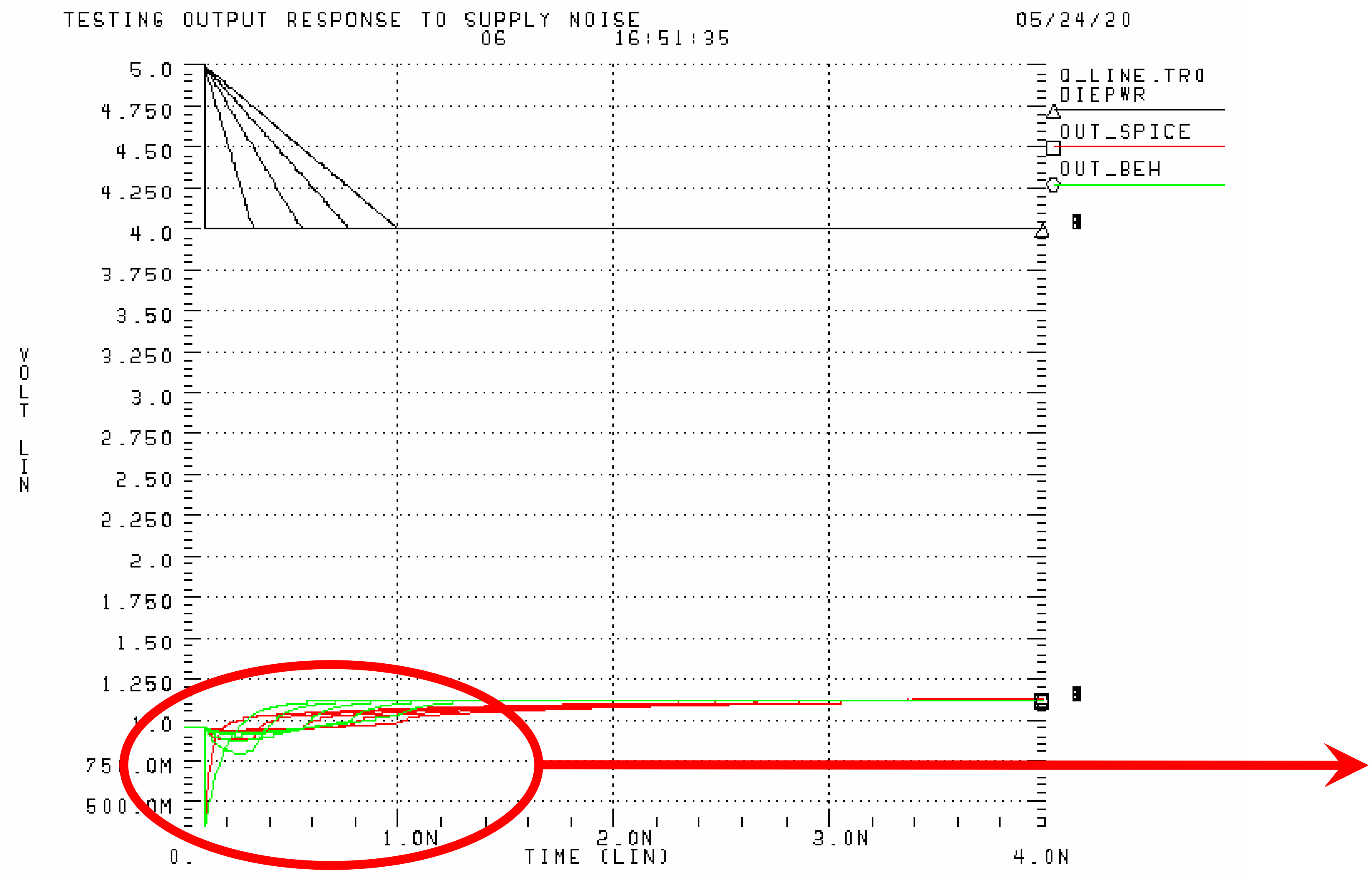
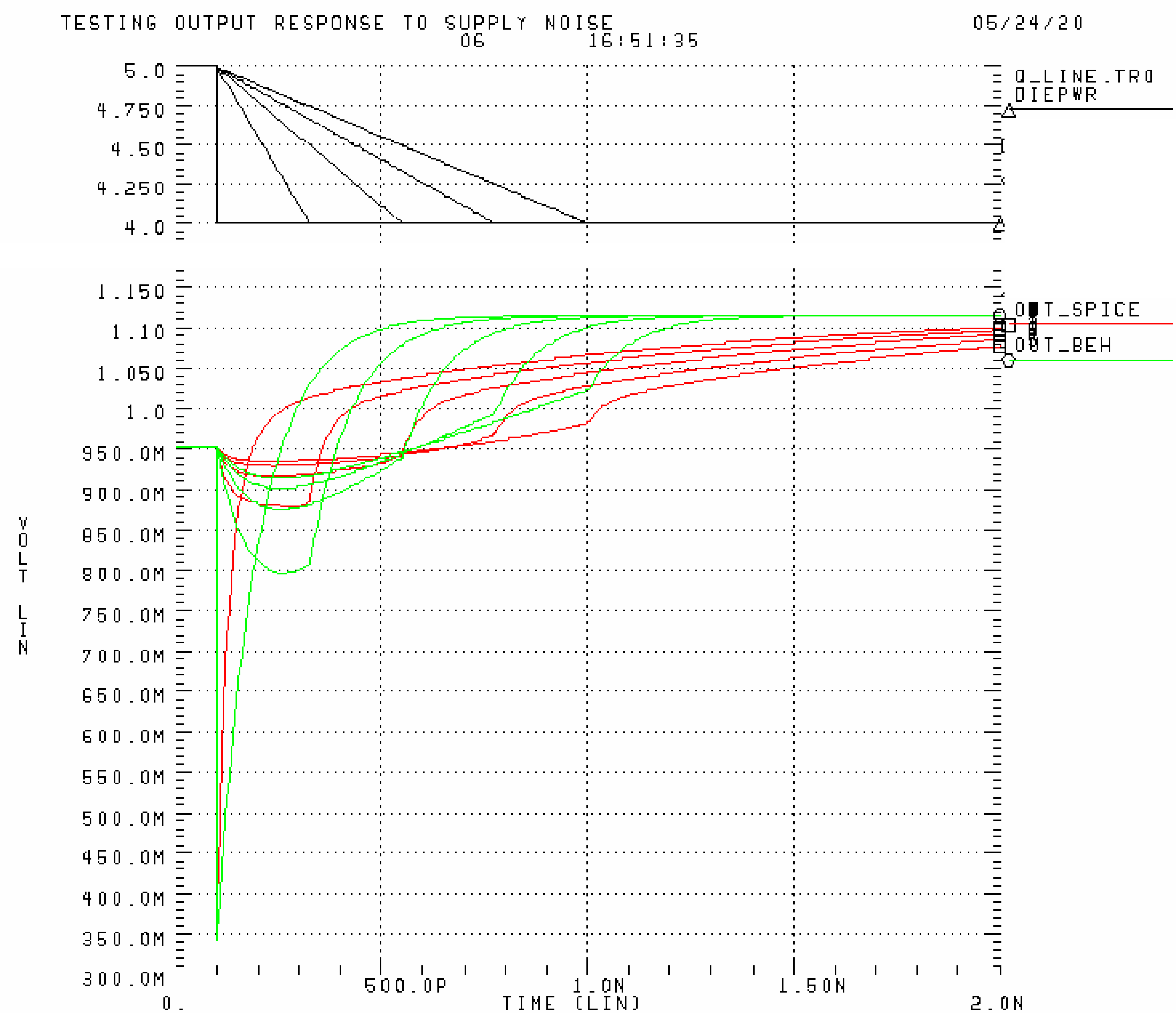
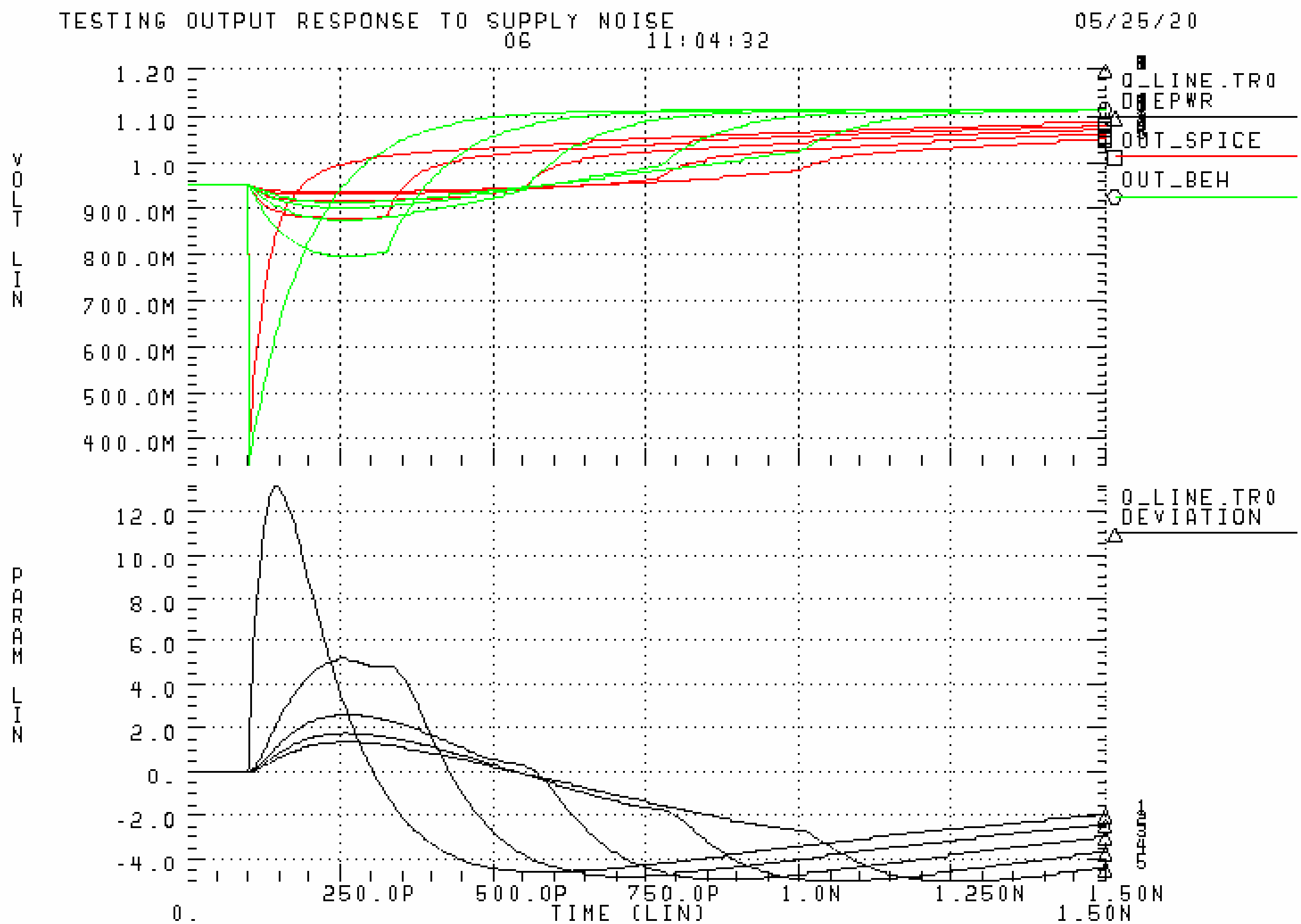
Linear scaling of I_{out} w/r V_{power} (Low state)



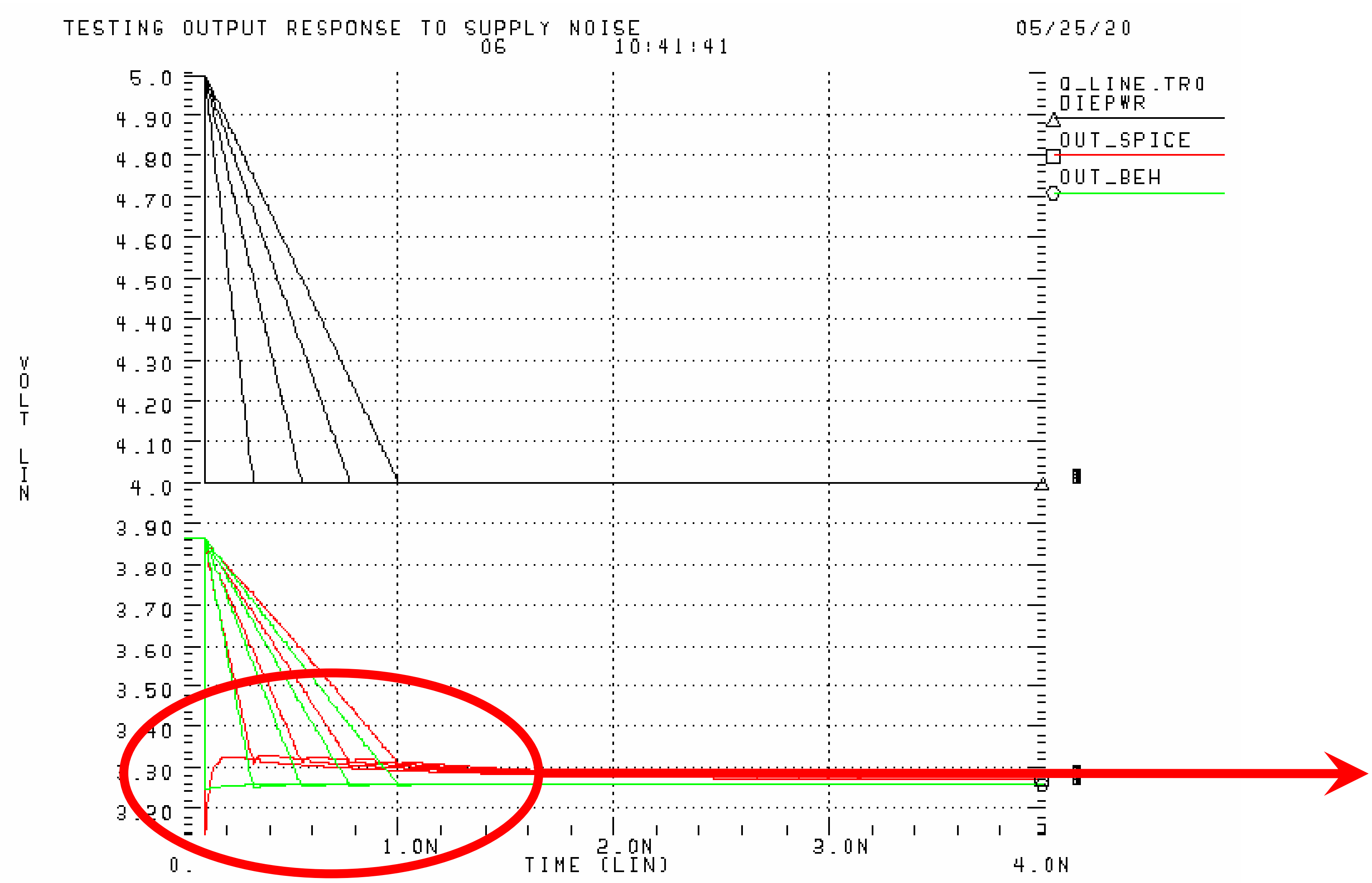
Zooming in to see the details…



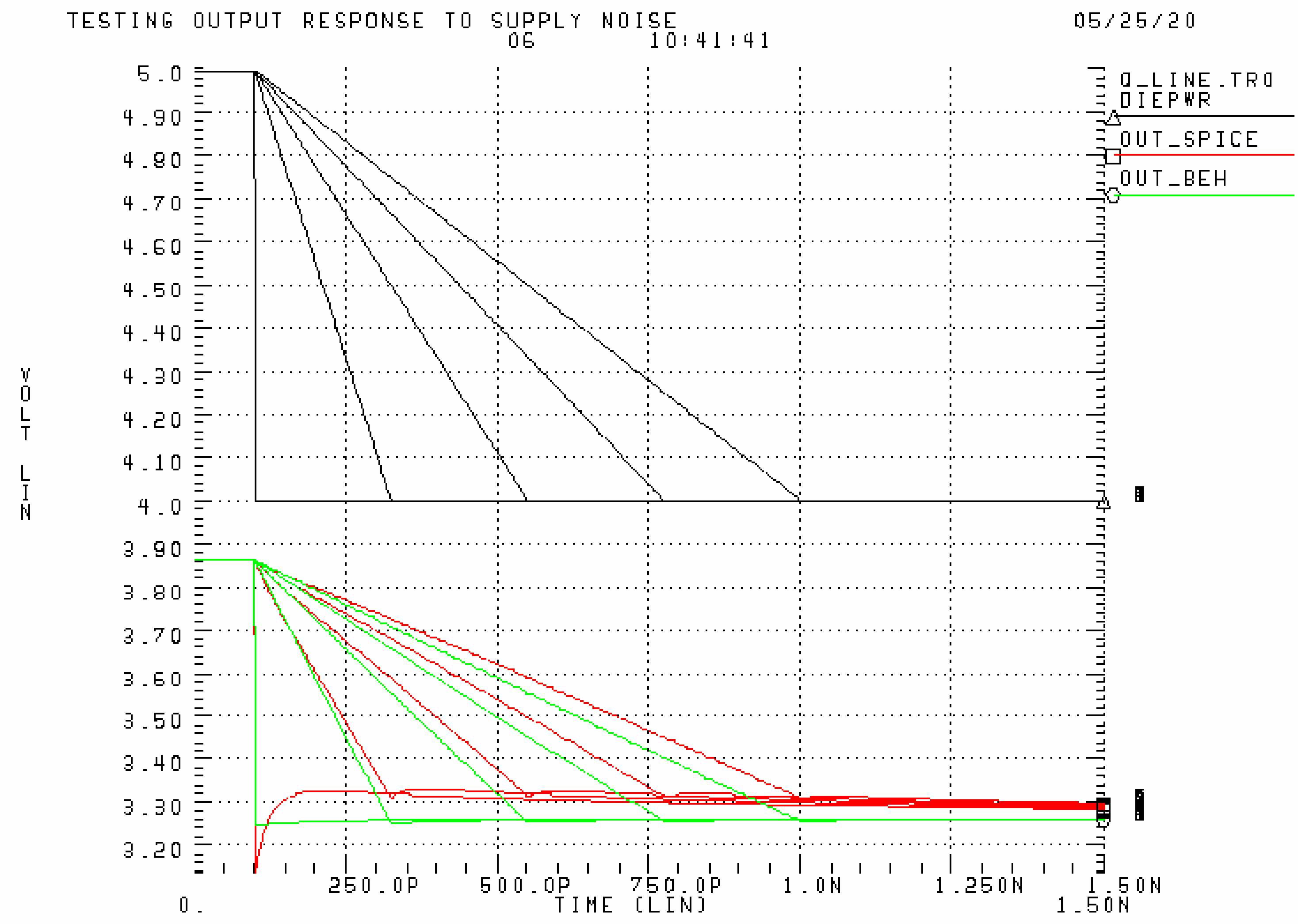
Percent deviation of I_{out}



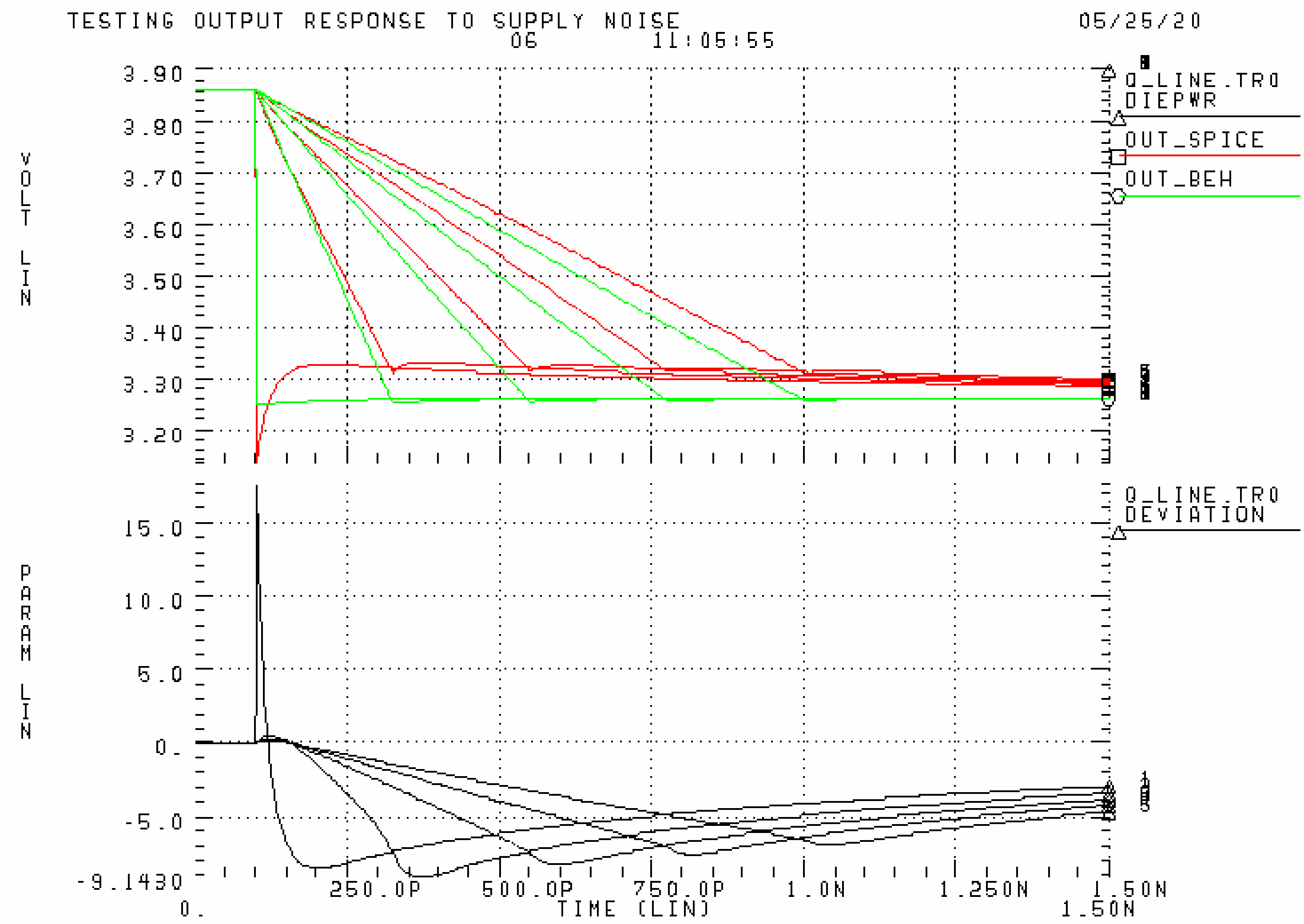
Linear scaling of I_{out} w/r V_{power} (High state)



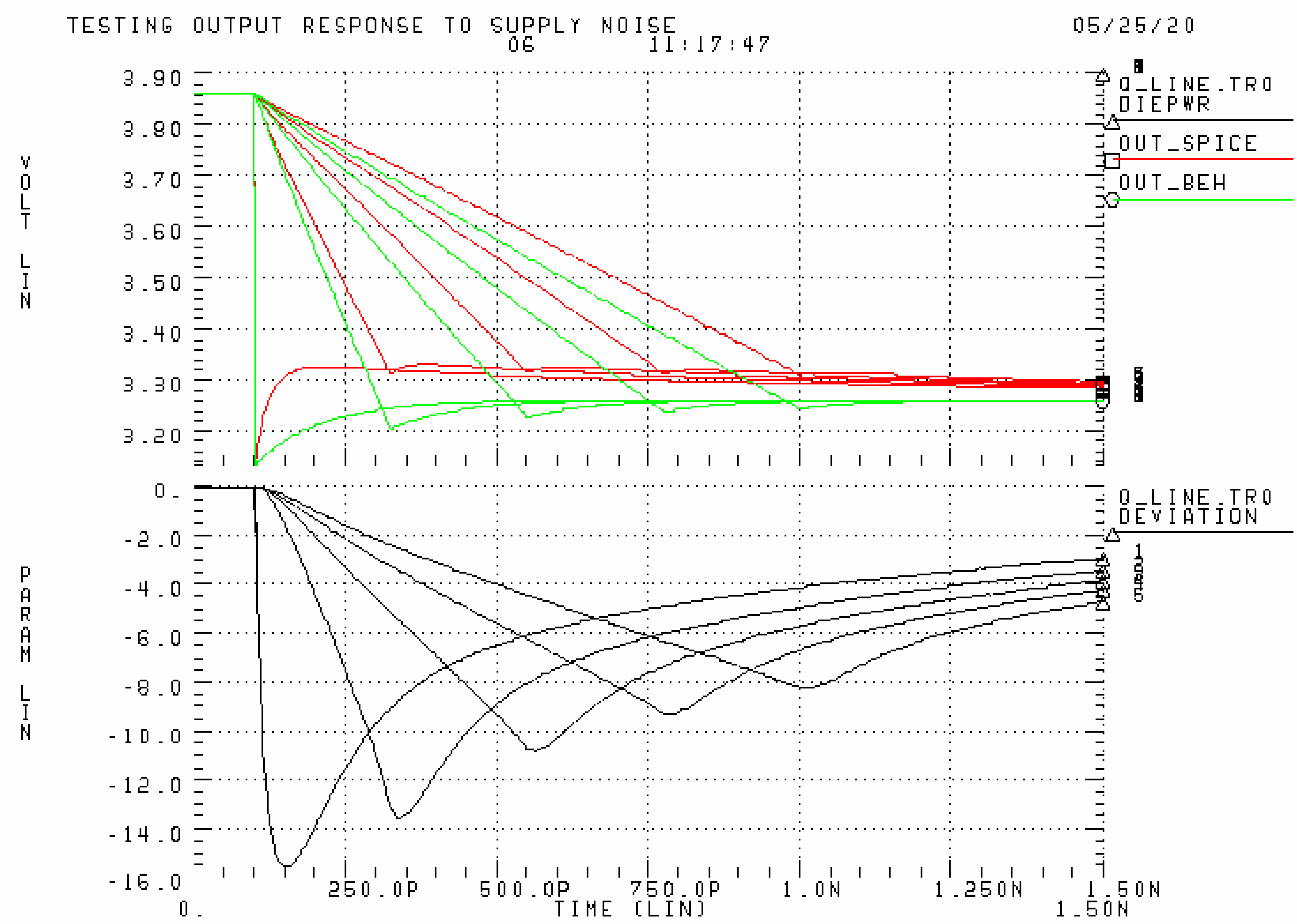
Zooming in to see the details…



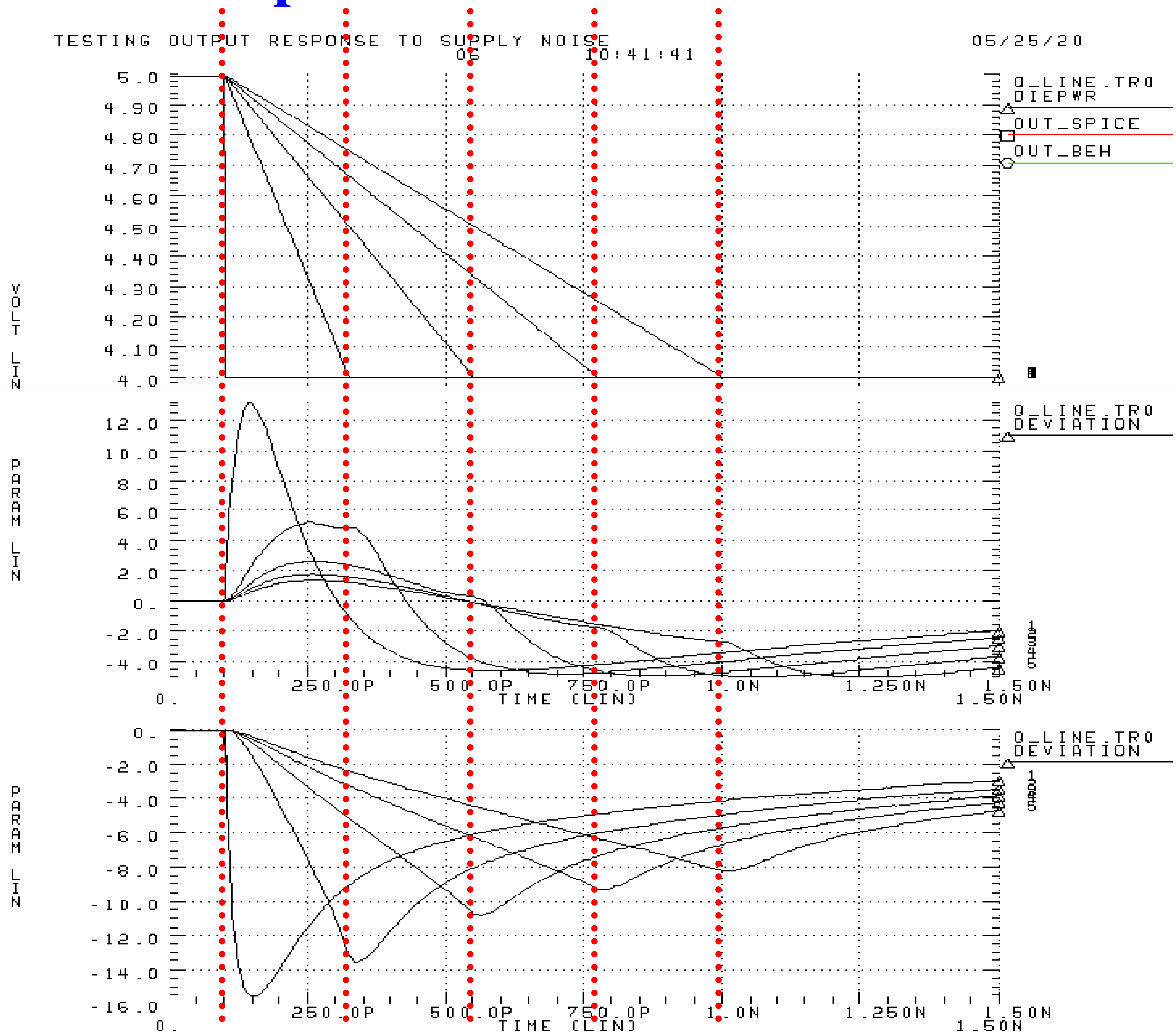
Percent deviation of I_{out}



Percent deviation of I_{out} with different C_comp splitting

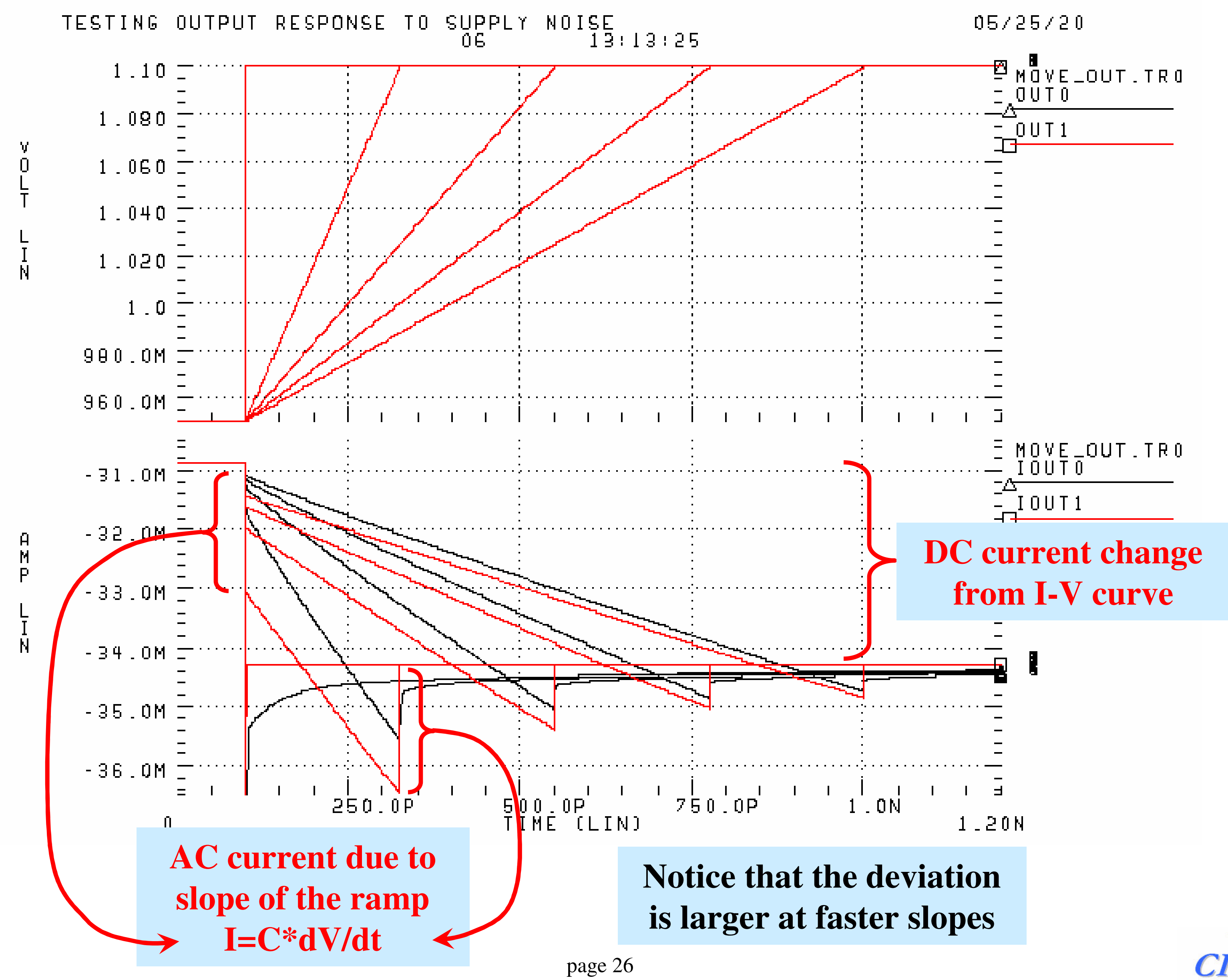


Compare stimulus with deviations

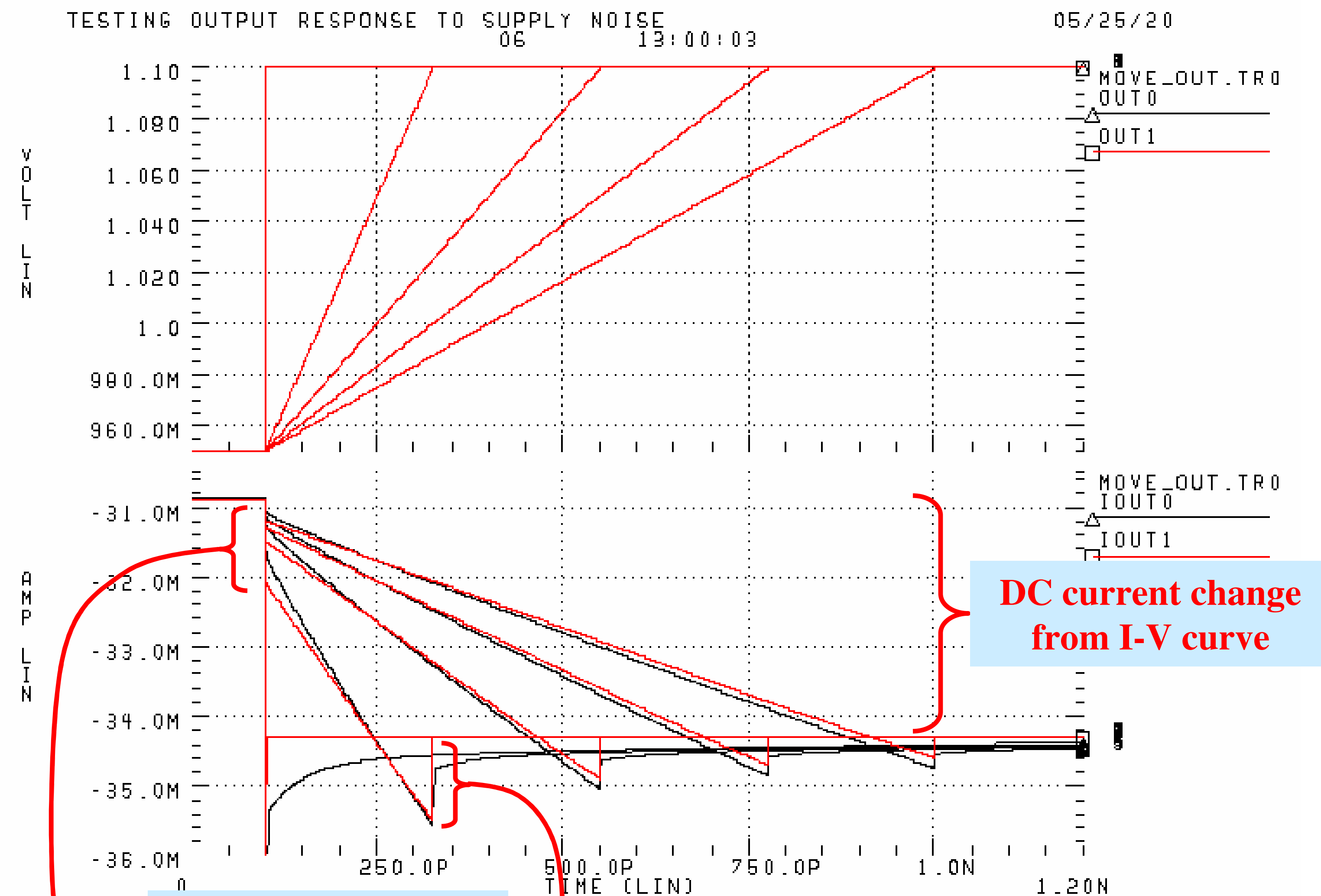


Part III: C_comp revisited

Steady supply, moving pad voltage (Low state, 3.27 pF)



Same with smaller C_comp in IBIS model (1.8 pF)

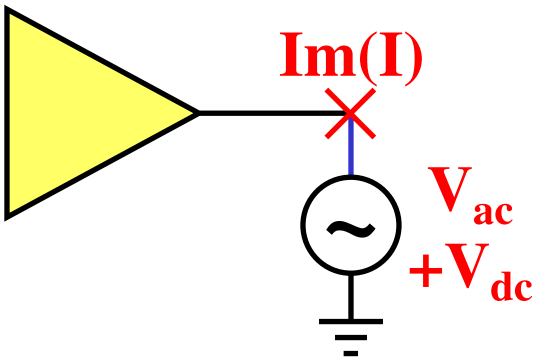


DC current change from I-V curve

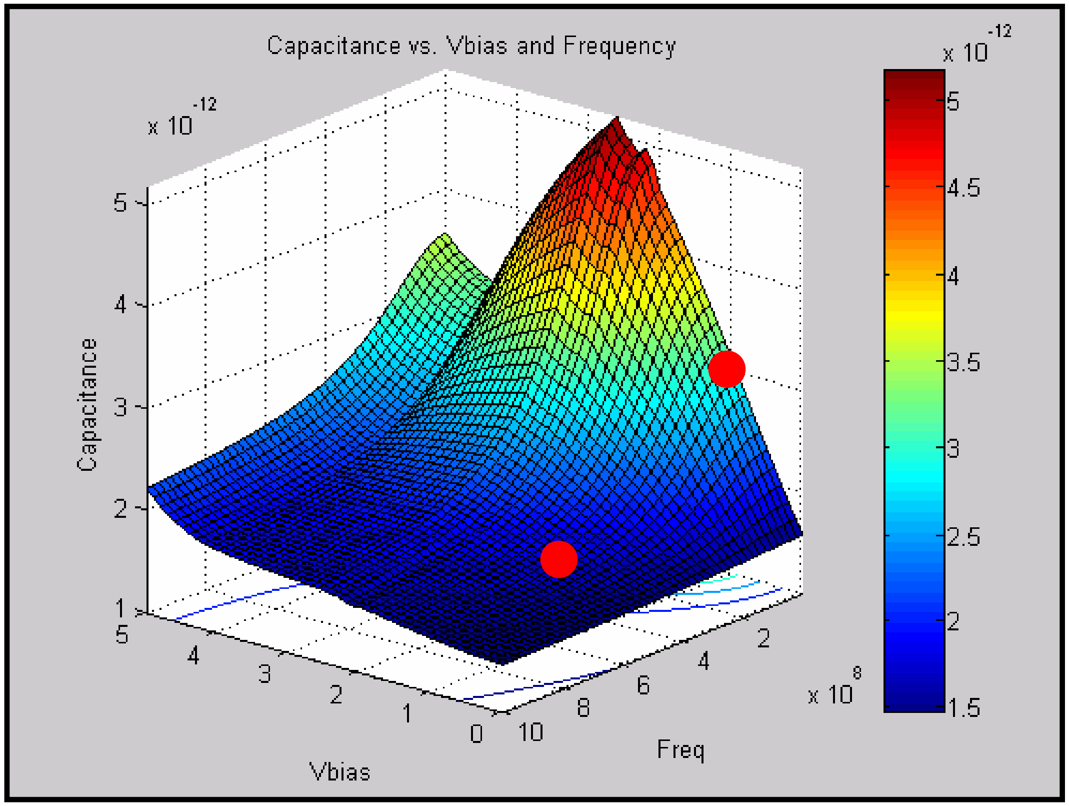
AC current due to slope of the ramp I=C*dV/dt

Smaller C_comp reduces the deviation

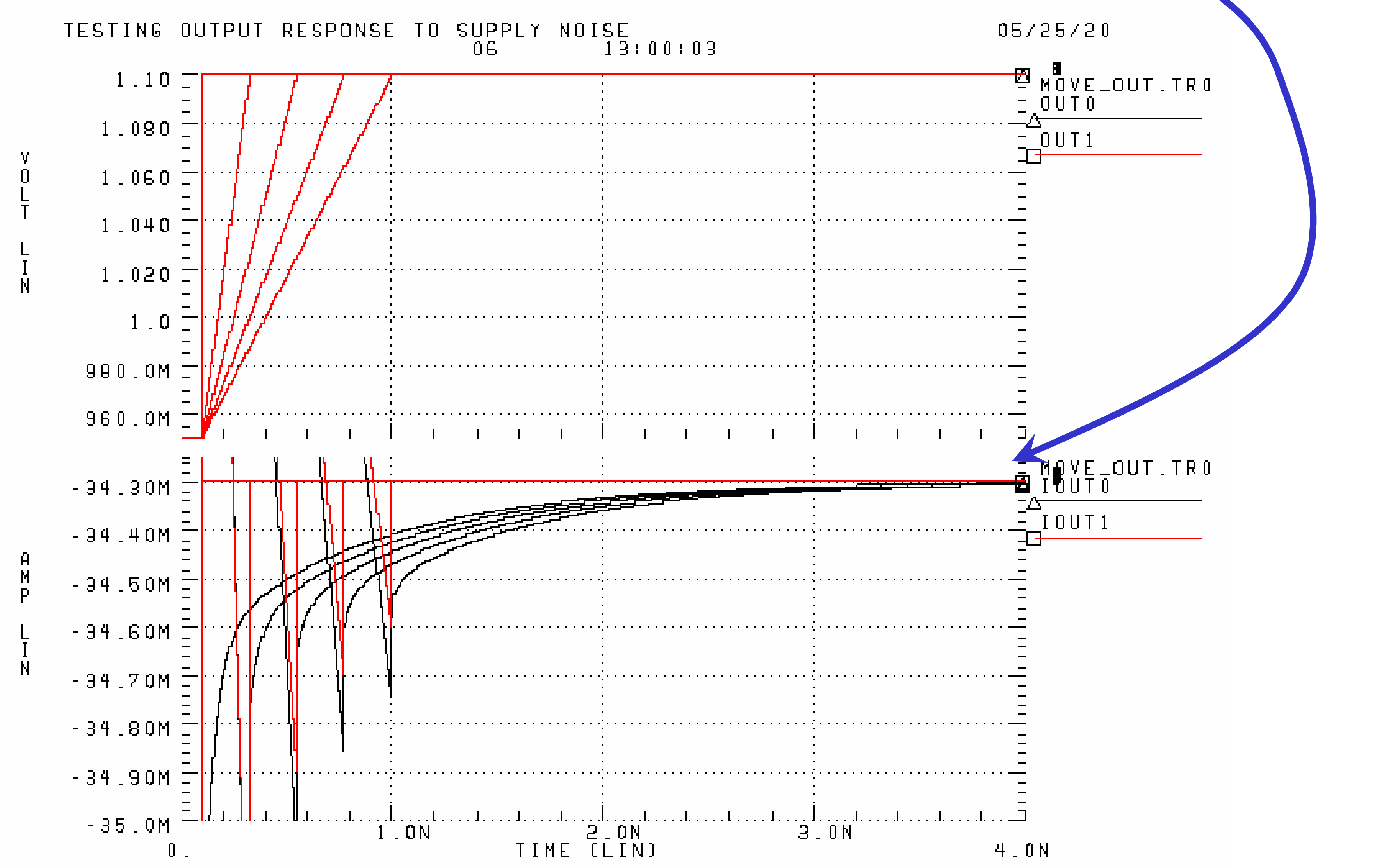
Frequency and voltage dependence in C_comp



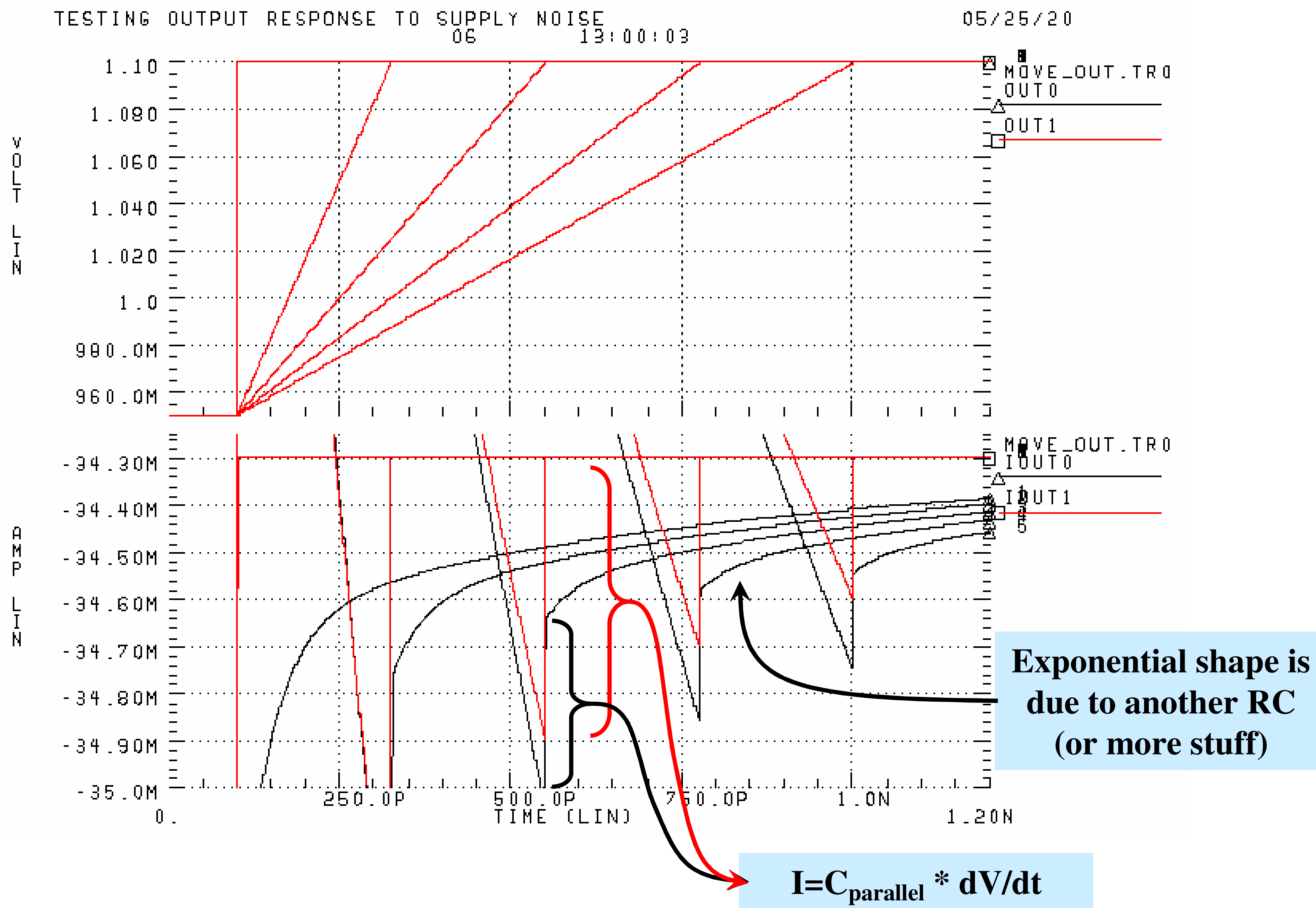
$$C = Im(I)/(2*\pi*f*V_{ac})$$



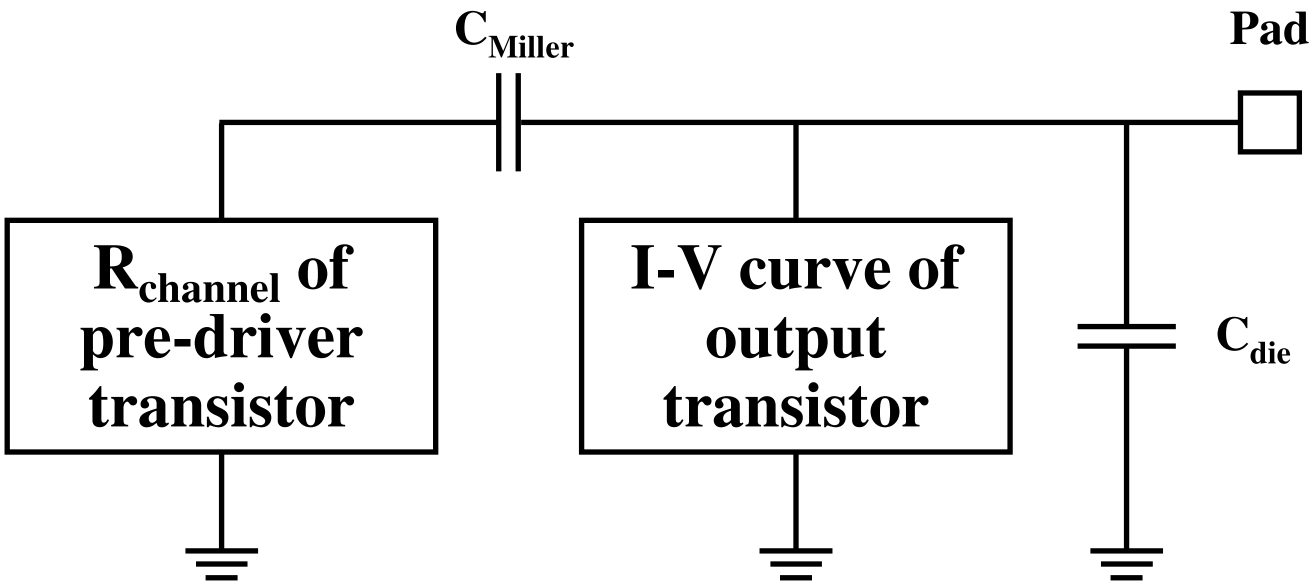
To be sure, steady state solution is correct



Zoom in to see details…



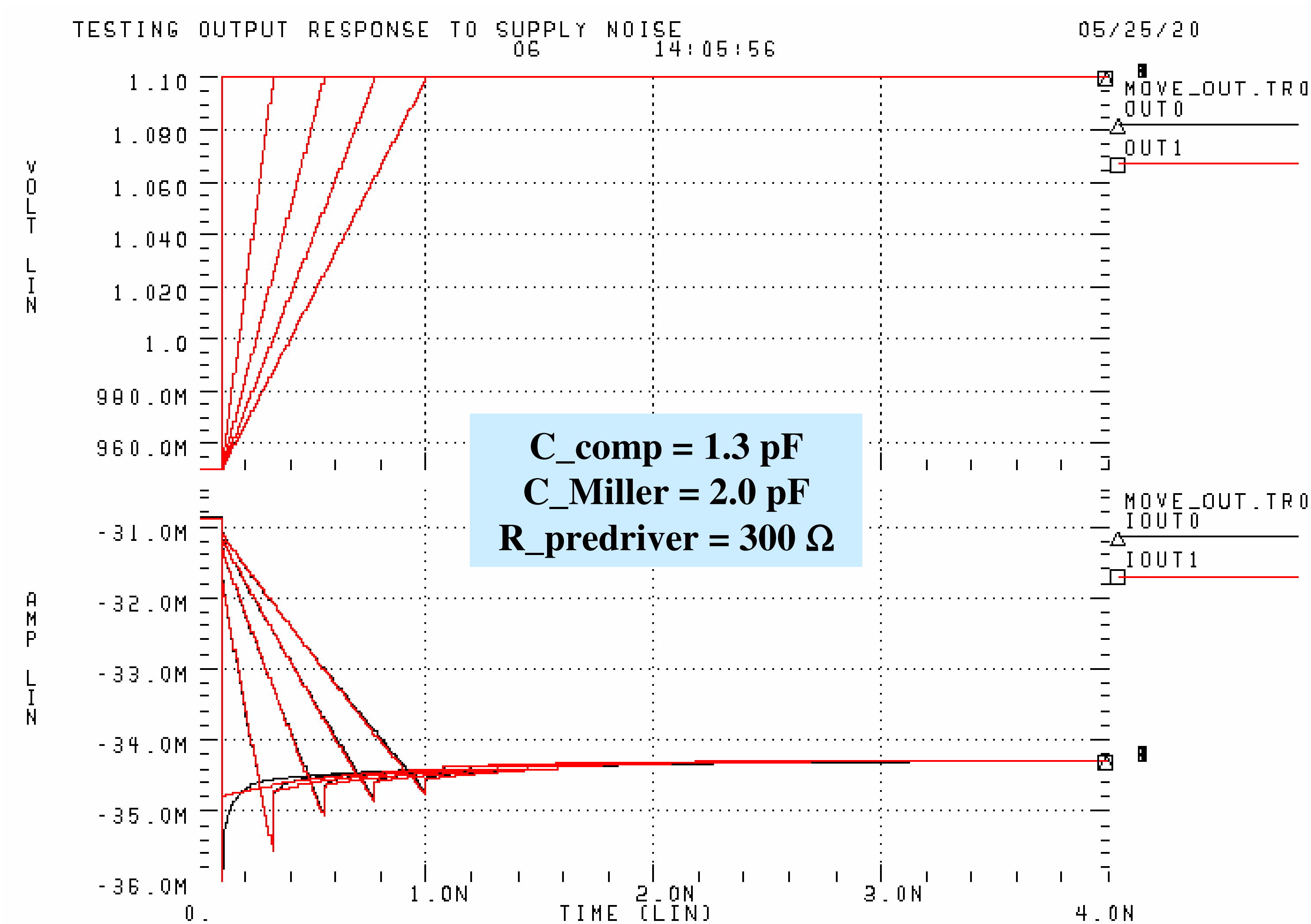
Additional RC explained



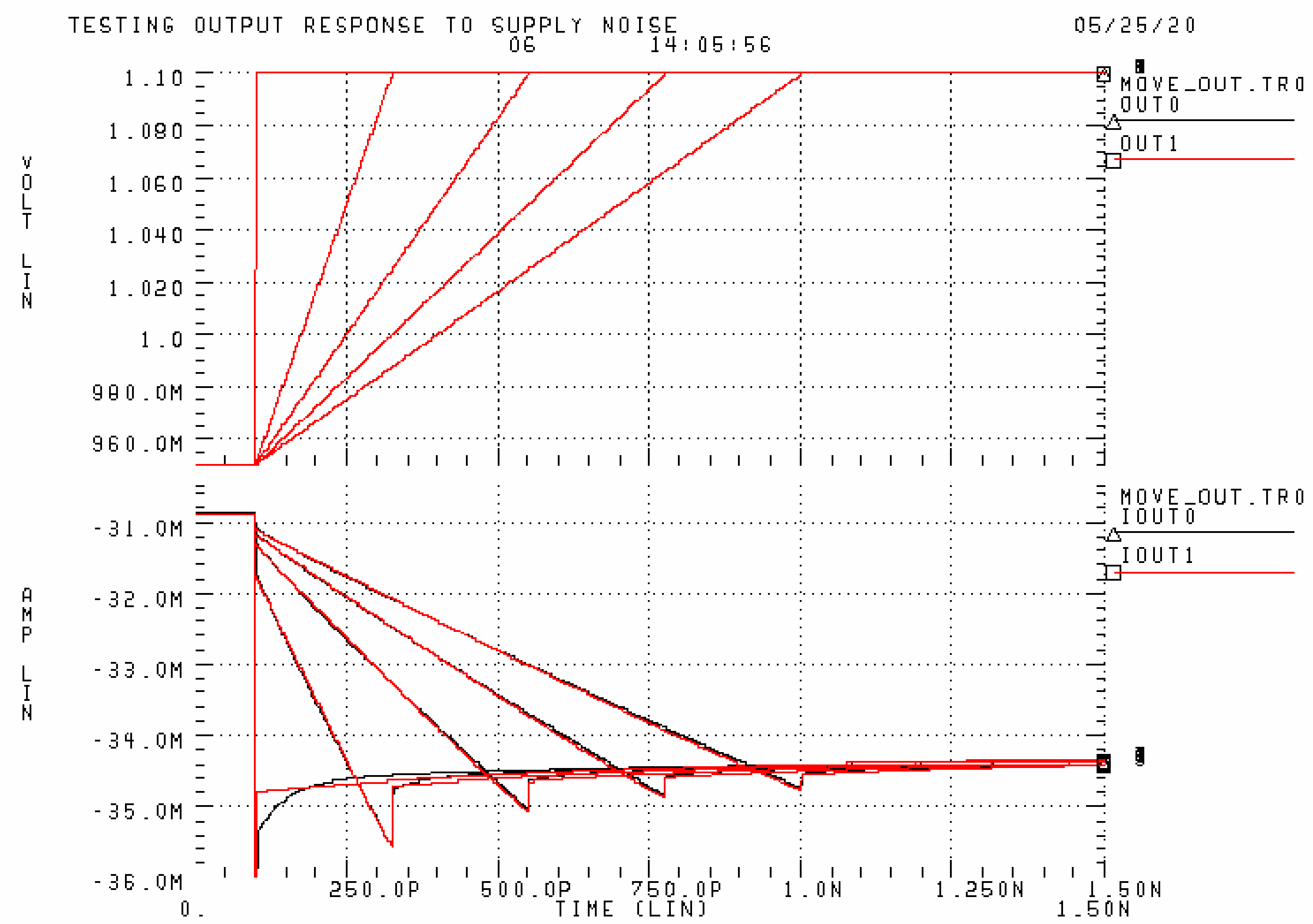
The circuit shown here also agrees with the analysis results of the IBIS BIRD 79 and the accompanying presentations

http://www.vhdl.org/pub/ibis/birds/bird79.txt
http://www.eda.org/pub/ibis/summits/mar02/giacotto.pdf
http://www.eda.org/pub/ibis/summits/jun02/giacotto.pdf

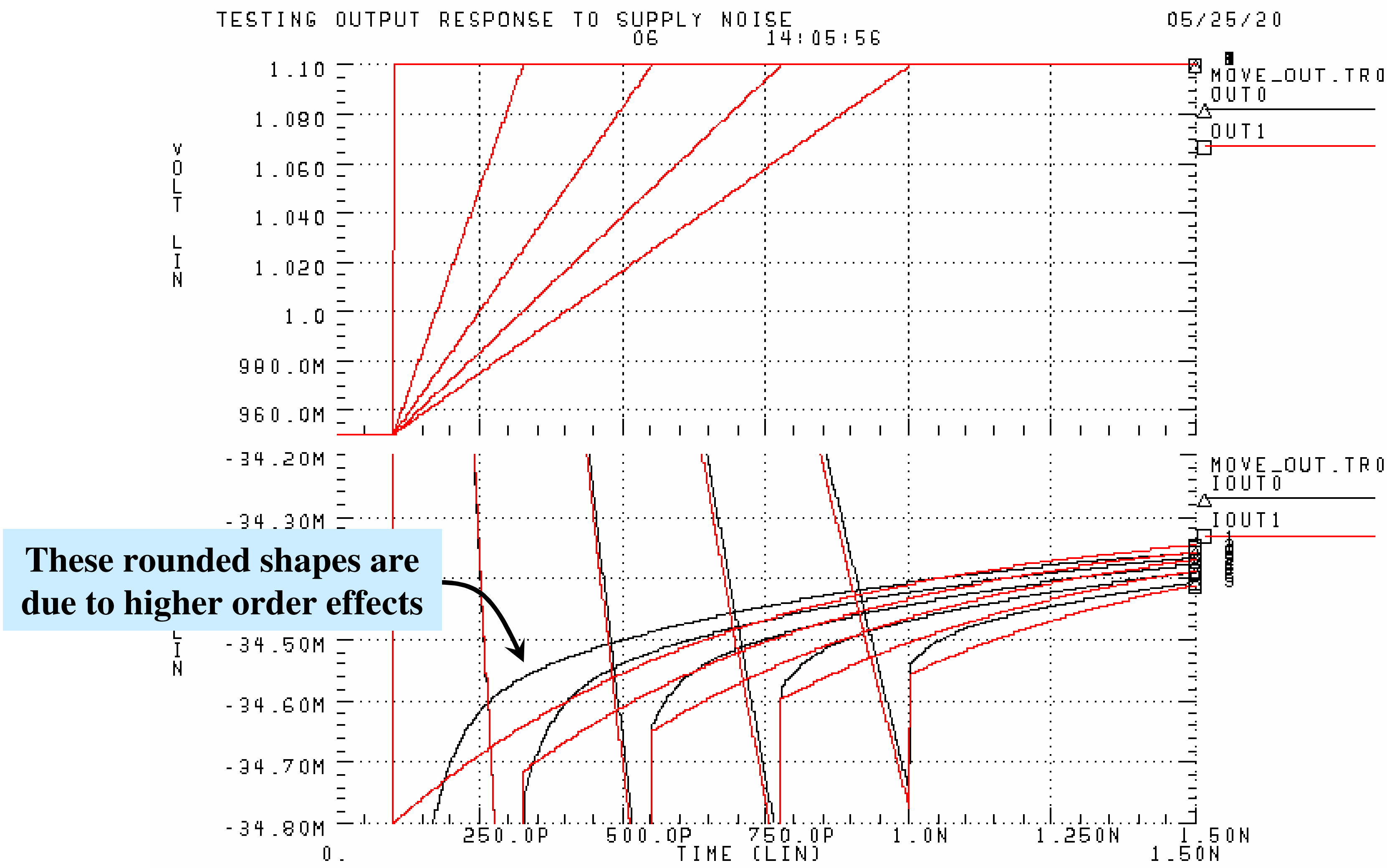
Testing a series RC in parallel with C_comp



Zooming in to see the details…

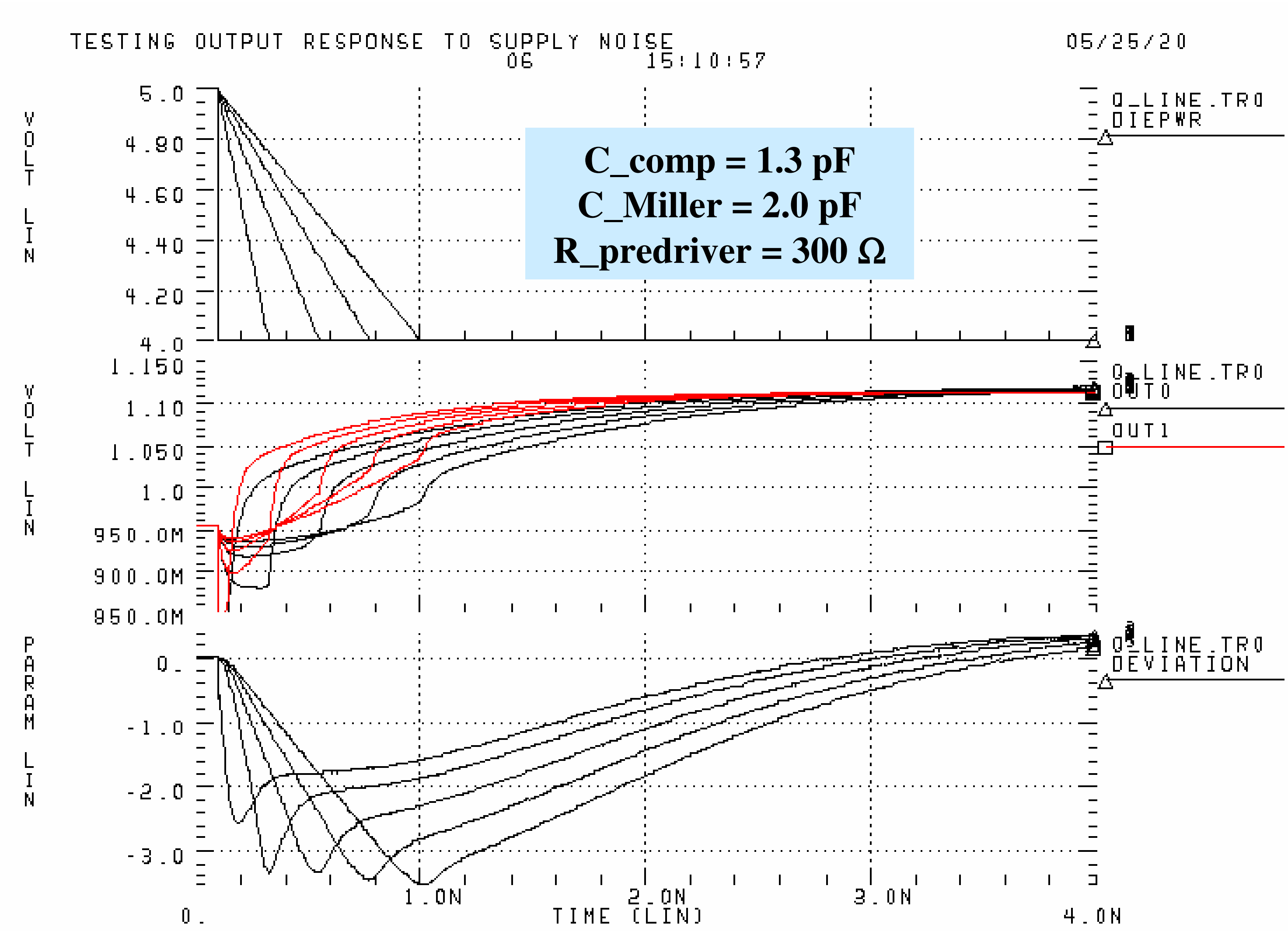


Zooming some more…

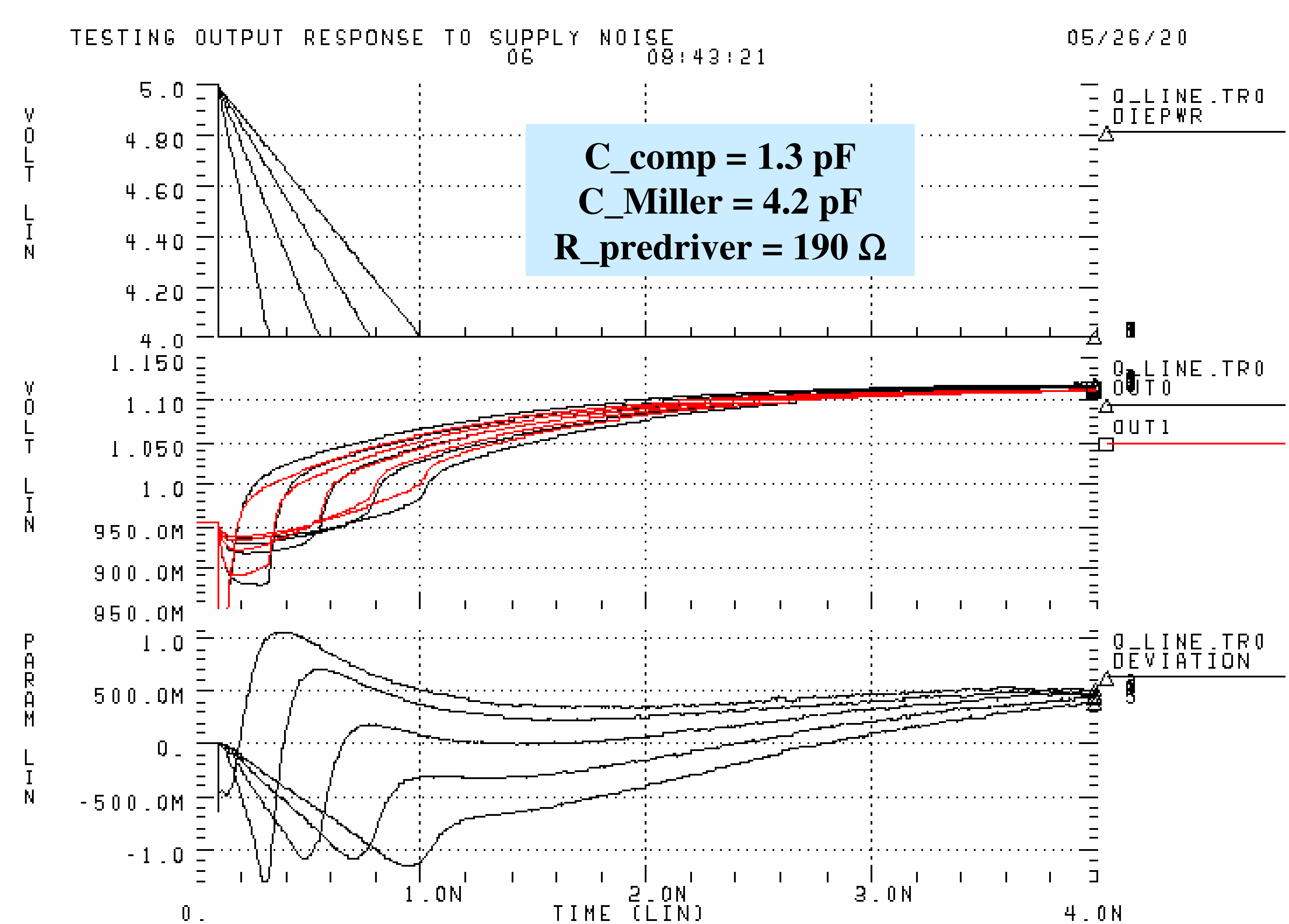


Back to Part II with revised model

Modified IBIS model (Low state)



Same as previous, but tuned RC a little



Conclusions

- **It may be possible to achieve a reasonably good model for the gate modulation effect by**
  - *scaling the I-V curves with static coefficients as described in BIRD98*
  - *adding a series RC in parallel with each (split) C_comp*
  - *fine tuning the C_comp splitting coefficients*
  - *PROBLEM: these are voltage and* ***state*** *dependent!*
- **The previous pages did not attempt to achieve the highest accuracy, additional fine tuning of the parameters would most likely achieve better results**
  - *continue work to show that this will also work in the high state*
  - *do more experiments to determine the best parameter extraction techniques (and/or automation) for model makers*
- **Based on this, the recommendation is to use additional RC circuits in parallel with each (split) C_comp**
  - *need to test more cases to prove this will work in most cases*
  - *this can be either added to BIRD98 or described by a new BIRD*