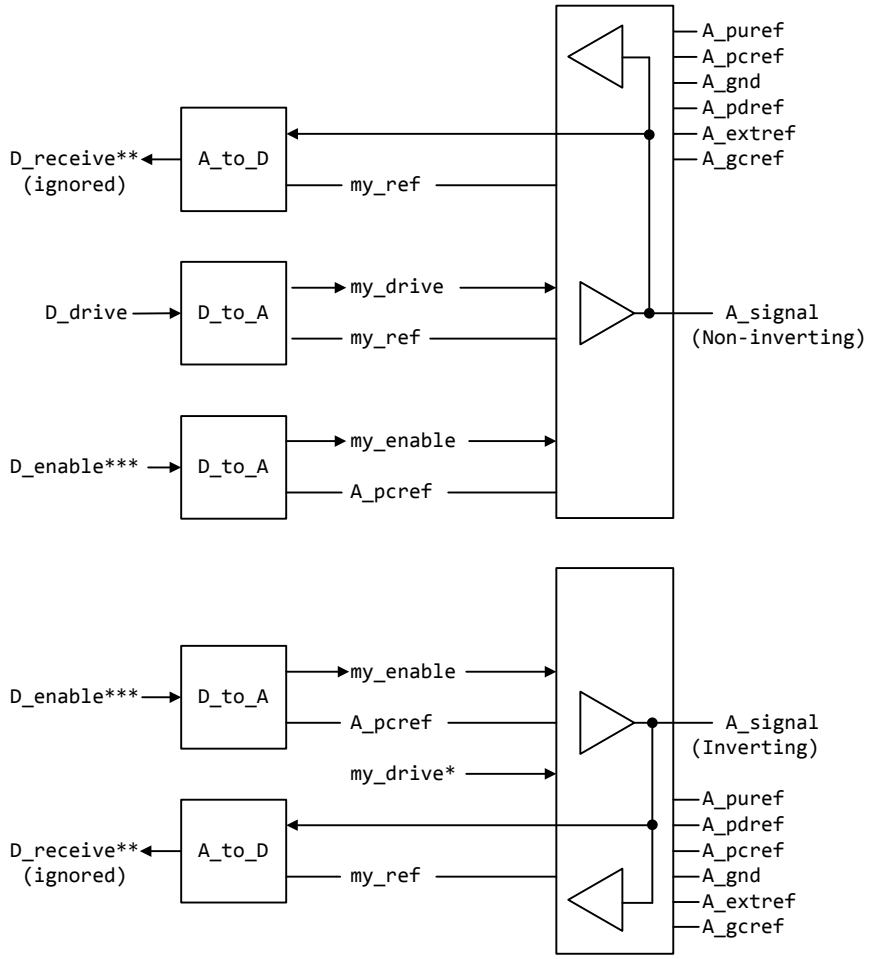


Figure 8: Example SPICE, Verilog-A(MS) or VHDL-A(MS) implementation

* This signal is automatically created, by inverting and delaying D_drive based on the information in [Diff Pin].

** Pseudo-differential buffers must have A_to_D entries, but D_receive is determined by the state of A_signal (Inverting) and A_signal (Non-inverting) according to the [Diff Pin] declaration.

*** D_enable is shared between the separate buffers. This sharing is handled by the EDA tool.