**Text to be blended in IBIS Specification into 2 STATEMENT OF INTENT:**

This document defines behavioral models of I/O buffers, thereafter called IBIS models, as well as the format, requirements and restrictions for both the required and optional data which shall be (or can be) supplied by the model developers to enable EDA tools to simulate such models. It is the intent of this specification that the simulation results of IBIS models generated by different EDA tools are as consistent as they can be. Some discrepancies of those simulation results are possible due to potential differences between inner workings of different EDA tools, for example proprietary interpolation algorithms.

The data for simulation of IBIS models is generally assumed to have been collected using measurements or simulation under static conditions using a test fixture, under dynamic switching conditions or derived from data sheet information. The data itself is to be included in ASCII files, thereafter called IBIS files, following the format defined in this specification.

This specification defines several types of the IBIS models, each with a predefined topology and components whose electrical behavior is defined by the model data. Alternatively the specification allows definition of I/O buffers via some circuit/hardware description languages, spanning predefined IBIS model terminals.

Keywords and subparameters in IBIS files describe device behaviors in terms of data sets, to be used in combination with model equations and assumptions defined within EDA tools. Unless stated otherwise, all device under test (DUT) voltages declared by keywords and subparameters are values with respect to a single reference node (often a DUT reference node such as 0.0 V value or ground used to extract the IBIS file model data).  Some keywords and subparameters may also describe how the data is expected to be used or measured.  Unless stated otherwise, all model data collections assume that the package values are not included.

During simulation (referred to as device in action or DIA), external voltages and loads may be applied to model terminals that are different than those used for DUT extraction.  Some EDA tools may choose to transform the simulation results back to DUT voltage levels for testing against certain specification information. In other words, IBIS buffer data generally describes a “device under test” (DUT), while the actual modeling of the collected data is performed by the EDA tool.

**Text to be included in 5 COMPONENT DESCRIPTION:**

**Text to be included in 6 BUFFER MODELING:**

**Text to be included in 7 PACKAGE MODELING:**