Resolution of IBIS Ground Issues Introduction

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Background Information 1

- The original IBIS specification silently assumed that the reference node of the I/O signal ports was the node GND.
- There is only one place in the description of the node “A_gnd” (intended as the counterpart of GND) in the Multi-Lingual Model Extension section which refers to “universal reference node, similar to SPICE node 0”.
- Otherwise there is no enforcement of using GND as the global node “0”, though starting with Version 5.1 some diagrams now show the global node symbol.

Background Information 2

- Nevertheless, particularly in simulation of a single buffer, or multiple buffers where there is a common reference node, there is nothing wrong to attach that reference node to the global node “0”, either by the user or the EDA tool.
- The only other place where the global node “0” can be present is an IBIS-ISS subcircuit, if intentionally specified by the model vendor.
- Consequences and limitation arising out of any such occurrences need to be clarified.

Background Information 3

- Introduction of the [Pin Mapping] for power and ground bounce simulation and the presence of the [Pulldown Reference] keyword established the presence of the “Pulldown Reference” and “GND Clamp Reference” nodes but have not identified clearly their relationship with respect to the signal I/O reference node, or GND.
- It needs to be clearly stated what the signal I/O reference node is.
- It is not only the “second” node in the I/O port, but also the common mode port for the differential and pseudo-differential buffers.
- Furthermore, for the pseudo-differential buffers, it is the connection node of the inverting and non-inverting buffers.

Purpose of This Work

– The purpose of this discussion is to decide how the specification needs to address the following questions.

– Some answers are commonly understood, yet the specification may need to unambiguously clarify it.

Topics 1

- Is the global node “0” assumed in any discussion or any diagram?
- Under what circumstances the global node “0” can be used by the user or the EDA tool?
- What can be done if any IBIS-ISS subcircuit contains a global node “0”?
- What nodes is the C_comp capacitance connected to?
- What is the impact of different [Pulldown Reference] and [GND Clamp Reference] values?

Topics 2

- What is the relationship between non-zero [Pulldown Reference], [GND Clamp Reference] and the signal I/O reference node in the absence of the [Pin Mapping] keyword?
- What is the relationship between non-zero [Pulldown Reference], [GND Clamp Reference] and the signal I/O reference node when the [Pin Mapping] keyword is present?
- What is the relationship between pulldown_ref, and/or the gnd_clamp_ref bus declaration under the [Pin Mapping] keyword and the signal I/O reference node?
- Do we need to extend the [Pin Mapping] definition to cover signal I/O reference bus declaration?