The Cref and Rref subparameters correspond to the test load that the semiconductor vendor uses when specifying the propagation delay and/or output switching time of the model. The Vmeas subparameter is the timing reference voltage level that the semiconductor vendor uses for the model. Include Cref, Rref, Vref, and Vmeas information to facilitate board-level timing simulation. The assumed connections for Cref, Rref, and Vref are shown in Figure 1.



1. - Reference Load Connections

A single-ended or true differential buffer can have Rref\_diff and Cref\_diff (Figure 2).



1. - Single-Ended or True Differential Buffer



1. - Low State (Logic Zero) Isso\_pd Data Collection

The effective current table for the Isso\_pu current is extracted by the following process. The buffer is set to “logic one”. A Vtable voltage source is inserted between the [Pullup Reference] node and the buffer as shown below. This Vtable voltage is swept from -Vcc (typical) to +Vcc (typical) and is relative to the [Pullup Reference] typ/min/max values for the corresponding columns. The output is connected to the GND (typical) value as shown in Figure 8.



1. - High State (Logic One) Isso\_pu Data Collection

For each of these extractions, the corresponding [GND Clamp] and [POWER Clamp] currents need to be removed. Normally these are negligible. However, if on-die terminators exist, the extra currents that are associated with them should be removed from the [ISSO PD] and [ISSO PU] tables. The process details are not discussed here, but need to be solved by the modeler. Such details may depend upon the contents of the [GND Clamp] and [POWER Clamp] tables and the [GND Clamp Reference] and [POWER Clamp Reference] selections.

Currents are considered positive when their direction is into the component.

*Other Notes:* EDA tools can use such tables to calculate modulation coefficients to modulate the original pulldown and pullup currents when a voltage variation on the pullup and pulldown reference nodes is revealed during power and/or ground bounce, and/or SSO simulation events.

To describe the modulation coefficients, a reference algorithm to generate an output response producing Vout(t) for a given load including clamp currents that requires an Iout(t) is shown in terms of pullup table currents Ipu(Vcc-Vout(t)) and pulldown table currents Ipd(Vout(t)). See Figure 9.



1. - Reference Data Collection

When the supplies are modulated during simulation, the modulation coefficients Ksso\_pu(Vtable\_pu) and Ksso\_pd(Vtable\_pd) modify the equations as shown in Figure 10.



1. - Reference Data Collection with Supply Modulation



1. - [Rgnd], [Rpower], [Rac], [Cac] in Relation to Package and Buffer Data

*Other Notes:* There is no monotonicity requirement. However the model supplier should realize that it may not be possible to derive a behavioral model from non-monotonic data.



1. - [Series MOSFET] Voltage Polarities and Current Direction



1. - [Rising Waveform] and [Falling Waveform] Fixtures



1. - [External Reference] - (used only for non-driver modes)

For \*\_ECL model types, the [Pullup] and [Pulldown] sections of the DUT share the same power reference terminal. The [Composite Current] includes the currents through both sections.

*Other Notes:* Figure 17 documents some expected internal paths for a useful special case where only one common power pin (VDDQ) and one common ground exists (GND).



1. - [Composite Current] Internal Current Paths

Table 12 – Port Names in Multi-Lingual Modeling

| **Port** | **Name** | **Description** |
| --- | --- | --- |
| 1 | D\_drive | Digital input to a model unit |
| 2 | D\_enable | Digital enable for a model unit |
| 3 | D\_receive | Digital receive port of a model unit, based on data on A\_signal (and/or A\_signal\_pos and A\_signal\_neg) |
| 4 | A\_puref | Voltage reference port for pullup structure |
| 5 | A\_pcref | Voltage reference port for power clamp structure |
| 6 | A\_pdref | Voltage reference port for pulldown structure |
| 7 | A\_gcref | Voltage reference port for ground clamp structure |
| 8 | A\_signal | I/O signal port for a model unit |
| 9 | A\_extref | External reference voltage port |
| 10 | D\_switch | Digital input for control of a series switch model |
| 11 | A\_gnd | Global reference voltage port |
| 12 | A\_pos | Non-inverting port for series or series switch models |
| 13 | A\_neg | Inverting port for series or series switch models |
| 14 | A\_signal\_pos | Non-inverting port of a differential model |
| 15 | A\_signal\_neg | Inverting port of a differential model |



1. - Port Names for I/O Buffer



1. - Example Showing [External Circuit] Ports



1. - Reference Example for [Node Declarations] Keyword



1. - [Test Load] Elements and Placement



1. - Example of TTgnd Extraction Setup



1. - Example of Series MOSFET Table Extraction