IBIS Gate Modulation Effect (STMicroelectronics Proposal)

Introduction

The following proposal is aimed at solving the so called “Gate Modulation Effect”, which represents a critical limit of the actual IBIS model to describe properly the change of buffer’s drive strength when a bouncing occurs on the power/ground nodes due to a Simultaneous Switching Output (SSO) noise.

The ST solution has been implemented and validated by the VHDL-AMS IBIS implementation on several test-cases.

The results obtained have shown a very good matching with the equivalent SPICE results.

Hereafter for discriminating between the IBIS VHDL-AMS implementation, including also the ST algorithm to solve the “Gate Modulation Effect”, and the current standard format, the first one will be called IBIS-AMS, whereas the second one will be called IBIS-STD.

Today the IBIS simulations are gaining an increasing importance, as an alternative to SPICE, into the system design verification phase because the SPICE simulations are too time expensive and, sometimes, the SPICE models are not available (for instance when some components are provided from third parties).

Considering also the current trend of IC design towards system/PCB design (the system-in-package technology is a real example), IBIS is becoming the unique way for performing signal integrity analysis before the prototype phase. In addition, the low-power-supply trend, especially in wireless and mobile applications, is pushing to investigate properly the power integrity issues such as the bouncing that the IBIS-STD is unable to analyze accurately.
In conclusion, today it is mandatory to make available to the design community a reliable solution to the “Gate Modulation Effect”, even though it is not perfect, because the actual IBIS-STD bouncing simulations are completely inaccurate and SPICE is not always a possible alternative.

ST Gate Modulation proposal

In the IBIS-STD model the pullup and pulldown currents are related to a fixed value of the gate-to-source voltage (Vgs), equal to power supply voltage value (Vgs= VDD), whereas the Vds voltage can change over the range [-VDD, 2VDD].

Therefore, the MOS-like characteristics of both pullup and pulldown stages are described by the following equation:

$$I\_IBIS\text{-}STD = I(Vgs=VDD, Vds)$$

Unfortunately, it implies that during an IBIS-STD SSO simulation the Vgs modulation, due to the bouncing on the source node, is not well modeled because the operating point tends to evolve along the characteristic Vgs = VDD. This produces a remarkable mismatch between SPICE and IBIS-STD simulation results.

A solution has been identified by introducing two coefficients, which modulate properly the IBIS-STD current during a SSO simulation, and it has been validated by the VHDL-AMS implementation of IBIS model, introduced by the IBIS Open Forum.

The two coefficients are so defined:

- **K_ssn_pulldown** is the ratio between the effective current of the pulldown stage, flowing from drain to source, I(Vgs, Vds), and the IBIS-STD model current I(Vgs=VDD,Vds),

$$\mathbf{K\_ssn\_pulldown = I(Vgs, Vds)/I(Vgs=VDD, Vds)} \quad \mathbf{(1)}$$

- **K_ssn_pullup** is the ratio between the effective current of the pullup stage, flowing from source to drain, I(Vsg, Vsd), and the IBIS-STD model current I(Vsg=VDD,Vsd),

$$\mathbf{K\_ssn\_pullup=I(Vsg, Vsd)/I(Vsg=VDD, Vsd)} \quad \mathbf{(2)}$$

The algorithm implemented in the IBIS-AMS model recognizes the Vgs changes by monitoring the source node voltage (Vs) changes (the gate node voltage (Vg) is presupposed stable) and then modulates/corrects properly the IBIS-STD current by the K_ssn coefficient:

$$\mathbf{I(Vgs, Vds) = Kssn(Vgs,Vds)*I(Vgs=VDD,Vds)} \quad \mathbf{(3)}$$

$$\Downarrow$$

$$\mathbf{I\_effective = Kssn(Vgs,Vds)*I\_IBIS\text{-}STD} \quad \mathbf{(4)}$$

$$\Downarrow$$

$$\mathbf{Kssn(Vgs,Vds) = I\_effective/I\_IBIS\text{-}STD} \quad \mathbf{(5)}$$

A table approach has been used to implement the above relationship in the IBIS-AMS model, thus preserving the compliance with IBIS-STD format.

The effective pullup and pulldown currents, and so the K_ssn coefficients, depend on Vgs and Vds; therefore, to describe the different I(Vgs, Vds) MOS-like characteristics of both stages, a lot of tables could be requested.

Nevertheless, a good number of trials have showed that a good accuracy can be obtained by drawing the I(Vgs, Vds) currents for different values of Vgs and only one fixed value of Vds, chosen in the saturation zone. A good choice may be Vds =VDD.

For this reason, actually, only one table of the real current I(Vgs, Vds) for Vds=VDD is extracted for the pullup and pulldown stage, respectively. Therefore, a two-table approach is the best trade-off between simulation accuracy and computational time. Such tables are managed by the VHDL-AMS IBIS model to extrapolate the K_ssn coefficients by using the equation (5).

In more details, the tables I-Vgs are extracted by a dc sweep [-VDD, VDD] on the source node Vs, around the ground voltage (0V) for the pulldown stage and around the power supply voltage (VDD) for the pullup stage. Therefore, the pulldown table provides the current flowing through the ground node over a source voltage range [-VDD, VDD], whereas the pullup table provides the current flowing through the power node over a source voltage range [0, 2VDD]. As said before, considering the gate voltage (Vg) stable, the extracted tables are I-Vs.

During a bouncing simulation, the IBIS-AMS model reveals that the source voltage changes and, by using these additional tables, adjusts the IBIS-STD current by the K_ssn coefficients.

In the figure 1 it is possible to notice the mismatch between the classic IBIS-STD model and the SPICE model of the buffer in a SSO case, whereas in the figure 2 a remarkable improvement can be observed by using the identified solution.

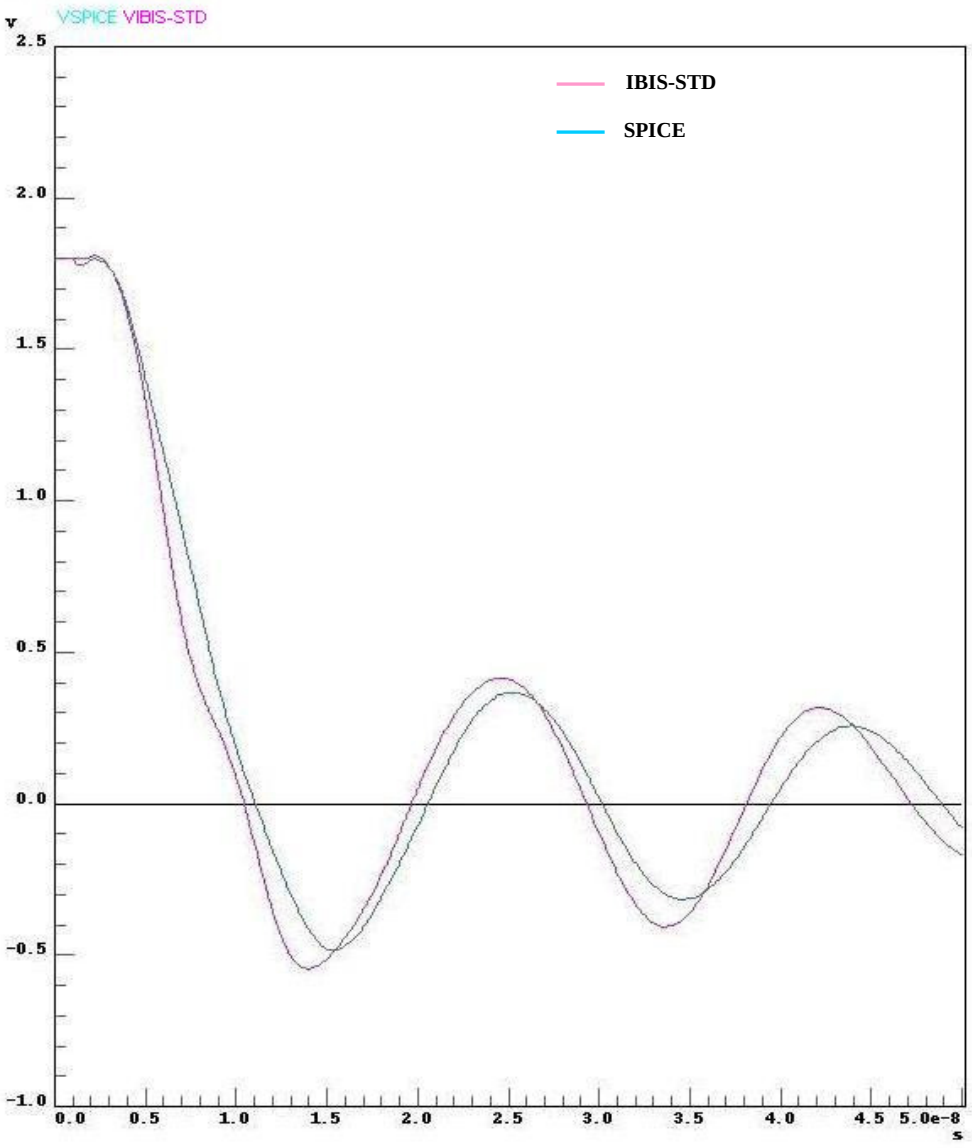

Fig.1 – SSO simulation - Comparison results IBIS- STD vs SPICE

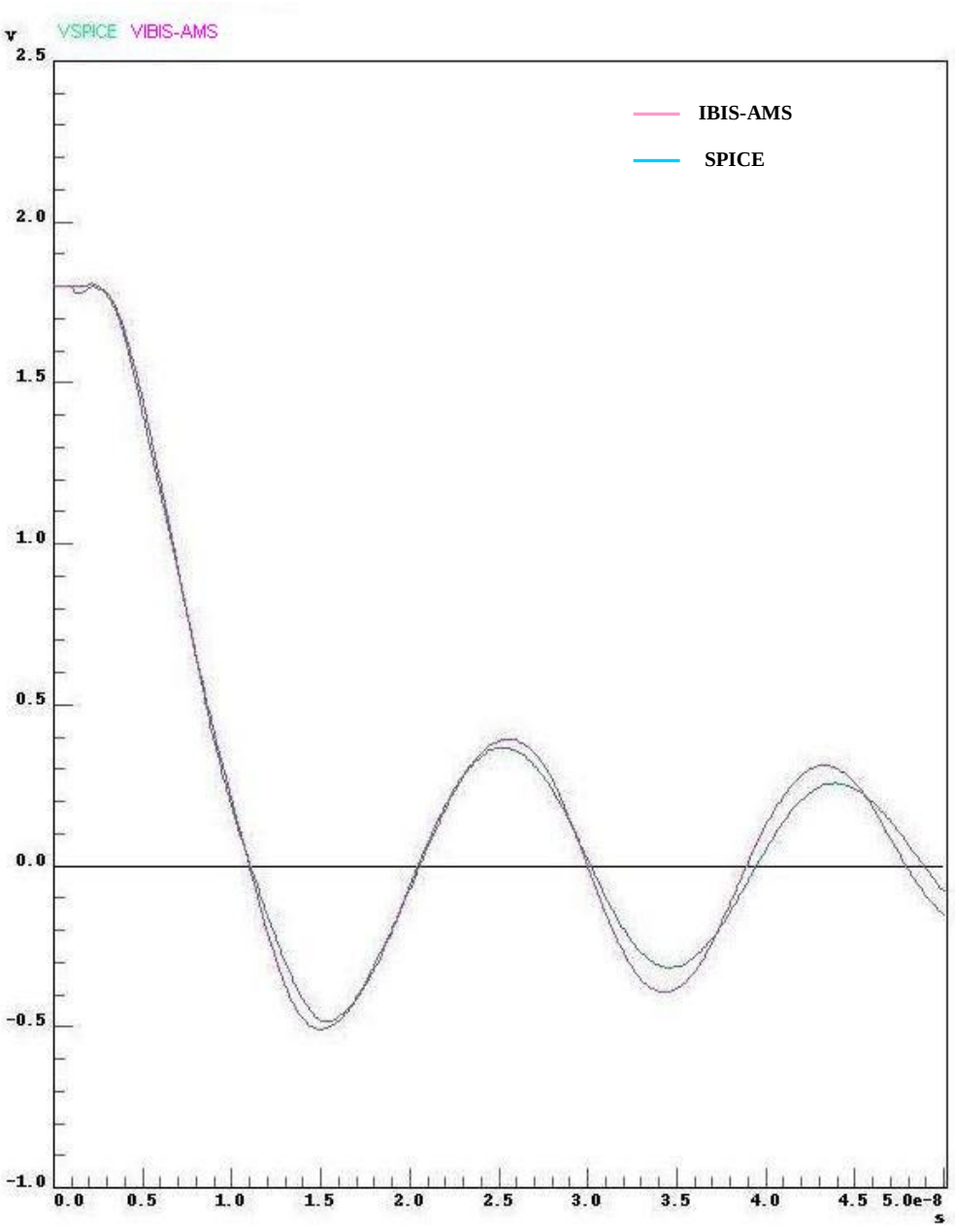

Fig.2 – SSO simulation - Comparison results IBIS-AMS vs SPICE

Potential implementation into a transistor-level EDA tool

In order to show how easy may be the implementation of the above solution in any commercial transistor-level tool, hereafter it is reported a potential implementation into the Mentor Graphics tool (Eldo), which has been the reference SPICE tool for validating the ST "Gate Modulation" solution.

The ST solution is very well compatible with the IBIS-STD equivalent model used in Eldo's simulation, reported in the figure 3.

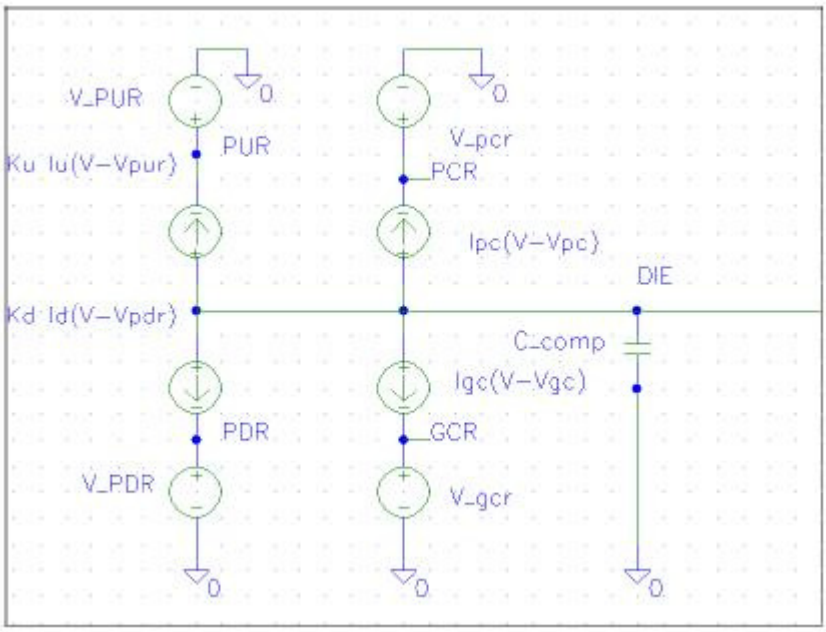

Fig.3 – IBIS-STD driver representation in Eldo

If the ST proposal was implemented in Eldo, the pullup and pulldown equations would become:

K_ssn_pullup*Ku*Iu(V-Vpur)

K_ssn_pulldown*Kd*Id(V-Vpdr)

The two tables I-Vs of the real pullup and pulldown currents might be linked by introducing two additional keywords to the IBIS-STD statement in Eldo. For instance, these new keywords might be called ISSO_PU and ISSO_PD. Moreover, they may be managed by translating the VHDL-AMS algorithm of the ST proposal in the Eldo's proprietary code.

A possible Eldo's IBIS-STD statement may be the following:

_IO_xx NN {NN} file="path" component="componet_name" model="model_name"

+ pin="pin_name" power=on|off ……VI_Corner=typ|min|max…….
……..

+ ISSO_PD=typ|min|max ISSO_PU=typ|min|max…….

Whereas the two tables I(Vs) might be provided in the following format

```
|
[ISSO_PD]
| voltage          I(typ)            I(min)            I(max)
|
-1.8000V         372.1000mA        302.8200mA        459.2100mA
-1.7640V         357.0800mA        292.1800mA        440.5700mA
……
……
1.6560V          749.4600pA         14.0370pA         45.4350nA
1.6920V          187.3100pA        -76.0480pA         11.9810nA
1.7280V          -10.7480pA       -116.7800pA         3.0124nA
1.8000V         -108.0300pA       -163.1300pA        85.4930pA
|

|
[ISSO_PU]
|
| voltage          I(typ)            I(min)            I(max)
|
0.0000V          -37.7430pA        -85.2600pA        -19.4290pA
36.0000mV        -75.5960pA       -181.7600pA        -24.4690pA
……
……
3.4560V         -15.6350mA        -12.8160mA        -19.3770mA
3.4920V         -15.8610mA        -12.9840mA        -19.6380mA
3.5280V         -16.0840mA        -13.1350mA        -19.8970mA
3.6000V         -16.5140mA        -13.3920mA        -20.4060mA
|
```

The first column contains the sweep voltage around the Vs node voltage (zero for the pulldown and VDD for the pullup), whereas the three remaining columns contain the typical, minimum, and maximum current values.
In the above example the typical power supply voltage value is VDD=1.8V, therefore the voltage values of the ISSO_PU table is centered on 1.8V.