Report on IBIS Committee to IEEE EMC Society

This report was delivered by Roy.Leventhal@ieee.org at the Technical Committee 10 (TC10) meeting during the IEEE EMC2007 Symposium on 7/11/07. Roy was an interested observer with no official IBIS function. EIA IBIS Open Forum website: http://www.eigroup.org/ibis/default.htm

Introduction

The goal of this report was to inform TC10, the Signal Integrity Technical Committee, about the on-going activities of the EIA IBIS Open Forum and to later communicate their activities back to the IBIS Committee for possible future collaboration.

Executive Summary

The EIA IBIS Open Forum facilitates data exchange for modeling. Not only do IBIS Specifications support traditional IBIS models, they also support SPICE, S-Parameters, VHDL-AMS, and Verilog-AMS. These other models are optimized for different simulation jobs than the original IBIS model.

As engineers scale up from ICs and gate-level physics to complex system emissions from a cabinet, they need to address turning "physical" models into "behavioral" models. This is because simulation run time increases as the number of nodes[3] unless abstraction strategies such as equation-based models are used.

My opinion is that engineers will increasingly need to also turn to statistics and probability to design complex systems. As physical systems become more complex, a given manufactured unit's behavior becomes more random and probabilistic because of process variation. The process variation is illustrated by population histograms.

In 2007, the EIA IBIS Open Forum has worked on the following activities:

1. Subcommittee for Specification on IBIS Model Quality

To improve the quality of IBIS models, the IBIS Model Quality Specification (IQ Spec) is being developed to guide model makers through the steps necessary to produce a quality model that will run in a simulator. The IQ Spec also provides a list of correctness checks and correlation checks for the model.

The Subcommittee for Specification on IBIS Model Quality has a weekly phone-in meeting on Tuesdays. The specification has been reviewed up to section 4 (V1.1r). In all, there are six sections. After the subcommittee's work has been completed and accepted by the EIA IBIS Open Forum, the Spec will be submitted for EIA vetting as a standard.

Quality Level Definitions
The IQ level is defined as a combination of correctness checks and correlation checks. The correctness level is a number from 0 to 4, and other modifiers are: M = measured, S = simulated, X = exceptions as noted. Some examples are:

IQ0	No IQ checking at all.
IQ1	Passes IBISCHK without errors or unexplained warnings.
IQ2	IQ1 + data for basic simulation checked.
IQ3	IQ2 + data for timing analysis checked
IQ4	IQ3 + data for power analysis checked
IQ3M	IQ3 + correlated against hardware measurements
IQ3MS	IQ3 + correlated against measurements and simulation
IQ4X	IQ4, but exceptions to checks commented in file

Quality Subcommittee website: http://www.vhdl.org/pub/ibis/quality_wip/

Regular Attendees

Bob Ross	Teraspeed Consulting Group
David Banas	Xilinx
Eckhard Lenski	Siemens
Kim Helliwell	LSI Logic
Mike LaBonte	Cisco - Chair
Moshiul Haque	Micron Technology
Roy Leventhal	Leventhal Design & Communications

2. Touchstone/IBIS Joint Draft Specification V 2.0

Agilent's Touchstone® is a proprietary de facto industry standard on S-Parameters. To expand the capability for the Touchstone format and create a neutral standard enhancement to Touchstone a subcommittee has been working with Agilent. The new draft standard provides:

- Complete backward compatibility with Touchstone 1.0.
- Per-port impedance references. This facilitates power to signal port modeling of coupling and Power Integrity simulation.
- Removal of upper limits on number of data points and number of ports. This facilitates modeling of large ICs.
- Some minor fixes and clarifications. In Touchstone 1.0, Z and Y were normalized with respect to Z_0. In Touchstone 2.0, Z and Y are non-normalized and independent of Z_0. Z_0 is specified.

The subcommittee's website is: http://www.eda.org/pub/ibis/adhoc/interconnect/. The draft was submitted to the full EIA IBIS Open Forum on 6/22/07 to undergo EIA specification vetting. The website for the draft is: http://www.eda.org/pub/ibis/adhoc/interconnect/touchstone_spec2_draft8.pdf

The established approach to modeling interconnects is the IBIS Interconnect Modeling Specification (ICM). A major reason for the Touchstone upgrade is to make interactions between Touchstone S-parameters and ICM easier. ICM supports Touchstone S-parameter data today. Touchstone is not intended to be an alternative to ICM, but a supported subset.

Regular Attendees

Sanjeev Gupta	Agilent
Lynne Green	Green Streak Programs
Michael Mirmak	Intel - Chair
John Angulo	Mentor Graphics Corp.
Randy Wolff	Micron Technology
Sam Chitwood	Sigrity
Bob Ross	Teraspeed Consulting Group
Radek Biernacki	Agilent — from the group that originated Touchstone

3. Efforts to Address Model Accuracy and Correlation in IBIS

IBIS has had an accuracy specification for a number of years. Interest is growing in a new approach to the quantification of model accuracy data. In June 2007, a presentation on quantification of correlations was given at the DAC IBIS Summit Meeting. This presentation summarized the Feature Selective Validation (FSV) method combined with statistical methods. FSV addresses data granularity and accuracy; statistics and probability address the randomness of manufactured units. For details on the topic, a full presentation is at: http://www.semiconductorsimulation.com/Verification%20of%20Simulation%20Results.pdf

With a standard for FSV in place, credibility for modeling and simulation can be facilitated in the EMC/EMI community. The standard can enable exchange of quantified correlation data about measurement versus simulation.

An IEEE-EMC and IEEE-Standards Society study group is developing a specification (P1597) for FSV. Andy Drozd, Bruce Archambeault, and others are involved. The subject is documented on IEEE Explorer: http://ieeexplore.ieee.org/Xplore/login.jsp?url=/iel5/9324/29634/01349883.pdf?arnumber=1349883

4. Advanced Technology Modeling Subcommittee (ATM)

The ATM subcommittee has weekly phone-in meetings on Tuesdays. The ATM work is somewhat hybrid. The original ATM charter was, as the Macromodeling Committee, to provide equivalent libraries between Berkeley SPICE and AMS, so that lack of EDA tool support for either family would not result in an inability to simulate. This work has essentially completed, and the focus has shifted to non-AMS solutions to SERDES modeling problems through the algorithmic approach.

The scope now includes algorithmic modeling for SerDes, plus methods to link to executables and dll's for proprietary digital equalization, methods for filtering algorithms, and methods for statistical processing of serial topologies for eye diagrams and jitter BER. A draft specification is under review.

The ATM Subcommittee website is at: http://www.eda-stds.org/ibis/macromodel_wip/. Their work-in-progress includes providing a library of analog macromodel elements. These elements are defined so that it is possible to create advanced models by wiring them into a circuit:

The Macromodel Element Library: http://www.eda-stds.org/ibis/macromodel_wip/element_lib allows tools that support Verilog-AMS and VHDL-AMS to directly use library AMS code; tools that do *not* support the AMS languages may use code defined in SPICE, with guaranteed equivalency.

The Macromodel Template Library: http://www.eda-stds.org/ibis/macromodel_wip/template_lib/ contains circuits implementing common advanced models using the macromodel library. These models are provided as examples, but are potentially useful for creating specific IBIS [External Circuit] implementations of a particular type of device.

Free tools are available to help developers of macromodel element implementations and macromodel netlist circuits at: http://www.eda-stds.org/ibis/macromodel_wip/tools/.

Regular Attendees

Ambrish Varma	Cadence Design Systems
Arpad Muranyi	Intel Corp. - Chair
Bob Ross	Teraspeed Consulting Group
Hemant Shah	Cadence Design Systems
Ian Dodd	Agilent
Joe Abler	IBM
John Angulo	Mentor Graphics
C. Kumar	Cadence Design Systems
Michael Mirmak	Intel Corp.
Mike LaBonte	Cisco Systems
Mike Steinberger	SiSoft
Radek Biernacki	Agilent (EESof)
Randy Wolff	Micron Technology
Richard Ward	Texas Instruments
Todd Westerhoff	SiSoft

5. IBIS "3S" Proposal for SPICE

At DAC 2007, Michael Mirmak, IBIS chairman, presented a paper to open a discussion about standardizing SPICE. The proposed SPICE Superset Specification ("3S") would combine the

most common features of proprietary and university SPICEs, for use in behavioral signal integrity modeling. Alternately, Verilog-A represents an extant standardized analog circuit format/language with more capabilities than current proprietary SPICEs. However, the lack of transmission line models (or at least, common libraries) is a major deficit for adapting it to SI work.

Both formats are already supported through the most recent versions of IBIS. IBIS 4.1 supports VHDL-AMS and Verilog-AMS code, where digital ports are required. Berkeley SPICE, as the closest to a standard SPICE, is also supported, with A/D and D/A connection features. IBIS 4.2 was expanded to support analog-only VHDL-AMS and Verilog-AMS (Verilog-A) code.

Current EIA IBIS Open Forum Officers

Chair: Michael Mirmak, Intel Corporation, michael.mirmak@intel.com

Vice-Chair: Syed Huq, Cisco Systems, shuq@cisco.com

Secretary: Randy Wolff, Micron Technology, rrwolff@micron.com

Librarian: Lance Wang, IO Methodology Inc., lwang@iometh.com

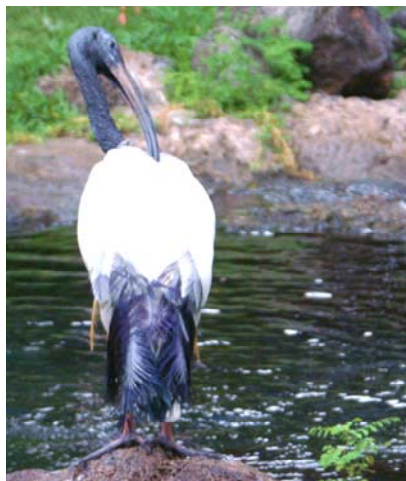Webmaster: Syed Huq, Cisco Systems, shuq@cisco.com

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Chris Denham, cdenham@geia.org

An IBIS Sighting at the Symposium!

IBIS was seen on the grounds of the Hilton Waikiki Village where many of the EMC2007 attendees stayed. Here's proof!

An IBIS relaxing near the pool.

A sign by the pool telling the visitor about the IBIS.

If you'd like to learn more about IBIS or the committees, please visit the EIA IBIS Open Forum website: http://www.eigroup.org/ibis/default.htm or contact Roy Leventhal at Roy.Leventhal@IEEE.org