**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER:** 226

**ISSUE TITLE:** PSIJ Sensitivity

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**DEFINITION OF THE ISSUE:**

The current IBIS specification (v7.2) only supports up to four supply terminals per buffer, [Pullup Reference], [Pulldown Reference], [POWER Clamp Reference] and [GND Clamp Reference]. Even if the [Model] includes the [ISSO PU], [ISSO PD] and [Composite Current] keywords to make it “power aware”, the [Model] may not include the power supply induced jitter (PSIJ) effects caused by voltage fluctuations in supply rails that are associated with other circuit blocks related to the buffer, such as pre-drivers, clock distribution tree and other logic blocks.

Furthermore, current signal integrity (SI) and power integrity (PI) co-simulations using power aware IBIS [Model]s are not able to include all PSIJ effects, such as:

(1) one power supply noise impacting multiple circuit blocks, such as digital control circuit blocks and analog front end circuit blocks, within one I/O interface,

(2) multiple power supply noise impacting one circuit block simultaneously,

(3) coupled power supply noise impacting one or more circuit blocks in one interface from circuit blocks in other I/O interfaces which share the same power supply rail(s), and

(4) PSIJ in front-end circuit blocks passed to subsequent circuit blocks.

This BIRD proposes to extend the IBIS specification to support SI & PI co-design through analyzing the holistic jitter impact from all power supplies to all circuit blocks of an I/O interface by adding the [PSIJ Sensitivity Rail] / [End PSIJ Sensitivity Rail] keyword pair, as illustrated in Figure-1.

This BIRD also proposes to add the [PSIJ Sensitivity] / [End PSIJ Sensitivity] keyword pair to group all [PSIJ Sensitivity Rail] / [End PSIJ Sensitivity Rail] keyword pairs together with [PSIJ Sensitivity Signal] / [End PSIJ Sensitivity Signal] keyword pair and [PSIJ Voltage List] /[End PSIJ Voltage List] keyword pair for all power supply rails involved in one I/O interface, as illustrated in Figure-1 below.

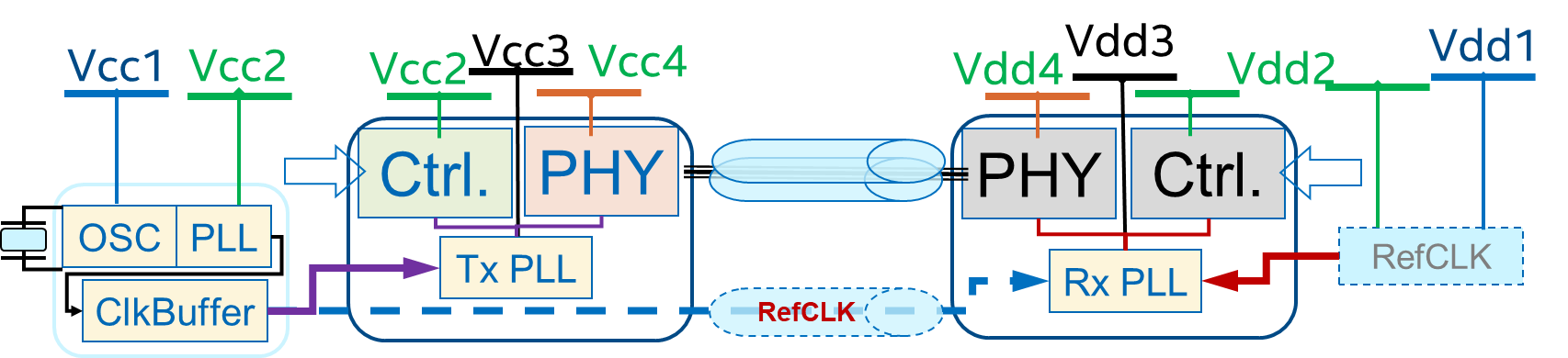


Figure-1. One I/O interface

With the data rate continuously increasing in high-speed I/O (HSIO) interfaces, in both the serial links, such as PCIe, USB, Display Port and Thunderbolt, and the parallel links, such as the memory interfaces of DDRx, LPDDRy and GDDRz, the Unit Interval (UI) keeps shrinking, and consequently the jitter timing budget keeps getting smaller. Meanwhile the evolving silicon process lowers the operating voltage of transistors resulting in smaller voltage margin for the power supply rails.

As shown in Figure-1, a HSIO interface usually includes equalization and CDR (Clock Data Recovery) in the Tx and Rx PHY circuits using multiple power supply rails, which may be dedicated or shared among the digital and analog circuit blocks. The jitter of a HSIO interface comes from its data and clock channels, and its Reference Clock channel, common or independent to Tx and Rx. The total jitter of a HSIO interface is induced by its SI channel and the power supply noise which may come from multiple power supply rails. This total jitter is further subdivided into deterministic jitter Dj and random jitter (using peak-to-peak or RMS values).

Traditionally, the SI and PI analysis for a HSIO interface was performed independently. The total jitter of a HSIO interface was a direct sum of the contribution from the worst-case SI channel and the worst-case PI PDN. This would usually result in over-design since the worst-case SI channel does not happen simultaneously with the worst-case PI PDN on a particular platform. The jitter contribution as listed in the parentheses in equation (1) might not be included from some of the circuitry, such as Tjctrl from control (Ctrl) circuit blocks, or TjPMfrom power management (PM), etc.

Tj = TjSI+TjPI(+TjPM+Tjctrl1+…) (1)

The status quo of jitter analysis for a HSIO interface is to perform SI and PI co-simulations, and to measure the total jitter TjEye of eye diagram resulting from the SI and PI co-simulation. The SI and PI co-simulations could utilize either transistor level models, which are very time consuming, making it impossible to include all jitter contributing circuitry, or could utilize power-aware IBIS models, which simulate much faster but may be less accurate since currently they cannot include the jitter contributions from all jitters contributing circuity. As illustrated in the parentheses, the jitter contribution TjPM from power management (PM) also needs lab verification, since there is no good algorithm to include the jitter contributions in SI and PI co-simulation, as implied in equation (2).

Tj = TjEye(+TjPM+…) (2)

**SOLUTION REQUIREMENTS:**

Table 1: Solution Requirements

|  |  |
| --- | --- |
| **Requirements** | **Notes** |
| The proposed [PSIJ Sensitivity] / [End PSIJ Sensitivity] keyword pair shall be defined, to group all keyword pairs of [PSIJ Sensitivity Rail] and [End PSIJ Sensitivity Rail] together with [PSIJ Sensitivity Signal] / [End PSIJ Sensitivity Signal] keyword pair and [PSIJ Voltage List] / [End PSIJ Voltage List] keyword pair for all power supply rails, having jitter impact to the signals in each I/O interface. |  |
| The proposed [PSIJ Sensitivity Rail] and [End PSIJ Sensitivity Rail] keyword pair shall be defined for every power supply rail, which is physically routed separately on the platform, with non-negligible noise impacting jitters for all signals in an I/O interface. |  |
| The proposed [PSIJ Sensitivity Signal] and [End PSIJ Sensitivity Signal] keyword pair should be defined for each type of signals with non-negligible jitter impact from each [PSIJ Sensitivity Rail] under each IO interface protocol described in [PSIJ Sensitivity]. |  |
| The [PSIJ Sensitivity Signal]   1. shall be defined for each type of signals for every [PSIJ Sensitivity Rail] under each IO interface protocol described in [PSIJ Sensitivity] but might not for a [PSIJ Sensitivity Rail] with negligible PSIJ sensitivity to a signal, in whole frequency range. The [PSIJ Sensitivity] is a superset of [ISSO PU], [ISSO PD] in a “power aware” [Model], and includes the contribution of [ISSO PU], and [ISSO PD]. 2. shall be a collective impact, additively or multiplicatively, from each [PSIJ Sensitivity Rail] to the signal type in an IO interface protocol, providing power supply to more than one circuit blocks of the concerned signals in an IO interface protocol. 3. shall be defined in frequency domain, including the starting frequency point of 0Hz for DC, up to the up-bound frequency point in GHz range. Unless specified by an available industry specification, the actual high-end frequency point shall not exceed the bandwidth of the I/O signal, which is defined by 1/(π\*tr), where tr is the rising time of high-speed I/O (HSIO) signal of concerned HSIO interface. 4. shall be the collective jitter impact of every power supply rail, which is accumulated or integrated from the convolution of its [PSIJ Sensitivity Rail] and total power supply noise which includes the coupling noise from other interfaces. The jitter value calculated from each power supply rail shall be additive for one I/O interface. 5. shall be described in PWL table of PSIJ sensitivity in s/V (second/voltage) in terms of frequency in first column, with typical PSIJ sensitivity values in second column. |  |
| The proposed [PSIJ Voltage List] and [End PSIJ Voltage List] keyword pair shall be defined with each [PSIJ Sensitivity] including all [PSIJ Sensitivity Rail] and GND rail. Conversely, a power rail listed within the keyword pair of [PSIJ Voltage List] and [End PSIJ Voltage List] may be excluded from any keyword pair of [PSIJ Sensitivity Rail] and [End PSIJ Sensitivity Rail], if its noise impacting jitter is negligible, or it is not even a power supply to a concerned I/O interface protocol. |  |

**PROPOSED CHANGES:**

1. **INTRODUCTION**

The total jitter of HSIO signal shall be categorized into deterministic jitter (Dj) and random jitter (Rj). Rj is unpredictable electronic noise, usually following a Gaussian distribution, and primarily caused by microscopic variations and thermal processes. It is usually covered by SI Bit-Error-Rate (BER) analysis, or directly provided by HSIO IP vendors as a platform design budget. Dj is predictable noise, coming from SI channel and PI noise through the PDN, as shown in equation (3).

Dj = DjSI + DjPI (3)

DjSI comes from SI eye diagram simulations, assuming all ideal power supplies to both Tx and Rx. DjPI is the total jitter contribution from the noise generated by all Tx and Rx circuit blocks in all the power supply rails in a HSIO interface, as shown in equation (4). For a HSIO interface, each power supply rail has its power supply induced jitter (PSIJ) sensitivity in frequency.

DjPI = (4)

The Fourier transform of Vnoise of the transistor circuit (CKT) block multiplied by PSIJ sensitivity is the jitter spectrum in the frequency domain, and the iFFT of this jitter spectrum is the jitter waveform in time domain, as shown in Figure-2.

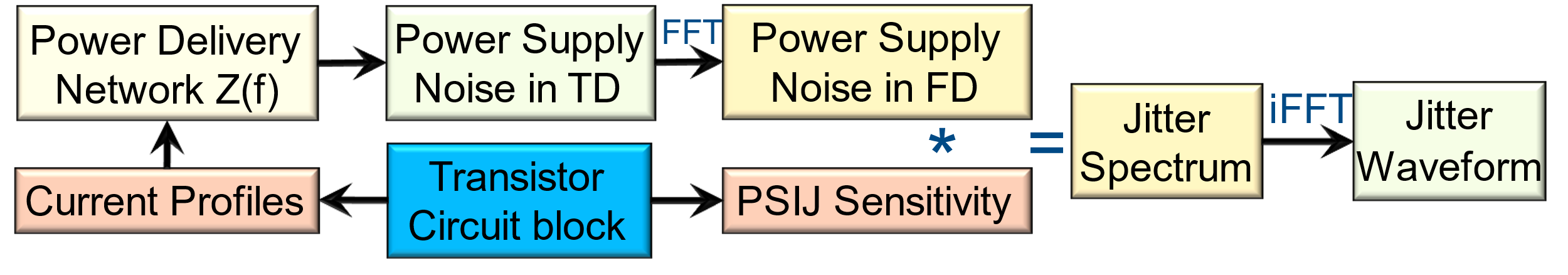


Figure-2. Jitter waveform of one power rail to a CKT block with PSIJ sensitivity

PSIJ sensitivity shall be measured or simulated for a circuit block CKT\_i as shown in Figure-3.

The simulation of PSIJ sensitivity PSIJ\_Vcc\_m\_CKT\_i from power supply Vcc\_m, starts from

Vcc\_m = Vtyp + A\*sin(2\*pi\*f\*t) (5)

A = (Vmax -Vmin)/2 (6)

PSIJ\_Vcc\_m\_CKT\_i(f)=Jitter\_PP(f)/(2\*A) (7)

where Vtyp, Vmax and Vmin are the typical, maximum, and minimum voltage values of the VCC\_m power supply. A and f are magnitude and frequency of power supply noise, and Jiiter\_pp is the peak-to-peak jitter in the output signal Sout induced by the power noise and with zero input jitter in Sin.

Meanwhile each circuit CKT\_i shall have a jitter transfer function JTF\_i (f), which is defined between the jitter of output signal Sout (f) and jitter of input signal Sin (f), as shown in equation (8)

JTF\_i(f)= Jitter\_of\_Sout\_i(f) /Jitter\_of\_Sin\_i(f) (8)

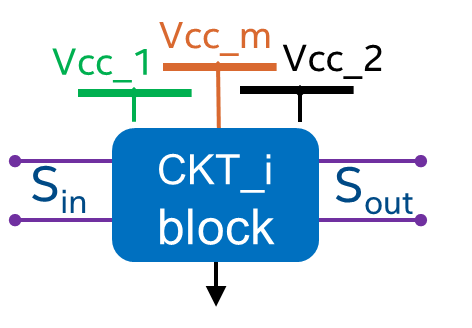
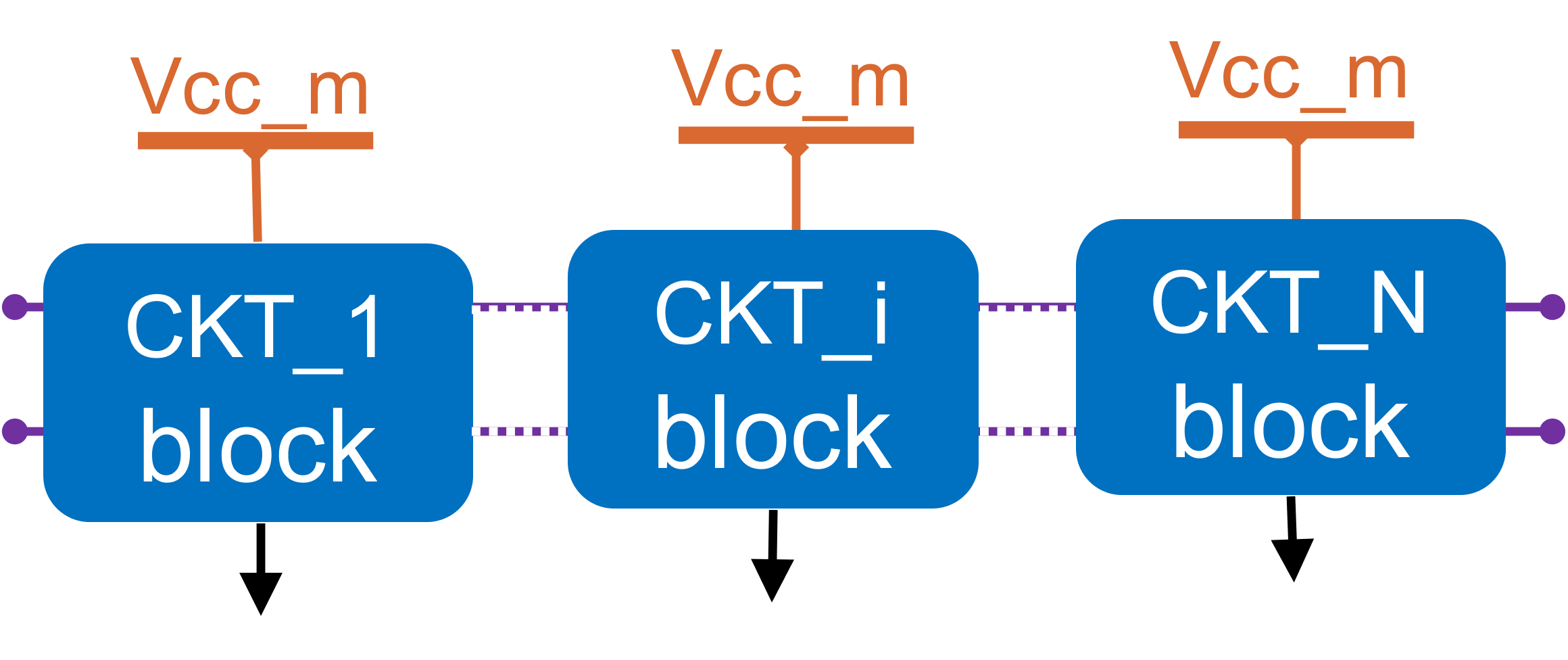
 

Figure3 - CKT\_i with multiple power supplies Figure 4 - Multiple CKT with one power supply

Here is one example illustrating PSIJ calculation of one power rail supplying multiple cascading CKT blocks chain. Given Vcc\_m power supplies to multiple circuit blocks, including CKT\_1, CKT\_i and CKT\_N in one HSIO interface as shown in Figure-4, the collective Vcc\_m PSIJ sensitivity to the HSIO interface is demonstrated in equation (9), in which covers up to N circuit blocks of PSIJ\_Vcc\_m\_CKT\_i.

PSIJ\_Vcc\_m\_i = PSIJ\_Vcc\_m\_(i-1) \* JTF\_i + PSIJ\_Vcc\_m\_CKT\_i, i ∊ 2, … N (9)

PSIJ\_Vcc\_m\_1 = PSIJ\_Vcc\_m\_CKT\_1 (10-1)

PSIJ\_Vcc\_m = PSIJ\_Vcc\_m\_N (10-2)

For a type of signals upon a particular circuit architecture, PSIJ sensitivity of CKT\_i, i ∊ 2, … N, are PSIJ\_VCC\_m\_(i-1)multiplicative to the JTF\_i of each CKT\_i stage, and then accumulative to PSIJ\_VCC\_m\_CKT\_i, as shown in equation (9), to calculate PSIJ sensitivity of CKT\_2, up to CKT\_N deductively. The PSIJ sensitivity of Vcc\_m from CKT\_1 is simplified in equation (10-1). The collective PSIJ sensitivity of Vcc\_m power supply for the circuitry of a holistic HSIO interface, is shown in equation (10-2), and illustrated in Figure-5.

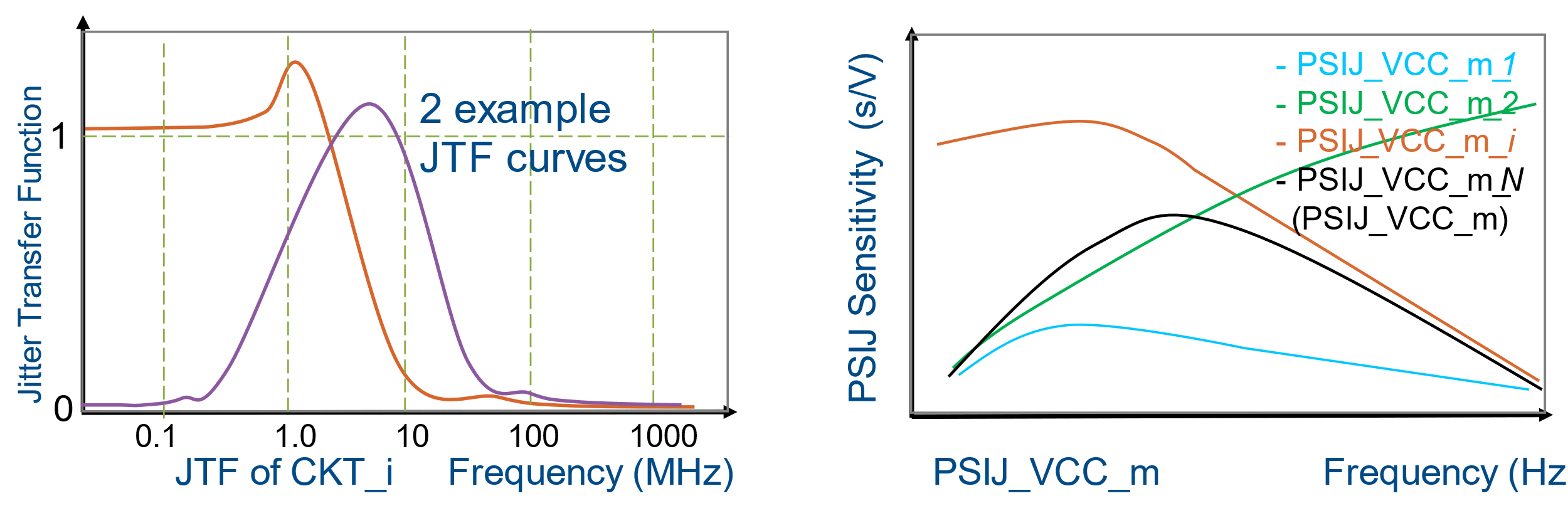


Figure 5 - Total Vcc\_m PSIJ Sensitivity to a type of signals from all involved CKT blocks

For a transmitter (Tx) circuit chain, the is measured at the output pin of last stage with a typical testing load. For a receiver (Rx) circuit chain, the is measured at the input to the latching circuit.

With known PSIJ sensitivity of each type of signals from every power supply rail of an entire HSIO interface operating in a protocol, from different IP vendors upon different processes with different technologies, it shall be easier for IP users to choose from all the available IP vendors’ offerings, besides considering the cost structure including Performance Power and Area (PPA).

With the operating protocol of an entire HSIO interface either serial or parallel declared in [PSIJ Sensitivity], each [PSIJ Sensitivity Rail] should be specified, the same as that in [PDN Domain], by a bus label and the reference GND with signal\_name declared in the [Pin]. The total PSIJ sensitivity should be further specified with [PSIJ Sensitivity Signal], such as PCIe-Tx and PCIe-Rx for a PCIe interface, TMDS and CLK in a HDMI interface, DQ, DQS, CMD, Addr and CLK in a DDRx, LPDDRy or GDDRz interface respectively. A [PSIJ Sensitivity Signal] should be specified by a model\_name in the [Pin], for the same type of signals for an PHY operating in same protocol.

Figure-6 illustrates four different PSIJ sensitivity curves of one major power supply for the same PSIJ sensitivity signals, from two different IP vendors upon two different processes. Given the in-par cost structure, the HSIO IP is better from vendor2 than from vendor1, and better from process1 than from process2. Consequently, the HSIO IP is the best from process1 of vendor2.

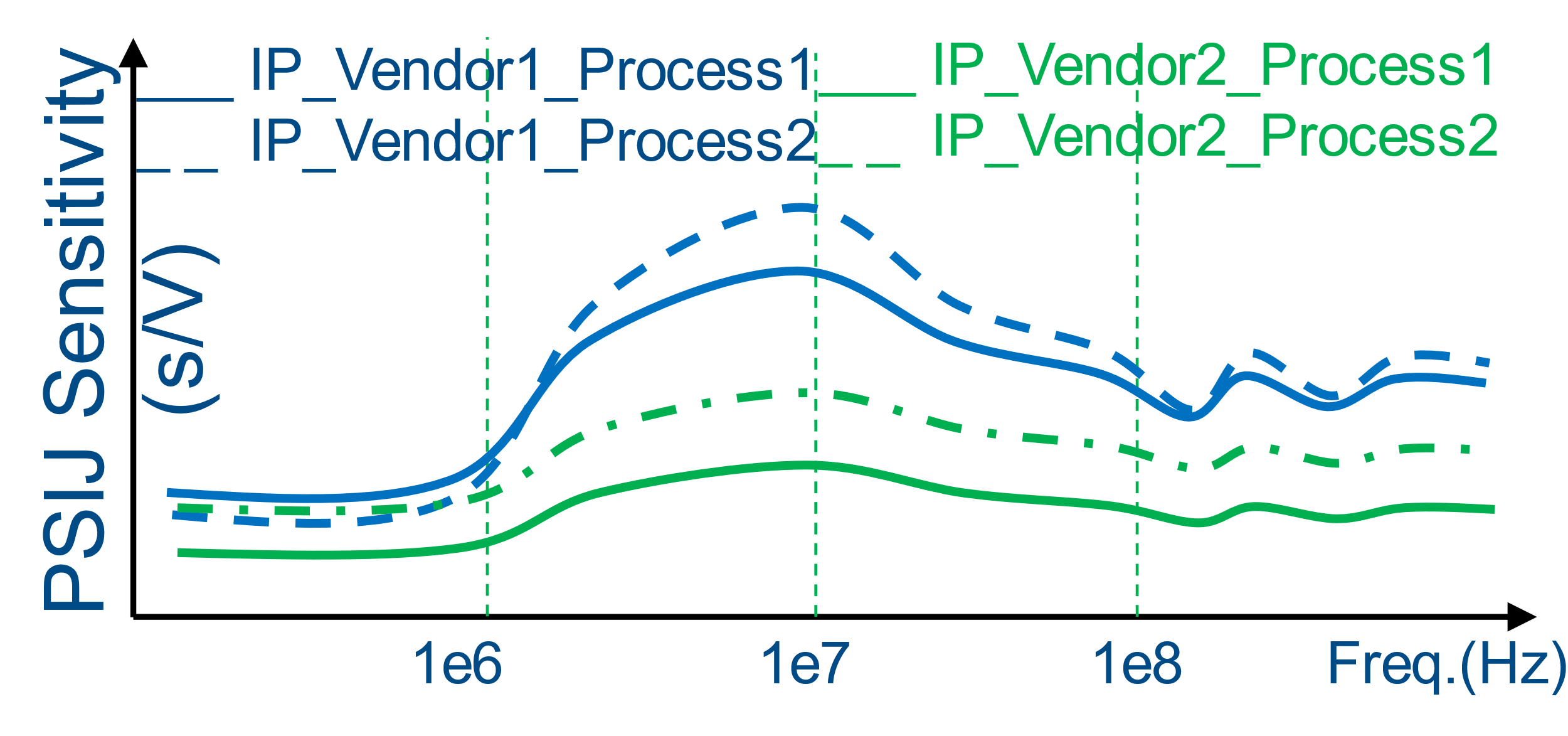


Figure 6 - PSIJ Sensitivity from different IP vendors and different processes

**Tale 2- IBIS Keywords and Subparameters**

|  |  |
| --- | --- |
| Keywords or subparameter | Notes |
| [PSIJ Sensitivity] | It is optional in a .ibs file. |
| [PSIJ Sensitivity Rail] | It is optional in a .ibs file. It is required within [PSIJ Sensitivity]. |
| [PSIJ Sensitivity Signal] | It is optional in a .ibs file. It is required within [PSIJ Sensitivity Rail]. |
| [End PSIJ Sensitivity Signal] | It is optional in a .ibs file. It is required within [PSIJ Sensitivity Signal]. |
| [PSIJ Voltage List] | It is optional in a .ibs file. It is required with [PSIJ Sensitivity Rail]. |
| [End PSIJ Voltage List] | It is optional in a .ibs file. It is required with [PSIJ Voltage List]. |
| [End PSIJ Sensitivity Rail] | It is optional in a .ibs file. It is required with [PSIJ Sensitivity Rail]. |
| [End PSIJ Sensitivity] | It is optional in a .ibs file. It is required with [PSIJ Sensitivity]. |

Add to ibs FILE [PSIJ Sensitivity] under [Component] after [Interconnect Model Group], [Device SPIM Group] or at a location approximately in order where it appears in the IBIS Specification.

ibs FILE

│…..

│

├── **[Component]** Si\_location, Timing\_location

│ │

│ │ …..

│ │

│ ├── **[Interconnect Model Group]**

│ │ └── **[End Interconnect Model Group]**

│ │

│ │

│ ├── **[PSIJ Sensitivity]**

│ │ ├── **[PSIJ Sensitivity Rail]** signal\_name

│ │ │ ├── **[PSIJ Sensitivity Signal]** model\_name

│ │ │ │ └── **[End PSIJ Sensitivity Signal]**

│ │ │ │

│ │ │ └── **[End PSIJ Sensitivity Rail]**

│ │ │

│ │ ├── **[PSIJ Voltage List]**

│ │ │ └── **[End PSIJ Voltage List]**

│ │ │

│ │ └── **[End PSIJ Sensitivity]**

│ │ …..

│ │

*Keyword:* **[PSIJ Sensitivity]**

*Required:* No. Required when [PSIJ Sensitivity Rail] is defined for at least one power supply rail in an I/O interface operating in a particular standard or protocol.

*Description*: Declares operating protocol of an I/O interface and the beginning of [PSIJ Sensitivity Rail] for the power supply rails.

*Usage Rules:* The [PSIJ Sensitivity] / [End PSIJ Sensitivity] keyword pair is used to define a list of [PSIJ Sensitivity Rail]s by name that shall be used together for one concerned IO interface operating in a particular standard or protocol in a simulation. A simulation may contain [PSIJ Sensitivity Rail]s of all power rails listed in only one keyword pair of [PSIJ Sensitivity] and [End PSIJ Sensitivity]. The [PSIJ Sensitivity] / [End PSIJ Sensitivity] keyword pair is hierarchically scoped by the [Component] keyword.

A [Component] may contain zero or more [PSIJ Sensitivity] keywords (identified by a name). Each [PSIJ Sensitivity] must contain at least one [PSIJ Sensitivity Rail] / [End PSIJ Sensitivity Rail] keyword pair for one power rail. The keyword [PSIJ Sensitivity] accepts a single string argument which is an I/O interface name. The I/O interface name may be used to further describe the selected function, if the I/O is configurable for supporting multiple interface standards or protocol. This string argument shall be no longer than 40 characters and shall not include whitespace.

*Example:*

[PSIJ Sensitivity] PCIe\_Gen4

| …

[End PSIJ Sensitivity]

[PSIJ Sensitivity] PCIe\_Gen5

| …

[End PSIJ Sensitivity]

| …

[PSIJ Sensitivity] TypeC

| …

[End PSIJ Sensitivity]

*Keyword:* **[End PSIJ Sensitivity]**

*Required:* No. Required if [PSIJ Sensitivity] keyword is present.

*Description:* Indicates the end of the data after [PSIJ Sensitivity].

*Example:*

[End PSIJ Sensitivity Group]

*Keyword:* **[PSIJ Sensitivity Rail]**

*Required:* No. Required when [PSIJ Sensitivity Rail] is defined for at least one power supply rail in an I/O interface.

*Description:* This keyword pair declares the IO POWER supply rail and its unique reference GND, with the next level two keywords of signal\_name at pin level. One signal\_name is for Power, and the other signal\_name for the reference GND.

*Sub-Params:* signal\_name

*Usage Rules:* The keyword [PSIJ Sensitivity Rail] accepts a string argument, on the same line, which is usually listed as PSR\_of\_<signal\_name> of a POWER supply rail. This string argument shall be no longer than 40 characters and shall not include whitespace.

The keyword pair of [PSIJ Sensitivity Rail] and [End PSIJ Sensitivity Rail] may appear multiple times, each with a unique PSR\_of\_<signal\_name> of a POWER supply rail, within a keyword pair of [PSIJ Sensitivity] and [End PSIJ Sensitivity] for the POWER supply rails in one I/O interface operating in one standard or protocol.

All power supply rails shall be listed with the keyword pairs of [PSIJ Sensitivity Rail] and [End PSIJ Sensitivity Rail], to evaluate the overall total jitter impact to an I/O interface, except when the power supply rail has extremely low PSIJ sensitivity or negligible noise to jitter impact to the I/O interface.

No [PSIJ Sensitivity Rail] / [End PSIJ Sensitivity Rail] keyword pair using the same power rail name (string argument) shall appear twice within the same [PSIJ Sensitivity] / [End PSIJ Sensitivity] pair.

signal\_name rules:

The signal\_name sub-parameter is followed by the name, up to 40 characters, of a signal\_name declared in the [Pin] section of the .ibs file. Only a signal\_name associated with POWER or GND can be used. All pins associated with the same signal\_name shall be considered as physically connected within one power delivery network.

*Example:*

[PSIJ Sensitivity] LPDDR4

[PSIJ Sensitivity Rail] PSR\_of\_VDD1

signal\_name VDD1 | signal\_name VDD1 is an IO power supply rail for LPDDR4 PHY.

signal\_name Vss

| …

[End PSIJ Sensitivity Rail]

[PSIJ Sensitivity Rail] PSR\_of\_VDD2

signal\_name VDD2 | signal\_name VDD2 is an IO power supply rail for LPDDR4 PHY.

signal\_name Vss

| …

[End PSIJ Sensitivity Rail]

[PSIJ Sensitivity Rail] PSR\_of\_VDDQ

signal\_name VDDQ | signal\_name VDDQ is an IO power supply rail for LPDDR4 PHY.

signal\_name VSS

| …

[End PSIJ Sensitivity Rail]

[End PSIJ Sensitivity]

*Keyword:* **[End PSIJ Sensitivity Rail]**

*Required:* No. Required if [PSIJ Sensitivity Rail] keyword is present.

*Description:* Indicates the end of the data after [PSIJ Sensitivity Rail].

*Example:*

[End PSIJ Sensitivity Rail]

*Keyword:* **[PSIJ Sensitivity Signal]**

*Required:* No. Required when [PSIJ Sensitivity Signal] is defined for at least one type of signals in an I/O interface operating in a particular standard, or protocol.

*Description:* This keyword pair describes the Power Supply Induced Jitter (PSIJ) sensitivity in PWL (Piece Wise Linear) table format in the frequency domain for a type of signals operating in the particular protocol of [PSIJ Sensitivity], to evaluate the jitter impact to the [PSIJ Sensitivity Signal] through all involved circuit blocks from the total power supply noise of the [PSIJ Sensitivity Rail].

*Sub-Params:* model\_name

*Usage Rules:* The keyword [PSIJ Sensitivity Signal] is followed by the next level keyword model\_name, on the next line, which is model name for the concerned type of signals.

PSIJ sensitivity signal shall be specified, even if there is only one type of signals being defined in an I/O interface operating in a particular standard or protocol specified in [PSIJ Sensitivity].

The keyword pair of [PSIJ Sensitivity Signal] and [End PSIJ Sensitivity Signal] may appear multiple times within one keyword pair of [PSIJ Sensitivity Rail] and [End PSIJ Sensitivity Rail]. Each keyword pair of [PSIJ Sensitivity Signal] and [End PSIJ Sensitivity Signal] should be defined for one type of signals within one [PSIJ Sensitivity Rail] and [End PSIJ Sensitivity Rail] keyword pair, under one [PSIJ Sensitivity] and [End PSIJ Sensitivity] for one IO interface operating in one protocol.

The [PSIJ Sensitivity Signal] keyword is followed by three (3) columns of data from the 4th line, consisting of one or more lines each containing three floating-point values separated by whitespace. The first column contains a frequency value in hertz (Hz). The second column contains an associated sensitivity value of magnitude in seconds-per-volt (s/V). The third column contains an associated sensitivity value of phase in degree, which should be within the range of 0 to 360. Values in the second or third column may be duplicated across lines. Values in the first column shall be provided in increasing order of frequency values (e.g., the row containing 0 Hz data shall appear before the row containing 1 Hz data, etc.). The number of frequency points provided should be sufficient to fit the data in the second and third columns, preferably with a cubic spline fitting algorithm, covering the entire frequency range of interest to document the worst case PSIJ profile, as shown by the blue curve in Figure-7, and not the detailed PSIJ curve as shown by the green curve in Figure-7. The number of frequency points in the table should not exceed 100.

model\_name rules:

The model\_name sub-parameter is followed by the name, up to 40 characters, of a model\_name declared in the [Pin] section of the .ibs file. Only a model\_name associated with I/O pins can be used, but not POWER, GND or NC. A model\_name, maps a pin to a specific I/O buffer model or model selector name.

*Example:*

[PSIJ Sensitivity] PCIe\_Gen4

[PSIJ Sensitivity Rail] PSR\_of\_VCC2

signal\_name VCC2

Signal\_name Vss

[PSIJ Sensitivity Signal]

model\_name PCIe\_Gen4\_TX | model\_name defined for same IO signals in the [Pin].

| frequency (Hz) magnitude(s/V) phase (degree)

0.0 1.00E-12 0

1.0E+03 1.00E-12 0

1.0E+04 2.00E-12 0

1.0E+05 1.20E-10 0

4.0E+05 1.20E-09 0

1.0E+06 3.00E-09 0

1.0E+07 5.40E-09 0

2.0E+07 5.80E-09 0

1.0E+08 4.50E-09 0

1.0E+09 4.30E-09 0

[End PSIJ Sensitivity Signal]

| The example PSIJ sensitivity curve of VCC2 is illustrated in Figure-7.

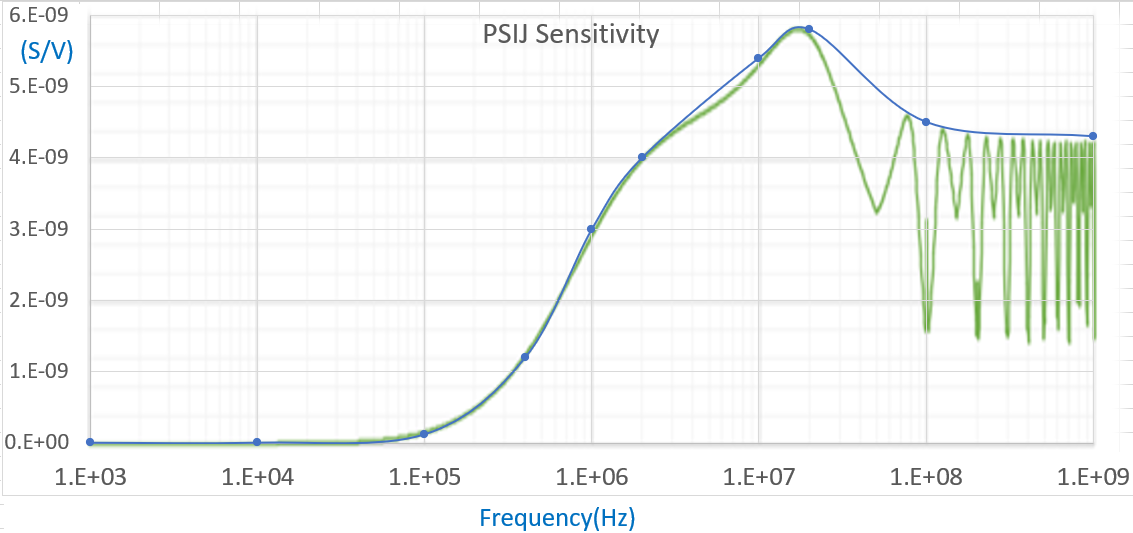


Figure 7 - Example PSIJ Sensitivity curve for VCC2 in PCIe\_Gen4

[PSIJ Sensitivity Signal]

model\_name PCIe\_Gen4\_RX

| frequency (Hz) magnitude(s/V) phase (degree)

0.0 1.10E-12 0

1.0E+03 1.20E-12 0

1.0E+04 2.20E-12 0

1.0E+05 1.30E-10 0

1.0E+06 3.10E-09 0

2.0E+06 4.10E-09 0

1.0E+07 5.50E-09 0

1.0E+08 4.60E-09 0

1.0E+09 4.20E-09 0

[End PSIJ Sensitivity Signal]

[End PSIJ Sensitivity Rail]

| …

[PSIJ Voltage List]

|V(name) V(typ) V(min) V(max)

VCC2 0.600 0.540 0.660

| …

VSS 0.000 0.000 0.000

[End PSIJ Voltage List]

[End PSIJ Sensitivity]

[PSIJ Sensitivity] DisplayPort

[PSIJ Sensitivity Rail] PSR\_of\_VDD1

signal\_name VDD1 | signal\_name VDD1 is an IO power supply for DisplayPort PHY.

Signal\_name VSS

[PSIJ Sensitivity Signal]

model\_name TMDS

| frequency (Hz) magnitude(s/V) phase (degree)

0.0 1.0e-9 0

1.0E+04 1.0e-9 0

1.0E+05 1.1e-9 0

1.0E+06 2.2e-9 0

1.0E+07 7.8e-9 0

1.0E+08 4.0e-9 0

1.0E+09 3.9e-9 0

[End PSIJ Sensitivity Signal]

[PSIJ Sensitivity Signal]

model\_name CLK

| frequency (Hz) magnitude(s/V) phase (degree)

0.0 1.0e-9 0

1.0E+04 1.0e-9 0

1.0E+05 1.1e-9 0

1.0E+06 2.2e-9 0

1.0E+07 7.8e-9 0

1.0E+08 4.0e-9 0

1.0E+09 3.9e-9 0

[End PSIJ Sensitivity Signal]

[End PSIJ Sensitivity Rail]

[PSIJ Sensitivity Rail] PSR\_of\_VCC2

signal\_name VCC2 | signal\_name VCC2 is an IO power supply for DisplayPort PHY.

signal\_name Vss

[PSIJ Sensitivity Signal]

model\_name TMDS

| frequency (Hz) magnitude(s/V) phase (degree)

0.0 2.0e-12 0

1.0E+04 2.0p 0

1.0E+05 2.7n 0

1.0E+06 3.0n 0

1.0E+07 4.9n 0

1.0E+08 4.1n 0

1.0E+09 3.8n 0

[End PSIJ Sensitivity Signal]

[PSIJ Sensitivity Signal]

model\_name CLK

| frequency (Hz) magnitude(s/V) phase (degree)

0.0 2.0e-12 0

1.0E+04 2.0p 0

1.0E+05 2.7n 0

1.0E+06 3.0n 0

1.0E+07 4.9n 0

1.0E+08 4.1n 0

1.0E+09 3.8n 0

[End PSIJ Sensitivity Signal]

[End PSIJ Sensitivity Rail]

| …

[PSIJ Voltage List]

|V(name) V(typ) V(min) V(max)

VDD1 1.000 0.900 1.100

VCC2 0.600 0.540 0.660

| …

VSS 0.000 0.000 0.000

[End PSIJ Voltage List]

[End PSIJ Sensitivity]

*Keyword:* **[End PSIJ Sensitivity Signal]**

*Required:* No. Required if [PSIJ Sensitivity Signal] keyword is present.

*Description:* Indicates the end of the data after [PSIJ Sensitivity Signal].

*Example:*

[End PSIJ Sensitivity Signal]

*Keyword:* **[PSIJ Voltage List]**

*Required:* No. Required when [PSIJ Sensitivity Rail] is defined for at least one power supply rail.

*Description:* This keyword defines the voltage for power the rails defined in [PSIJ Sensitivity Rail].

*Usage Rules*: Under the [PSIJ Voltage List] keyword are four columns:

The first column lists a rail signal\_name found within all [PSIJ Sensitivity Rail] and [End PSIJ Sensitivity Rail] keyword pairs. Duplicate entries in the first column are prohibited.

The second column, V(typ), lists the typical value of the voltage. This entry is required.

The third column, V(min), lists the minimum (by magnitude) value of the voltage. If missing, ‘NA’ is entered, and the default value is V(typ).

The fourth column, V(max), lists the maximum (by magnitude) value of the voltage. If missing, ‘NA’ is entered, and the default value is V(typ).

*Other Notes:* A power supply rail, defined within the keyword pair of [PSIJ Sensitivity Rail] and [End PSIJ Sensitivity Rail], shall be listed within the keyword pair of [PSIJ Voltage List] and [End PSIJ Voltage List]. A given power rail listed within [PSIJ Voltage List] and [End PSIJ Voltage List] keyword pair may be defined within multiple keyword pairs of [PSIJ Sensitivity Rail] and [End PSIJ Sensitivity Rail]. Conversely, a power rail listed within the keyword pair of [PSIJ Voltage List] and [End PSIJ Voltage List] may be excluded from any keyword pair of [PSIJ Sensitivity Rail] and [End PSIJ Sensitivity Rail] within a keyword pair of [PSIJ Sensitivity] and [End PSIJ Sensitivity] under [Component] keyword, if its noise impacting jitter is negligible, or it is not even a power supply to a concerned I/O interface.

*Example:*

[PSIJ Voltage List]

|V(name) V(typ) V(min) V(max)

VDD1 1.000 0.900 1.100

VCC2 0.600 0.540 0.660

VCC1 1.800 1.710 1.890

VSS 0.000 0.000 0.000

[End PSIJ Voltage List]

*Keyword:* **[End PSIJ Voltage List]**

*Required:* No. Required if [PSIJ Voltage List] keyword is present.

*Description:* Indicates the end of the data after [PSIJ Voltage List].

*Example:*

[End PSIJ Voltage List]

**BACKGROUND INFORMATION/HISTORY:**

[1] Kinger Cai, Fern Nee Tan, and Chi-te Chen, [[PSIJ Sensitivity] in IBIS](https://ibis.org/summits/aug22/cai2.pdf), IBIS Summit at 2022 IEEE Symposium on EMC+SIPI, August 2022

[2] Ralf Schmitt, Hai Lan, Chris Madden, and Chuck Yuan, [Investigating the Impact of Supply Noise on the Jitter in Gigabit 1/0 Interfaces](https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=4387157), IEEE, EPEPS, , Oct. 2007

[3] Analog Device, and Maximum Integrated, [Clock Jitter and Phase Noise Conversion](https://intel-my.sharepoint.com/personal/kinger_cai_intel_com/Documents/IEEEStandards/IEEE%202022%20EMC%20&%20SIPI%20Host/BIRD_SPIM/%5b2%5d), Dec. 2004