**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER:** 193

**ISSUE TITLE:** Figure 29 corrections

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**DATE SUBMITTED:** January 10, 2018

**DATE REVISED:**

**DATE ACCEPTED:** March 23, 2018

**DEFINITION OF THE ISSUE:**

Figure 29 and related examples in the IBIS v6.1 specification talk about “explicit pad connections” but there is also a note on pg. 131 which states that these types of connections are not supported by the specification:



Since BIRD189 defines a new syntax for connecting package models between pins and pads, and/or connecting on-die interconnect models between pads and buffer terminals, this statement will no longer be true after BIRD189 becomes part of the IBIS specification.

In addition, Figure 29 shows examples for joins and splits in the package model which are not supported in IBIS v6.1 and will not be supported by BIRD189 either. These unsupported concepts need to be removed from the figure and corresponding examples.

**SOLUTION REQUIREMENTS:**

The IBIS specification must meet these requirements:

Table : Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| 1. Remove any forward references to potential future package modeling syntax not supported by the specification | * Change figure 29 to be consistent with #1 * Chage the examples to be consistent with #1 |
| 1. Make sure that Figure 29, the related text and examples are consistent with BIRD189 |  |

**SUMMARY OF PROPOSED CHANGES:**

For review purposes, the proposed changes are summarized as follows:

Table : IBIS Keywords, Subparameters, AMI Reserved\_Parameters, and AMI functions Affected

|  |  |  |
| --- | --- | --- |
| Specification Item | New/Modified/Other | Notes |
|  |  |  |

(List each affected specification item in the table above, adding rows as needed.)

**PROPOSED CHANGES:**

On pg. 129/130, change the example from:

[Node Declarations] | Must appear before any [Circuit Call] keyword

|

| Die nodes:

a b c d e | List of die nodes

f g h nd1

|

| Die pads:

pad\_2a pad\_2b pad\_4 pad\_11 | List of die pads

|

[End Node Declarations]

To:

[Node Declarations] | Must appear before any [Circuit Call] keyword

|

| Die nodes:

a b c d e | List of die nodes

f g h nd1

|

[End Node Declarations]

On pg. 131, change:

Every occurrence of the Port\_map subparameter must begin on a new line and must be followed by two arguments, the first being a port name, and the second being a die node, die pad, or a pin name.

To:

Every occurrence of the Port\_map subparameter must begin on a new line and must be followed by two arguments, the first being a port name, and the second being a die node or a pin name.

On pg. 131, change:

“Please note that a pin name in the second argument does not mean that the connection is made directly to the pin. Since native IBIS does not have a mechanism to declare die pads explicitly, connections to die pads are made through their corresponding pin names (listed under the [Pin] keyword). This convention must only be used with native IBIS package models where a one-to-one path between the die pads and pins is assumed. When a package model other than native IBIS is used with a [Component], the second argument of Port\_map must have a die pad or die node name. These names are matched to the corresponding port name of the non-native package model by name (not by position). In this case, the package model may have an arbitrary circuit topology between the die pads and the pins. A one-to-one mapping is not required.”

To:

“Please note that a pin name in the second argument does not mean that the connection is made directly to the pin. Since IBIS assumes a one-to-one path between the die pads and pins (i.e. each pin has one and only one corresponding die pad, and each die pad has one and only one corresponding pin), it does not have a mechanism to declare die pads. Consequently, when the second argument of Port\_map contains a pin name, the connection is made to the die pad that is associated with that pin name.”

On pg. 131, delete the following text:

“The pad\_\* to pin connections in Figure 29 and in the example lines with the comment, "explicit pad connection", are shown for reference. The connection syntax has not yet been defined. Therefore, the connections for pad\_\* to pin are not supported in this specification.”

Page 132, Figure 29:

All “explicit pads” and joins/forks in the package model should be removed from the drawing as follows:

* change “pad\_11” to “11”
* change “pad\_2a” to “2”
* remove inductor between pin 2 and pad\_2b
* remove “pad\_2b”
* draw the “Analog Buffer Control” line to pad 2
* at [External Circuit] C change both “pad\_11” to “11” (the same way as “10”)
* at [External Circuit] D change “pad\_4” to “4” and “pad\_11” to “11” (like “10”)
* rename pin “4a Clocka” to “4 Clock”
* remove pin “4b Clockb” and associated inductor in package model box
* remove Note 2 below the figure

After making these changes, the figure should look as follows:



Pages 133-134, change the [Circuit Call] examples from:

[Circuit Call] A | Instantiates [External Circuit] named "A"

|

Signal\_pin 1

|

| mapping port pad/node

|

Port\_map A\_mypcr a | Port to internal node connection

Port\_map A\_mypur b | Port to internal node connection

Port\_map A\_mysig c | Port to internal node connection

Port\_map A\_mypdr d | Port to internal node connection

Port\_map A\_mygcr e | Port to internal node connection

|

[End Circuit Call]

|

|

[Circuit Call] B | Instantiates [External Circuit] named "B"

|

Signal\_pin 2

|

| mapping port pad/node

|

Port\_map A\_mypur f | Port to internal node connection

Port\_map A\_mysig g | Port to internal node connection

Port\_map A\_mypdr h | Port to internal node connection

Port\_map A\_mycnt pad\_2b | Port to explicit pad connection

|

[End Circuit Call]

|

|

[Circuit Call] C | Instantiates [External Circuit] named "C"

|

Signal\_pin 3

|

| mapping port pad/node

|

Port\_map A\_mypcr 10 | Port to implicit pad connection

Port\_map A\_mypur 10 | Port to implicit pad connection

Port\_map A\_mysig 3 | Port to implicit pad connection

Port\_map A\_mypdr pad\_11 | Port to explicit pad connection

Port\_map A\_mygcr pad\_11 | Port to explicit pad connection

Port\_map D\_mydrv nd1 | Port to internal node connection

|

[End Circuit Call]

|

|

[Circuit Call] D | Instantiates [External Circuit] named "D"

|

Signal\_pin 4a

|

| mapping port pad/node

|

Port\_map A\_my\_pcref 10 | Port to implicit pad connection

Port\_map A\_my\_signal pad\_4 | Port to explicit pad connection

Port\_map A\_my\_gcref pad\_11 | Port to explicit pad connection

Port\_map D\_receive nd1 | Port to internal node connection

|

[End Circuit Call]

|

|

[Circuit Call] Die\_Interconnect | Instantiates [External Circuit] named

| "Die\_Interconnect"

|

| mapping port pad/node

|

Port\_map vcc 10 | Port to implicit pad connection

Port\_map gnd pad\_11 | Port to explicit pad connection

Port\_map io1 1 | Port to implicit pad connection

Port\_map o2 pad\_2a | Port to explicit pad connection

Port\_map vcca1 a | Port to internal node connection

Port\_map vcca2 b | Port to internal node connection

Port\_map int\_ioa c | Port to internal node connection

Port\_map vssa1 d | Port to internal node connection

Port\_map vssa2 e | Port to internal node connection

Port\_map vccb1 f | Port to internal node connection

Port\_map int\_ob g | Port to internal node connection

Port\_map vssb1 h | Port to internal node connection

|

[End Circuit Call]

To:

[Circuit Call] A | Instantiates [External Circuit] named "A"

|

Signal\_pin 1

|

| mapping port pad/node

|

Port\_map A\_mypcr a | Port to internal node connection

Port\_map A\_mypur b | Port to internal node connection

Port\_map A\_mysig c | Port to internal node connection

Port\_map A\_mypdr d | Port to internal node connection

Port\_map A\_mygcr e | Port to internal node connection

|

[End Circuit Call]

|

|

[Circuit Call] B | Instantiates [External Circuit] named "B"

|

Signal\_pin 2

|

| mapping port pad/node

|

Port\_map A\_mypur f | Port to internal node connection

Port\_map A\_mysig g | Port to internal node connection

Port\_map A\_mypdr h | Port to internal node connection

Port\_map A\_mycnt 2 | Port to implicit pad connection

|

[End Circuit Call]

|

|

[Circuit Call] C | Instantiates [External Circuit] named "C"

|

Signal\_pin 3

|

| mapping port pad/node

|

Port\_map A\_mypcr 10 | Port to implicit pad connection

Port\_map A\_mypur 10 | Port to implicit pad connection

Port\_map A\_mysig 3 | Port to implicit pad connection

Port\_map A\_mypdr 11 | Port to implicit pad connection

Port\_map A\_mygcr 11 | Port to implicit pad connection

Port\_map D\_mydrv nd1 | Port to internal node connection

|

[End Circuit Call]

|

|

[Circuit Call] D | Instantiates [External Circuit] named "D"

|

Signal\_pin 4

|

| mapping port pad/node

|

Port\_map A\_my\_pcref 10 | Port to implicit pad connection

Port\_map A\_my\_signal 4 | Port to implicit pad connection

Port\_map A\_my\_gcref 11 | Port to implicit pad connection

Port\_map D\_receive nd1 | Port to internal node connection

|

[End Circuit Call]

|

|

[Circuit Call] Die\_Interconnect | Instantiates [External Circuit] named

| "Die\_Interconnect"

|

| mapping port pad/node

|

Port\_map vcc 10 | Port to implicit pad connection

Port\_map gnd 11 | Port to implicit pad connection

Port\_map io1 1 | Port to implicit pad connection

Port\_map o2 2 | Port to implicit pad connection

Port\_map vcca1 a | Port to internal node connection

Port\_map vcca2 b | Port to internal node connection

Port\_map int\_ioa c | Port to internal node connection

Port\_map vssa1 d | Port to internal node connection

Port\_map vssa2 e | Port to internal node connection

Port\_map vccb1 f | Port to internal node connection

Port\_map int\_ob g | Port to internal node connection

Port\_map vssb1 h | Port to internal node connection

|

[End Circuit Call]

On pg. 142-143 change:

“Since the [Merged Pins] keyword (defined below) provides a mechanism to explicitly and unambiguously define the connectivity of merged pins with greater detail and freedom, the use of the [Merged Pins] keyword is strongly recommended for new models in which merged pin modeling exists.”

To:

“Since the [Merged Pins] keyword (defined below) provides a mechanism to explicitly and unambiguously define the connectivity of merged pins with greater detail and freedom, the use of the [Merged Pins] keyword is strongly recommended for models in which merged pin modeling exists.”

**BACKGROUND INFORMATION/HISTORY:**

Note that while [Package], [Package Model] and R\_pin, L\_pin, C\_pin under the [Pin] keyword may coexist with [Interconnect Model Group] in the same [Component], BIRD189 prohibits the use of [External Circuit] and [Node Declarations] (consequently [Circuit Call]) together with [Interconnect Model Group]. Since this BIRD only affects the [Node Declarations] and [Circuit Call] keywords (with a very small editorial change under the [Merged Pins] keyword), the changes outlined in this BIRD are also compatible with BIRD189 without mentioning it. The source file for the update figure is “ver6.1 - Fig 29 - rc-02.vsd”.