**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER:** 176

**ISSUE TITLE:** Power Pin Package Modeling

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**STATEMENT OF THE ISSUE:**

Under the [Package] keyword, the IBIS specification defines a set of rules on the hierarchy of the various package modeling options. It is clearly stated that when present, the package information under the [Pin] keyword will override the package information in the [Package] keyword, and if present, the information in the [Package Model] and [Define Package Model] keywords will override the information in the [Pin] and [Package] keywords.

The Usage Rules of the [Pin Numbers] keyword in the [Define Package Model] keyword section do not prohibit a “partial package model”, i.e., a model which only describes a subset of a Component’s pins. The problem is that there are no rules under the [Pin Numbers] keyword to describe what the EDA tool should do when the keyword doesn't contain the name of a pin that is listed in the component's [Pin] keyword. In the absence of rules, model makers and EDA tool vendors may make different assumptions which may lead to incorrect simulation results. For example, when a pin name is missing under the [Pin Numbers] keyword one EDA tool might make use of the RLC values in the [Pin] or [Package] keyword, while others might implement an open or short instead.

**ANALYSIS PATH/DATA THAT LED TO SPECIFICATION:**

When creating coupled package models, it might be desirable to reduce the number of pins associated with power and ground, as these pins are often connected to plane structures in the package. Merging power/ground pins results in a more compact model. When this type of package model is used in IBIS with the [Define Package Model] format using [Model Data] containing R, L and C matrices, many pin names may be omitted under the [Pin Numbers] keyword that are associated with power and ground connections.

The usage of the [Package]/[Pin] RLC data for ***signal pins*** not defined in [Define Package Model] is acceptable, however, applying the same rule to ***power and ground pins*** not defined in [Define Package Model] is questionable as it seems that it may be better not to use the RLC data from the [Package]/[Pin] keywords for several reasons.

For data in the [Pin] keyword, representing the capacitance of a plane on multiple pins is an issue. In addition, there is no way to define critically important mutual inductances and capacitances.

For data in the [Package] keyword, the problem revolves around the min/max values. People use the min/max values based on the signal’s package parasitics, which is useless for the power/ground corner cases.

It seems that the only way to provide valid package model data for power integrity (PI) simulations is by placing it into the [Define Package Model] keyword, and by merging multiple power/ground pins into one pin while leaving the remaining pins in the group undefined or disconnected.

The proposed update to the IBIS specification in this BIRD describes the rules that when the [Pin Mapping] keyword defines power/ground buses that span over multiple power/ground pins (i.e., pads), the package parasitics of those power/ground pins should be merged into a single pin representation per group in the [Define Package Model] keyword and only one of the pin names for each of those groups should be present in the [Pin Numbers] keyword of the [Define Package Model] keyword.

Even though the new package/on-die interconnect specification proposal for IBIS is expected to resolve these problems, it might still be worth adding this change for the legacy package modeling syntax, since there may be numerous models which will never use the new package modeling syntax.

The table below summarizes the package model rules that already exist in this specification or are proposed in this BIRD, including the addition of [Merged Pins].

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POWER and GND PINS:

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[Component] Keyword [Define Package Model] EDA Tool Processing Expectation

Exists or Entries Exists or Entries

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[Pin] [Pin Mapping] [Pin Numbers] [Merged Pins] Expected Pin Package Model Source

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(RLC) NO NO \*\*Illegal RLC

(RLC) NO YES \*\*Illegal \*[Define Package Model] for [Pin Numbers] pins

 RLC for pins not in [Pin Numbers]

(RLC) YES NO \*\*Illegal RLC

(RLC) YES YES NO \*[Define Package Model] for [Pin Numbers] pins

 Unlisted pins connected to first [Pin Numbers] pin on same

 [Pin Mapping] bus overriding RLC (EDA tool is expected to

 make connection through first [Pin Numbers] pins and not

 to use RLC)

 RLC if NO [Pin Numbers] pin is declared from a

 [Pin Mapping] bus

(RLC) YES YES YES [Model Data] ONLY for [Pin Numbers] pins, [Merged Pins]

 shorted to [Pin Numbers] pin on the same bus as documented

 (All pins on [Merged Pins] keyword must be listed in the

 same [Pin Mapping] bus)

 RLC if [Pin Numbers] contain NO pins from a [Pin Mapping]

 bus (This is permitted)

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Signal PINS for [Model]/[External Model]

NC PINS (a generic package model could document [Define Package Model] connections):

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[Component] Keyword [Define Package Model] EDA Tool Optional Processing Expectation

Exists or Entries Exists or Entries

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[Pin] [Pin Mapping] [Pin Numbers] [Merged Pins] Expected Pin Package Model Source

----- ------------- ------------- ------------- ---------------------------------

(RLC) NO NO \*\*\*Illegal RLC

(RLC) NO YES \*\*\*Illegal \*[Define Package Model] for [Pin Numbers] pins

 RLC model for pins not in [Pin Numbers]

(RLC) YES NO \*\*\*Illegal RLC

(RLC) YES YES \*\*\*Illegal \*[Define Package Model] for [Pin Numbers] pins

 RLC model for pins not in [Pin Numbers]

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CIRCUITCALL PINS for Signal/POWER/GND paths using [External Circuit]:

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[Component] Keyword [Define Package Model] EDA Tool Optional Processing Expectation

Exists or Entries Exists or Entries

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[Pin] [Pin Mapping] [Pin Numbers] [Merged Pins] Expected Pin Package Model Source

----- ------------- ------------- ------------- ---------------------------------

(RLC) \*\*\*\*Illegal NO \*\*\*Illegal RLC

(RLC) \*\*\*\*Illegal YES \*\*\*Illegal \*[Define Package Model] for [Pin Numbers] pins

 RLC model for pins not in [Pin Numbers]

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Notes:

[Pin] (RLC): L\_pin/C\_pin/R\_pin or [Package] L\_pkg/C\_pkg/R\_pkg for any missing L\_pin/C\_pin/R\_pin

\*[Define Package Model]: [Number Of Sections] or [Model Data] formats are available

\*\*Illegal: For POWER and GND pins under the [Pin] keyword, [Merged Pins] requires BOTH [Pin Mapping] and [Pin Numbers] keywords

\*\*\*Illegal: [Merged Pins] is illegal for Signal Pins, NC pins and CIRCUITCALL pins under [Pin]

\*\*\*\*Illegal: [Pin Mapping] is also illegal with CIRCUITCALL pins under [Pin]

**ANY OTHER BACKGROUND INFORMATION:**

This issue was discussed in a series of emails with Randy Wolff and Aniello Viscardi of Micron Technology, Inc. during the weeks of March, 2015. In addition, an extensive email conversation took place with Bob Ross and Radek Biernacki in the month of April, 2015 on the details of the rules and various test cases. The topic was also discussed in the March 31, April 7, and May 5, 2015 Advanced Technology Modeling Task Group Teleconferences. The proposal presented in this BIRD is based on all these discussions.

On pg. 137 add a new line to the table for the new proposed [Merged Pins] keyword as follows:

Table 1 – Package Modeling Keywords

| **Keyword** | **Notes** |
| --- | --- |
| [Define Package Model] | Required if the [Package Model] keyword is used |
| [Manufacturer] | (note 1) |
| [OEM] | (note 1) |
| [Description] | (note 1) |
| [Number Of Sections] | (note 2) |
| [Number Of Pins] | (note 1) |
| [Pin Numbers] | (note 1) |
| [Merged Pins] | Optional when [Model Data] is used, otherwise illegal |
| [Model Data] | (note 2) |
| [Resistance Matrix] | Optional when [Model Data] is used |
| [Inductance Matrix] | (note 3) |
| [Capacitance Matrix] | (note 3) |
| [Bandwidth] | Required (for Banded\_matrix matrices only) |
| [Row] | (note 3) |
| [End Model Data] | (note 2) |
| [End Package Model] | (note 1) |
| Note 1 Required when the [Define Package Model] keyword is usedNote 2 Either the [Number Of Sections] or the [Model Data]/[End Model Data] keywords are required. Note that [Number of Sections] and the [Model Data]/[End Model Data] keywords are mutually exclusive.Note 3 Required when the [Define Package Model] keyword is used and the [Number Of Sections] keyword is not used. |

On pg. 140 change the following paragraph under the [Pin Numbers] keyword:

*Usage Rules:* Following the [Pin Numbers] keyword, the names of the pins are listed. There must be as many names listed as there are pins (as given by the preceding [Number Of Pins] keyword). Pin names cannot exceed 5 characters in length. The first pin name given is the “lowest” pin, and the last pin given is the “highest.” If the [Number Of Sections] keyword is used then each pin name must be followed by one or more of the legal subparameter combinations listed below. If the [Number Of Sections] keyword is not present then subparameter usage is NOT allowed.

to:

*Usage Rules:* Following the [Pin Numbers] keyword, the names of the pins are listed. There must be as many names listed as the number of pins given by the preceding [Number Of Pins] keyword, but it is not required to include all of the pins listed under the [Pin] keyword. Pin names cannot exceed 5 characters in length. The first pin name given is the “lowest” pin, and the last pin given is the “highest.” If the [Number Of Sections] keyword is used then each pin name must be followed by one or more of the legal subparameter combinations listed below. If the [Number Of Sections] keyword is not present then subparameter usage is NOT allowed.

If a [Component] references a [Define Package Model] with the [Package Model] or an [Alternate Package Models] keyword, the EDA tool is expected to simulate the package parasitics of the pins in the component's [Pin] keyword that are not listed in the [Pin Numbers] keyword according to the hierarchy rules stated under the [Package] keyword.

However, if power/ground buses are defined by the [Pin Mapping] keyword of a component, the following rules apply to the power/ground pins. If the name of one or more power/ground pin from the power/ground bus defined by the [Pin Mapping] keyword appears under the [Pin Numbers] keyword, then the model data of those pins which are members of the same bus but are not listed under the [Pin Numbers] keyword are assumed to be merged into the model data of the pin(s) which are listed. Consequently, pins which are not listed under the [Pin Numbers] keyword shall NOT be simulated with their corresponding RLC values from the [Pin] or the [Package] keywords. Instead, all unlisted pins whose corresponding pads are members of the bus defined by the [Pin Mapping] keyword shall be shorted to the first pin of the same bus that is listed under the [Pin Numbers] keyword. This mechanism supports merged power/ground pin package modeling without additional keywords. Since the [Merged Pins] keyword (defined below) provides a mechanism to explicitly and unambiguously define the connectivity of merged pins with greater detail and freedom, the use of the [Merged Pins] keyword is strongly recommended for new models in which merged pin modeling exists.

If none of the power/ground pins of a bus defined in the [Pin Mapping] keyword appears under the [Pin Numbers] keyword, the EDA tool is expected to use the RLC values from the [Pin] or [Package] keywords according to the hierarchy rules stated under the [Package] keyword.

On pg. 142 add a new keyword description before the [Model Data] keyword as follows:

*Keyword:* [Merged Pins]

*Required:* Optional when [Model Data] is used, otherwise illegal

*Description:* When the [Pin Mapping] keyword defines power/ground buses that span over multiple power/ground pins (i.e., pads), the package parasitics of one or more groups of power/ground pins may be merged into one or more single pin representations. The [Merged Pins] keyword declares the package model for the pin whose name follows the [Merged Pin] keyword as a merged package model and lists the names of the pins whose package parasitics have been merged into this merged package model.

*Usage Rules:* This keyword may optionally be used when the [Model Data] keyword is present in the [Define Package Model] section. When used, it must be placed after the end of the pin list defined by the [Pin Numbers] keyword and before the [Model Data] keyword. The keyword must be followed by one pin name (the merging pin) on the same line on which the keyword appears, separated by at least one white space. This pin name must be listed under the [Pin Numbers] keyword, it must be listed as a POWER or GND pin under the [Pin] keyword and it must also be a member of a power or ground bus defined by the [Pin Mapping] keyword. This is the pin whose package model contains the merged package model data for a group of power or ground pins.

The line on which the [Merged Pins] keyword appears must be followed by a new line providing a list of one or more pin names (the merged pins), which are separated by at least one white space. The list may be on a single line or span multiple lines and is terminated by either another [Merged Pins] keyword or the [Model Data] keyword.

Each pin name in the list of merged pins must match the name of a POWER or GND pin in the [Pin] keyword and must also be a member of the same power or ground bus as the merging pin (pin name that follows the [Merged Pins] keyword). Pin names in this list must not be present in the pin list under the [Pin Numbers] keyword. The list must include the names of all those pins which are to be connected to the merging pin that follows the [Merged Pins] keyword due to merged modeling. No pin name may appear more than once under all [Merged Pins] keywords.

The EDA tool shall connect all of the pins (not die pads) named in the [Merged Pins] keyword together with an ideal short. It will connect other pins according to the usage rules of the [Pin Numbers] keyword.

*Other Notes:* Note that power integrity (PI) analysis including the package parasitics on power and ground nets is not possible with Components which do not contain power/ground bus definitions using the [Pin Mapping] keyword together with the [Define Package Model] keyword, because key pieces of information on how power is distributed between the power and ground pins and the power terminals of buffer [Model]s are not available for the EDA tool. For PI analysis, at least one power/ground pin should be included in [Pin Numbers] from each power/ground bus defined in [Pin Mapping] for a given signal pin’s buffer. If no power/ground pins are defined, ideal power/ground connections based on the [Voltage Range] and/or the [\* Reference] keywords can be assumed. However, there is insufficient information for PI analysis.

*Example:*

[Manufacturer] ACME, Inc.

[OEM] ACME, Inc.

[Description] FBGA Package Model for x4 Data Pins and POWER/GND

[Number of Pins] 13

[Pin Numbers]

A1 |VDD

A2 |VSSQ

A8 |VSSQ

A9 |VSS

B2 |VDDQ

B3 |DQS\_c

B7 |DQ1

C2 |DQ0

C3 |DQS\_t

C7 |VDD

D3 |DQ2

D7 |DQ3

D9 |VSSQ

[Merged Pins] A1

H1 M1 | Merged VDD

[Merged Pins] C7

F9 J9 N9 | Merged VDD (electrically in parallel with A1, shorted at the die)

[Merged Pins] A9

C8 E9 G1 H9 K1 K9 N1 | Merged VSS

[Merged Pins] A2

D1 | Merged VSSQ (electrically in parallel with A8 and D9, shorted at the die)

[Merged Pins] B2

B8 C1 C9 E2 E8 | Merged VDDQ