**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER: BIRD 145.3**

**ISSUE TITLE:** *Cascading IBIS I/O buffers with [External Circuit]s using the [Model Call] keyword*

**REQUESTOR:**  *Taranjit Kukal, Ambrish Varma, Cadence Design Systems, Inc. Arpad Muranyi, Mentor Graphics.*

**DATE SUBMITTED:** September 19, 2011

**DATE REVISED:** November 10, 2011; May 21, 2013

**DATE ACCEPTED:** Rejected July 20, 2018

**STATEMENT OF THE ISSUE:**

The current [External Circuit] and [Circuit Call] usage rules do not allow the direct interconnection and instantiation of existing IBIS I/O models with [External Circuit] blocks. Based on that, in order for a model developer to use an IBIS I/O model in an [External Circuit] the following steps need to

be followed:

1) Develop SPICE-like wrappers in which the corresponding typ, min, and max IBIS I/O subcircuits are instantiated

2) Develop an [External Circuit] to point to the wrapper subcircuits

3) Use the [Circuit Call] keyword to call the [External Circuit]

It is obvious that the previous usage rules are cumbersome especially when the developer could just directly call the desired IBIS I/O model without the need to develop a SPICE-like wrapper as well as an [External Circuit] section. In this BIRD, we propose the syntax to directly cascade an IBIS I/O model with an [External Circuit] using the new [Model Call] keyword.

**ANALYSIS PATH/DATA THAT LED TO SPECIFICATION:**

The proposed approach in this BIRD came from commercial on-die terminations (ODT) and on-die RDL parasitics modeling efforts where new functionality was needed to meet customer expectations for model functionality, accuracy and performance.

The approach and keywords in this BIRD are defined by Cadence and its semiconductor partners to make the SPICE-IBIS model development process easier.

**ANY OTHER BACKGROUND INFORMATION:**

BIRD 145 was originally titled:

Instantiation of IBIS I/O buffers in an [External Circuit] using the [Model Call] keyword

This BIRD is being requested by the following IBIS users and model developers, in conjunction with the authors:

IBM: Adge Hawes, Kent Dramstad

We introduce the new [Model Call] and [End Model Call] keywords to directly instantiate and connect regular IBIS buffer [Model]s with [External Circuit]s.

At the end of the [Circuit Call] section (i.e., at the end of page 121 in the IBIS 5.1 specification) add the following lines:

*Keyword:* **[Model Call], [End Model Call]**

*Required:* No

*Description:* This keyword is used to instantiate IBIS buffer [Model]s to connect their reserved ports to the ports of an [External Circuit] by connecting them to the same node declared by the [Node Declarations] keyword.

*Sub-Params:* Signal\_pin, Diff\_signal\_pins, Series\_pins, Port\_map

*Usage Rules:* The [Model Call] keyword must be followed by the name of a [Model] that exists in the same [Component]. When a [Model] is called in an IBIS file, then there is NO need to associate it with an [External Circuit] section. As in this case the EDA tool should model the buffer "as usual" based on its existing I-V and V-T tables as well as its subparameters, which can be found in the called [Model].

A [Model Call] keyword should always define connections that involve one or more nodes declared by the [Node Declarations] keyword. If the involved [Circuit Call] keywords define any connections that involve one or more die pads (and consequently pins), the corresponding pins on the [Pin] list must use the reserved word "CIRCUITCALL" in the third column instead of a model name.

Multiple [Model Call] keywords may appear under a [Component] using the same [Model] name, if multiple instantiations of an IBIS buffer [Model] are needed.

Signal\_pin:

Signal\_pin is used when the referenced [Model] has a single analog signal port (I/O) connection to one pin through [External Circuit]. The subparameter is followed by a pin name that must match one of the pin names under the [Pin] keyword.

Diff\_signal\_pins:

Diff\_signal\_pins is used when the referenced [Model] (e.g., [External Model] inside [Model]) describes a true differential model which has two analog signal port (I/O) connections, each to a separate pin through [External Circuit]. The subparameter is followed by two pin names, each of which must match one of the pin names under the [Pin] keyword. The first and second pin names correspond to the non-inverting and inverting signals of the differential model, respectively.

The two pin names must not be identical.

Series\_pins:

Series\_pins is used when the referenced [Model] describes a Series or Series\_switch model which has two analog signal port (I/O) connections to two pins through [External Circuit]. The subparameter is followed by two pin names, each of which must match one of the pin names under the [Pin] keyword. The first and second pin names correspond to the positive and negative ports of the Series or Series\_switch model, respectively. However, the polarity order matters only when the model is polarity sensitive (as with the [Series Current] keyword). The two pin names must not be identical.

Port\_map:

The Port\_map subparameter is used to connect the reserved ports of an IBIS buffer [Model] to the ports of an [External Circuit] by connecting them to the same node declared by the [Node Declarations] keyword.

Every occurrence of the Port\_map subparameter must begin on a new line and must be followed by two arguments, the first being a port name, and the second being a node name declared by the [Node Declarations] keyword.

The first argument of Port\_map must contain a port name that matches one of the reserved port names of an IBIS [Model]. These reserved ports are defined in the table below.

Port Name Description

========= ==========================

1 D\_drive Digital input to a model unit

2 D\_enable Digital enable for a model unit

3 D\_receive Digital receive port of a model unit

4 A\_puref Voltage reference port for pullup structure

5 A\_pcref Voltage reference port for power clamp structure

6 A\_pdref Voltage reference port for pulldown structure

7 A\_gcref Voltage reference port for ground clamp structure

8 A\_signal I/O signal port for a model unit

9 A\_extref External reference voltage port

10 D\_switch Digital input for control of a series switch model

11 A\_gnd Global reference voltage port

12 A\_pos Non-inverting port for series or series switch models

13 A\_neg Inverting port for series or series switch models

14 A\_signal\_pos Non-inverting port of a differential model

15 A\_signal\_neg Inverting port of a differential model

The first letter of the port name designates it as either digital ("D") or analog ("A"). Reserved ports 1 through 15 listed above are assumed or implied under the native IBIS [Model] keyword.

Under the [Model] description, power and ground reference ports are defined and connected by IBIS-compliant tools as defined by the [Power Clamp Reference], [GND Clamp Reference], [Pullup Reference], [Pulldown Reference] and/or [Voltage Range] keywords. The A\_signal port is connected to an [External Circuit] node, to drive or receive an analog signal.

The pre-defined voltage reference ports (i.e., A\_pcref, A\_puref, A\_pdref, A\_gcref) of any [Model] that is called in the circuit can be either: a) manually interconnected by the model developer to the

ports of an [External Circuit] by connecting them to the same node declared by the [Node Declarations] keyword as shown in example 1 below (i.e., in this case the model developer needs to guarantee that the [External Circuit] contains the appropriate circuitry to deliver the required power to each of the voltage reference ports), or b) automatically interconnected "as usual" by the EDA tool to the corresponding voltage sources when those ports are left floating as shown in example 2 below (i.e., in this case the EDA tool should connect the reserved voltage reference ports to DC voltage sources with voltage values equal to the corresponding reference voltage values in the [Model]).

No port name may be listed more than once within a [Model Call] statement. Only those reserved port names need to be listed with the Port\_map subparameter which are connected to an [External Circuit] port by connecting them to the same node declared by the [Node Declarations] keyword

The second argument of the Port\_map subparameter contains the name of a node declared by the [Node Declarations] keyword. The node name may appear multiple times as Port\_map subparameter arguments within the same [Model Call] statement to signify a common connection between multiple ports, such as common voltage supply.

*Examples:*

The following two examples demonstrate how the proposed [Model Call] keyword could be used to directly instantiate and connect regular IBIS I/O buffers with [External Circuit]s. Both examples are based on the [Pin] section in page 17 in the IBIS 5.1 specification, which is modified below to indicate that pins 5 and 9 are each referenced in a [Circuit Call] section.

|-------------------------------------------------------------------------------

[Pin] signal\_name model\_name R\_pin L\_pin C\_pin

|

1 RAS0# Buffer1 200.0m 5.0nH 2.0pF

2 RAS1# Buffer2 209.0m NA 2.5pF

3 EN1# Input1 NA 6.3nH NA

4 A0 3-state

5 D0 CIRCUITCALL

6 RD# Input2 310.0m 3.0nH 2.0pF

7 WR# Input2

8 A1 I/O2

9 D1 CIRCUITCALL

10 GND GND 297.0m 6.7nH 3.4pF

11 RDY# Input2

12 GND GND 270.0m 5.3nH 4.0pF

| .

| .

| .

18 Vcc3 POWER

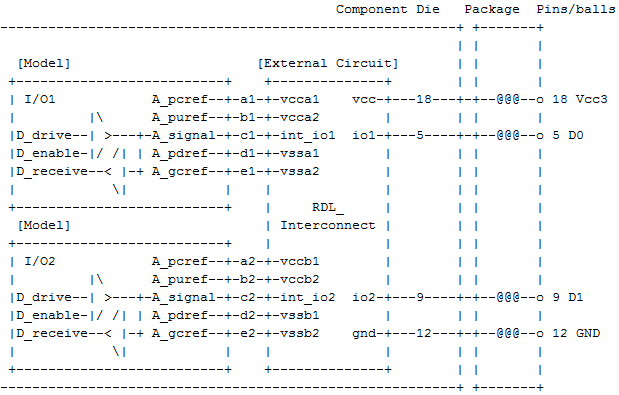
19 NC NC

20 Vcc5 POWER 226.0m NA 1.0pF

21 BAD1 Series\_switch1 | Illegal assignment

22 BAD2 Series\_selector1 | Illegal assignment

*Example 1:* *I/O [Model] with an RDL [External Circuit]*



|

[Node Declarations] | Must appear before any [Circuit Call] or

| | [Model Call] keyword

|

| Die nodes:

a1 b1 c1 d1 e1 | List of die nodes

a2 b2 c2 d2 e2

|

[End Node Declarations]

|

| NOTE:

| A [Model] named "I/O1" must be present in the IBIS file in order to enable

| the tool to instantiate and connect the called model "as usual" based on

| the I-V and V-T curves as well as the subparameters under the corresponding

| [Model] section.

|

[Model Call] I/O1 | Instantiates [Model] named "I/O1"

|

Signal\_pin 5

|

| mapping port node

|

Port\_map A\_pcref a1 | Port to internal node connection

Port\_map A\_puref b1 | Port to internal node connection

Port\_map A\_signal c1 | Port to internal node connection

Port\_map A\_pdref d1 | Port to internal node connection

Port\_map A\_gcref e1 | Port to internal node connection

|

[End Model Call]

|

| NOTE:

| A [Model] named "I/O2" must be present in the IBIS file in order to enable

| the tool to instantiate and connect the called model "as usual" based on

| the I-V and V-T curves as well as the subparameters under the corresponding

| [Model] section.

|

[Model Call] I/O2 | Instantiates [Model] named "I/O2"

|

Signal\_pin 9

|

| mapping port node

|

Port\_map A\_pcref a2 | Port to internal node connection

Port\_map A\_puref b2 | Port to internal node connection

Port\_map A\_signal c2 | Port to internal node connection

Port\_map A\_pdref d2 | Port to internal node connection

Port\_map A\_gcref e2 | Port to internal node connection

|

[End Model Call]

|

[Circuit Call] RDL\_Interconnect | Instantiates [External Circuit] named

| "RDL\_Interconnect"

|

| mapping port pad/node

|

Port\_map vcc 18 | Port to implicit pad connection

Port\_map gnd 12 | Port to implicit pad connection

Port\_map io1 5 | Port to implicit pad connection

Port\_map io2 9 | Port to implicit pad connection

Port\_map vcca1 a1 | Port to internal node connection

Port\_map vcca2 b1 | Port to internal node connection

Port\_map int\_io1 c1 | Port to internal node connection

Port\_map vssa1 d1 | Port to internal node connection

Port\_map vssa2 e1 | Port to internal node connection

Port\_map vccb1 a2 | Port to internal node connection

Port\_map vccb2 b2 | Port to internal node connection

Port\_map int\_io2 c2 | Port to internal node connection

Port\_map vssb1 d2 | Port to internal node connection

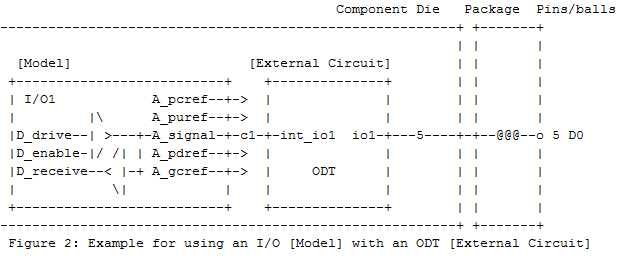
Port\_map vssb2 e2 | Port to internal node connection

|

[End Circuit Call]

|

*Example 2:* *I/O [Model] with an ODT [External Circuit]*



| NOTE 1:

| A [Model] named "I/O1" must be present in the IBIS file in order to enable

| the tool to instantiate and connect the called model above based on the

|\* I-V and V-T curves as well as the subparameters of the corresponding [Model].

|

| NOTE 2:

| The voltage reference ports of [Model] I/O1 above are not connected in

| this circuit. Therefore, the tool has to automatically connect them to the

| corresponding voltage sources similarly to any other IBIS models.

|

[Node Declarations] | Must appear before any [Circuit Call] or

| | [Model Call] keyword

|

| Die nodes:

c1 | List of die nodes

|

[End Node Declarations]

|

[Model Call] I/O1 | Instantiates [Model] named "I/O1"

|

Signal\_pin 5

|

| mapping port node

|

Port\_map A\_signal c1 | Port to internal node connection

|

[End Model Call]

|

[Circuit Call] ODT | Instantiates [External Circuit] named "ODT"

|

|

| mapping port pad/node

|

Port\_map io1 5 | Port to implicit pad connection

Port\_map int\_io1 c1 | Port to internal node connection

|

[End Circuit Call]

|