**TOUCHSTONE ISSUE RESOLUTION DOCUMENT (TSIRD)**

**TSIRD NUMBER: (**Y\_draft\_11)

**ISSUE TITLE:** Standardized Port Mapping

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**DATE SUBMITTED:** {for administrative use}

**DATE REVISED:** {for administrative use}

**DATE ACCEPTED:** {for administrative use}

**DEFINITION OF THE ISSUE:**

When using Touchstone models, it is essential to know how their ports should be connected in a design. This implies that the “port ordering” or “port mapping” information must be supplied along with or inside the Touchstone file. Currently, this is information is sometimes provided in a separate file, but increasingly more often it is included in the Touchstone file as a commented “header” section.

When a Touchstone file contains many ports, connecting its ports manually becomes a tedious and error-prone job. Consequently automation is highly desired. EDA vendors developed several different formats throughout the years, but the problem is that they are all different with various degrees of features and capabilities, making it difficult to parse them with software. Additionally, in most cases this information is provided as a commented header section in the Touchstone file, and strictly speaking, comments are non-parsable, arbitrary text.

The goal of this proposal is to provide a standardized port mapping format for Touchstone files so that all relevant information could be included in it, and all EDA tools could parse them reliably.

**SOLUTION REQUIREMENTS:**

Port Mapping data must be able to support:

1. Reliably, hooking up a Touchstone File in a simulation.
2. Automate creating a schematic symbol.
3. Automate generating/verifying [Interconnect Model]s in .ibs files.
4. Automate generating/verifying [EMD Model]s in .emd files.
5. Automate generating/verifying [C Comp Model]s in .ibs files.
6. Enable Touchstone File viewers to generate mixed-mode S-parameters for differential ports.
7. Sij Status (Measured | Simulated | TBD | Placeholder)
8. Automatic generation of test probe locations for test equipment.
9. Swathing
10. Ability to add new user defined parameters

The Touchstone specification must meet these requirements:

Table 1: Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| 1. Define two new keywords | [Begin Port Map] / [End Port Map] |
|  |  |
|  |  |
|  |  |

**SUMMARY OF PROPOSED CHANGES:**

For review purposes, the proposed changes are summarized as follows:

Table 2: Touchstone Keywords Affected

|  |  |  |
| --- | --- | --- |
| Specification Item | New/Modified/Other | Notes |
|  |  |  |

**PROPOSED CHANGES:**

**Add the following keywords to the Touchstone specification in the appropriate location:**

*Keyword:* **[Begin Port Map] / [End Port Map]**

*Required:* Optional; illegal prior to Version 3.0.

*Description:* Identifies and associates physical, schematic, and optionally measurement locations with the port numbers specified in a Touchstone file

*Sub-Params:* IBIS\_file, EMD\_file, C\_comp\_model\_file, Ts4file, Source, Swathing, Group, Symbol\_leftside, Symbol\_topside, Symbol\_rightside, Symbol\_bottomside, UD, Units, Port

*Usage rules:* If present in the file, the [Begin Port Map] / [End Port Map] keyword pair shall immediately follow the [Number of Ports] keyword and its associated data. Each subparameter shall start on a new line.

The following optional subparameters identify what the Touchstone file port map is describing; only one of these subparameters is permitted per [Begin Port Map]/[End Port Map] keyword pair.

The **IBIS\_file** subparameter is optional. It is followed by an IBIS file name and component. If present, this Touchstone file represents an [Interconnect Model] that is present in the named IBIS file.

The **EMD\_file** subparameter is optional. It is followed by an EMD file name. If present, this Touchstone file represents an [EMD Model] that is present in the named EMD file.

The **C\_comp\_model\_file** subparameter is optional. It is followed by a C Comp Model file name. If present, this Touchstone file represents an IBIS C Comp Model that is present in named model file.

The **Ts4file** subparameter is optional. It is followed by an IBIS

The **Source** subparameter is optional. It is followed by a file name identifying the original file where the Touchstone data was obtained or derived. The file name may be an ODB++ board data base, a schematic file, a simulation model, or any other data file. As the subparameter is purely informational, the data file is not required to be present on the computer system containing the associated Touchstone file.

The **Swathing** subparameter is optional. It is followed by a string, defining a Schema name. There are several ways that connector companies create Touchstone files for a slice (e.g., 3 wafers of a connector) of a connector that can be combined algorithmically to create a virtual Touchstone file that represents all the pins of the connector. Separately, both Reserved Schemas, and other, model-maker-defined Schema values will be supported.

The **Group** subparameter is optional. Group may appear multiple times for a [Begin Port Map]/[End Port Map] pair, with each Group subparameter appearing on a separate line. These lines are placed after the last Port subparameter (see below) and the [End Port Map] keyword. The Group subparameter is followed by a white space and the name of the Group whose port is described by the line. This Group <name> is followed by a white space, a “(“, followed by a list of Physical names, and terminated by a “)”. Any Physical port names (see below) cannot be used as Group names. An EOL (end of line character) without a “)” will continue the list of Physical names on the next line.

The **Symbol\_leftside** subparameter is optional. These lines are placed after the last Port subparameter and the [End Port Map] keyword. The Symbol\_left subparameter string is followed by a list of Port numbers that can be terminals on the left side of a schematic symbol ordered top to bottom.

The **Symbol\_rightside** subparameter is optional. These lines are placed after the last Port Subparameter and the [End Port Map] keyword. The Symbol\_right subparameter string is followed by a list of Port numbers that can be terminals on the right side of a schematic symbol ordered top to bottom.

The **Symbol\_topside** subparameter is optional. These lines are placed after the last Port Subparameter and the [End Port Map] keyword. The Symbol\_top subparameter string is followed by a list of Port numbers that can be terminals on the top side of a schematic symbol ordered left to right.

The **Symbol\_bottomside** subparameter is optional. These lines are placed after the last Port Subparameter and the [End Port Map] keyword. The Symbol\_bottomside subparameter string is followed by a list of Port numbers that can be terminals on the bottom side of a schematic symbol ordered left to right.

If any Symbol\_leftside, Symbol\_rightside, Symbol\_topside or Symbol\_bottomside subparameters are present then any Port number shall appear once and only once in these subparameters.

The **Units** subparameter is optional. The “Units” string shall be followed by a string declaring the units for physical coordinates. The only permitted arguments are: “mm”, “inches”, “mils”, “A”.

The UD (for user-defined) subparameter is optional.

For UD data on Port lines, the UD string shall be followed by the colon character and a name-value string pair within the same pair of parentheses. After the Port declarations, UD data shall be declared using lines, where an arbitrary number of strings may follow the “UD:” string. These subparameters are effectively ignored by the parser and EDA tools, but may be used by recipients to track whether physical measurements have been conducted on a Port, and/or how the Port data was measured.

Examples:

UD:SijStatus 1 5 Measured

(UD:Probe\_Angle 15)

The **Port** subparameter is required. The [Begin Port Map] keyword shall be followed by as many Port subparameter lines as the number of ports defined by the [Number of Ports] keyword. The entire content of each Port subparameter shall be on a single line.

The Port subparameter is followed by a white space and an integer number, indicating which port is described by the line. Note that the Port number shall be larger than zero and shall be smaller than or equal to the Number of Ports entry in the same Touchstone file. The integer port number is followed by a white space, then (<name> <value>) pairs enclosed in parentheses. Unless otherwise noted, all Port subparameter pairs are optional. Subparameter names are case-sensitive.

Several names are reserved and shall not be used as values or arguments to Port subparameters. These are listed below:

Diff\_Port

Logical

Net

Physical

Reference

Side

The Port subparameter and its value shall appear first, at the beginning of each line. All other name/value pairs may appear in any order thereafter.

Examples:

Port 1 (Physical U7.1)

Port 2 (Physical U7.3) (Logical DQ5+) (Diff\_Port 3)

Port 3 (Physical U7.4) (Logical DQ5-) (Diff\_Port 2)

**Port Subparameter Name Rules**

**Type**: The value is either S or P. S stands for Signal, P stands for Power (in other words, rail). If not specified, the Type default is S.

**Physical**: The value is a string that describes the physical location of the terminal used to generate the Port network data. This can be a pin on a component, a set of coordinates identifying the location of a probe, or a sheet and node location for a schematic. The string should clearly indicate to a human where, for instance, the probe used to measure the S-parameter data is placed, or how to connect to the described network element in a circuit simulator. For a printed circuit board (PCB), the argument to “Physical” should either be a reference designator (also called a “refdes”), followed by a dot and a pin number (e.g., U7.3), or an X,Y,Layer, with each coordinate value separated by the colon (“:”) character. X and Y values shall be numeric (floating point) values. Layer may be a numeric (floating point) value, a non-negative integer, or a string without whitespace. There are special rules that can be followed to automatically connect the element described by the Touchstone network data in IBIS and EMD [Interconnect Model]s and in IBIS [C\_comp\_Model]s. If the value is provided in the Bus\_Label:<name> format, then <name> shall be either defined in the IBIS or EMD file, or defined in the Bus\_Labels subparameter section.

Allowed Physical names for C Comp Models:

Buffer\_I/O

Buffer\_I

Pullup\_ref

Pulldown\_ref

Power\_clamp\_ref

Gnd\_clamp\_ref

Ext\_ref

A\_gnd

Rules for [EMD Model]s:

For Type S Ports, the Physical name shall be either the EMD Pin\_name or a designator.pin\_name

For Type P Ports, the Physical name shall be either the EMD Pin\_name, a designator.pin\_name, a Bus\_Label.name or Group.name

Rules for IBIS [Interconnect Model]s:

For Type S Ports, the Physical name shall be either pin.<pin\_name>, pad.<pin\_name> or buf.<pin\_name>

For Type P Ports, the Physical name shall be either pin.pin\_name, pad.pin\_name The list of Bus\_Label pins can be determined from the associated .ibs file. Rail connections to the buffer shall be in one of the following formats:

Pullup\_ref.<pin\_name>

Pulldown\_ref.pin\_name

Power\_clamp\_ref.pin\_name

Gnd\_clamp\_ref.pin\_name

Pullup\_ref.Bus\_label:<name>

Pulldown\_ref. Bus\_label:<name>

Power\_clamp\_ref. Bus\_label:<name>

Gnd\_clamp\_ref. Bus\_label:<name>

Pullup\_ref.Group:<name>

Pulldown\_ref.Group:<name>

Power\_clamp\_ref. Group:<name>

Gnd\_clamp\_ref. Group:<name>

Ext\_ref

A\_gnd

**Logical**: The Logical value identifies a grouping of ports to be used in a schematic symbol for the Touchstone file.

**Net**: The Net value identifies a grouping for generation of simulation or schematic topologies. All ports that have the same Net value are part of the same signal path (this does not mean they share the same node, as in a short).

**Side**: The Side value identifies a grouping, for connecting elements described by Touchstone network data in larger structures across multiple components. A Touchstone-described interconnect file often has two sides (e.g., a connector between a mainboard and daughterboard). A memory DQ route may have a Controller Side, and separate Sides for each memory device connected to that route. A cable assembly for a car may have four Sides (e.g., CPU, Brake, Engine, and Camera).

**Diff\_Port:** The Diff\_Port value identifies the given Port as one-half of a differential pair, and states the Port number of the complementary port. Polarity is not directly indicated, since this will be established by how the port is used by the differential models in simulation. Each port declared as a Diff\_port shall have a corresponding (complementary) Diff\_port declaration.

**Reference**: The Reference value identifies the physical location of the reference terminals used for probing (measurement). If more than one reference is needed, the value shall be in the format Bus\_Label:<Bus\_Label name> or Group:<Group name>.

Need examples of non-Port subparameters

Example 1: 4 pin cable from CPU to Sensor.

[Begin Port Map]

Port 1 (Physical A.1) (Side CPU) (Net 1)

Port 2 (Physical A.2) (Side CPU) (Net 2)

Port 3 (Physical A.3) (Side CPU) (Net 3)

Port 4 (Physical A.4) (Side CPU) (Net 4)

Port 5 (Physical B.1) (Side Sensor) (Net 1)

Port 6 (Physical B.2) (Side Sensor) (Net 2)

Port 7 (Physical B.3) (Side Sensor) (Net 3)

Port 8 (Physical B.4) (Side Sensor) (Net 4)

Symbol\_left 1 2 3 4

Symbol\_right 5 6 7 8

(Add Short Cuts e.g., NFNF, NNFF, Gonzalez, Bogatin, IEEE)

[End Port Map]

Example 2: Transistor

[Begin Port Map]

Port 1 (Logical Emitter)

Port 2 (Logical Base)

Port 3 (Logical Collector)

Symbol\_left 1

Symbol\_right 3

Symbol\_bottom 2

[End Port Map]

Example 3: A 8” coplanar wave guide. (probe has 3 connections: 1 signal and 2 references)

| colon is separator below; location with arbitrary strings?

| Group & Reference separately?

[Begin Port Map]

Port 1 (Physical 0.0:0.0:Top) (Side Left) (Net 1)(Reference 0.0:0.1:Top)

Port 2 (Physical 8.0:0.0:Top) (Side Right) (Net 1)(Reference Group:GND\_R)

Port 1 (Physical 0.0:0.0:Top) (Side Left) (Net 1)(Reference Group:GND\_L)

Port 2 (Physical 8.0:0.0:Top) (Side Right) (Net 1) (Reference Group:GND\_R)

Group GND\_L (0.0:0.1:Top 0.0:-0.1:Top)

Group GND\_R (8.0:0.1:Top 8.0:-0.1:Top)

[End Port Map]

Example 4: Single ended IBIS package model between pin and pad on pin 7.

[Begin Port Map]

Port 1 (Physical pin.7)(Side Pin)(Net 7)(Logical DQ3pin) (Reference pin.8)

Port 2 (Physical pad.7)(Side Pad)(Net 7)(Logical DQ3pad)

[End Port Map]

Example 5: Single ended IBIS package model between pin and buffer on pin 7, including VDD voltage port.

[Begin Port Map]

Port 1 (Physical pin.7) (Type S) (Side Pin) (Net 7) (Logical DQ3pin)

| Type S is redundant, as this is the default

Port 2 (Physical buffer.7) (Type S) (Side buffer) (Net 7) (Logical DQ3buffer)

| Type S is redundant, as this is the default

Port 3 (Physical Pin.Bus\_label:VDD) (Type P) (Side Pin) (Net VDD) (Logical VDDpin)

Port 4 (Physical Pullup\_ref.7) (Type P) (Side Buffer) (Net VDD) (Logical VDDbuffer)

[End Port Map]

Example 6: Single-ended connection between U1.7 and U3.5 for a PCB.

[Begin Port Map]

Port 1 (Physical U1.7) (Side U1) (Net DQ3) (Logical CPU)

Port 2 (Physical U3.5) (Side U3) (Net DQ3) (Logical SDRAM)

[End Port Map]

Example 7: EMD of a 4 bit DQ nibble in a 2 rank DIMM

[Begin Port Map]

Port 1 (Physical 20) (Side EMD) (Net DQ0) (Logical DQ0)

Port 2 (Physical 21) (Side EMD) (Net DQ1) (Logical DQ1)

Port 3 (Physical 22) (Side EMD) (Net DQ2) (Logical DQ2)

Port 4 (Physical 23) (Side EMD) (Net DQ3) (Logical DQ3)

Port 5 (Physical 25) (Side EMD) (Net DQS+) (Logical DQS+) (Diff\_port 6)

Port 6 (Physical 26) (Side EMD) (Net DQS-) (Logical DQS-) (Diff\_port 5)

Port 7 (Physical 27) (Side mem1) (Net DQ0) (Logical mem1\_DQ0)

Port 8 (Physical 28) (Side mem1) (Net DQ1) (Logical mem1\_DQ1)

Port 9 (Physical 29) (Side mem1) (Net DQ2) (Logical mem1\_DQ2)

Port 10 (Physical 30) (Side mem1) (Net DQ3) (Logical mem1\_DQ3)

Port 11 (Physical 31) (Side mem1) (Net DQS+) (Logical mem1\_DQS+) (Diff\_port 12)

Port 12 (Physical 32) (Side mem1) (Net DQS-) (Logical mem1\_DQS-) (Diff\_port 11)

Port 13 (Physical 33) (Side mem2) (Net DQ0) (Logical mem2\_DQ0)

Port 14 (Physical 34) (Side mem2) (Net DQ1) (Logical mem2\_DQ1)

Port 15 (Physical 35) (Side mem2) (Net DQ2) (Logical mem2\_DQ2)

Port 16 (Physical 36) (Side mem2) (Net DQ3) (Logical mem2\_DQ3)

Port 17 (Physical 37) (Side mem2) (Net DQS+) (Logical mem2\_DQS+) (Diff\_port 18)

Port 18 (Physical 38) (Side mem2) (Net DQS-) (Logical mem2\_DQS-) (Diff\_port 17)

[End Port Map]

Example 8: 4 pin cable from CPU to Sensor.

[Begin Port Map]

Port 1 (Physical A.1) (Side CPU) (Net 1)

Port 2 (Physical A.2) (Side CPU) (Net 2)

Port 3 (Physical A.3) (Side CPU) (Net 3)

Port 4 (Physical A.4) (Side CPU) (Net 4)

Port 5 (Physical B.1) (Side Sensor) (Net 1)

Port 6 (Physical B.2) (Side Sensor) (Net 2)

Port 7 (Physical B.3) (Side Sensor) (Net 3)

Port 8 (Physical B.4) (Side Sensor) (Net 4)

Symbol\_left 1 2 3 4

Symbol\_right 5 6 7 8

Units mm

UD:SijStatus 1 5 Measured

[End Port Map]

Example 9: 4 pin cable from CPU to Sensor

[Begin Port Map]

Port 1 (Physical A.1) (Side CPU) (Net 1)

Port 2 (Physical A.2) (Side CPU) (Net 2)

Port 3 (Physical A.3) (Side CPU) (Net 3)

Port 4 (Physical A.4) (Side CPU) (Net 4)

Port 5 (Physical B.1) (Side Sensor) (Net 1)

Port 6 (Physical B.2) (Side Sensor) (Net 2)

Port 7 (Physical B.3) (Side Sensor) (Net 3)

Port 8 (Physical B.4) (Side Sensor) (Net 4)

IBIS\_file my\_ibis\_file.ibs my\_component

[End Port Map]

Examples 10+ to include at least EMD\_file, C\_comp\_model\_file, Ts4file, Source, Swathing

**Examples from the HL proposal, formatted according to the syntax in this proposal.**

#1) An EMD-like model example with “per interface” referencing using **Group** (currently not supported by the EMD specification because only one reference connection is allowed for all ports):

[Begin Port Map]

Port 1 (Type S)(Physical U1.94)(Side Die1) (Net A0)(Reference Group:GND\_U1)

Port 2 (Type S)(Physical U2.94)(Side Die2) (Net A0)(Reference Group:GND\_U2)

Port 3 (Type S)(Physical U3.94)(Side Die3) (Net A0)(Reference Group:GND\_U3)

Port 4 (Type S)(Physical K2) (Side EMDpin)(Net A0)(Reference Group:GND\_BGA)

…

Port 7 (Type S)(Physical U1.95)(Side Die1) (Net A1)(Reference Group:GND\_U1)

Port 8 (Type S)(Physical U2.95)(Side Die2) (Net A1)(Reference Group:GND\_U2)

Port 9 (Type S)(Physical U3.95)(Side Die3) (Net A1)(Reference Group:GND\_U3)

Port 10 (Type S)(Physical J2) (Side EMDpin)(Net A1)(Reference Group:GND\_BGA)

…

Port 121 (Type S)(Physical U1.71)(Side Die1) (Net CLK\_c)(Reference Group:GND\_U1) (Diff\_port 123)

Port 122 (Type S)(Physical E2) (Side EMDpin)(Net CLK\_c)(Reference Group:GND\_BGA)(Diff\_port 124)

Port 123 (Type S)(Physical U3.70)(Side Die1) (Net CLK\_t)(Reference Group:GND\_U1) (Diff\_port 121)

Port 124 (Type S)(Physical D2) (Side EMDpin)(Net CLK\_t)(Reference Group:GND\_BGA)(Diff\_port 122)

…

Port 163 (Type P)(Physical Group:VDD\_U1) (Side Die1) (Net VDD)(Reference Group:GND\_U1)

Port 164 (Type P)(Physical Group:VDD\_U2) (Side Die2) (Net VDD)(Reference Group:GND\_U2)

Port 165 (Type P)(Physical Group:VDD\_U3) (Side Die3) (Net VDD)(Reference Group:GND\_U3)

Port 166 (Type P)(Physical Group:VDD\_BGA)(Side EMDpin)(Net VDD)(Reference Group:GND\_BGA)

…

Group VDD\_U1 (U1.4 U1.8 U1.17 U1.20 U1.33 U1.36 U1.40 U1.45 U1.49 U1.52 ...)

Group VDD\_U2 (U2.4 U2.8 U2.17 U2.20 U2.33 U2.36 U2.40 U2.45 U2.49 U2.52 ...)

Group VDD\_U3 (U3.4 U3.8 U3.17 U3.20 U3.33 U3.36 U3.40 U3.45 U3.49 U3.52 ...)

Group VDD\_BGA (BGA.A3 BGA.A4 BGA.A7 BGA.AB5 BGA.AB9 BGA.AB11 BGA.AB13 BGA.AC7 BGA.B1 BGA.B5...)

…

Group GND\_U1 (U1.2 U1.11 U1.15 U1.23 U1.38 U1.42 U1.43 U1.47 U1.50 U1.54 ...)

Group GND\_U2 (U2.2 U2.11 U2.15 U2.23 U2.38 U2.42 U2.43 U2.47 U2.50 U2.54 ...)

Group GND\_U3 (U3.2 U3.11 U3.15 U3.23 U3.38 U3.42 U3.43 U3.47 U3.50 U3.54 ...)

Group GND\_BGA (BGA.A5 BGA.A9 BGA.A11 BGA.A14 BGA.AA5 BGA.AA13 BGA.AC5 BGA.AC9 BGA.AC11 BGA.AC14...)

[End Port Map]

#2) An EMD-like model example with one reference at all Designator pins and another at EMD pins using **Group with RefDes wildcards** (currently not supported by the EMD specification because only one reference connection is allowed for all ports):

[Begin Port Map]

Port 1 (Type S)(Physical U1.94)(Side Die1) (Net A0)(Reference Group:GND\_Ux)

Port 2 (Type S)(Physical U2.94)(Side Die2) (Net A0)(Reference Group:GND\_Ux)

Port 3 (Type S)(Physical U3.94)(Side Die3) (Net A0)(Reference Group:GND\_Ux)

Port 4 (Type S)(Physical K2) (Side EMDpin)(Net A0)(Reference Group:GND\_BGA)

…

Port 7 (Type S)(Physical U1.95)(Side Die1) (Net A1)(Reference Group:GND\_Ux)

Port 8 (Type S)(Physical U2.95)(Side Die2) (Net A1)(Reference Group:GND\_Ux)

Port 9 (Type S)(Physical U3.95)(Side Die3) (Net A1)(Reference Group:GND\_Ux)

Port 10 (Type S)(Physical J2) (Side EMDpin)(Net A1)(Reference Group:GND\_BGA)

…

Port 121 (Type S)(Physical U1.71)(Side Die1) (Net CLK\_c)(Reference Group:GND\_Ux) (Diff\_port 123)

Port 122 (Type S)(Physical E2) (Side EMDpin)(Net CLK\_c)(Reference Group:GND\_BGA)(Diff\_port 124)

Port 123 (Type S)(Physical U3.70)(Side Die1) (Net CLK\_t)(Reference Group:GND\_Ux) (Diff\_port 121)

Port 124 (Type S)(Physical D2) (Side EMDpin)(Net CLK\_t)(Reference Group:GND\_BGA)(Diff\_port 122)

…

Port 163 (Type P)(Physical Group:VDD\_U1) (Side Die1) (Net VDD)(Reference Group:GND\_Ux)

Port 164 (Type P)(Physical Group:VDD\_U2) (Side Die2) (Net VDD)(Reference Group:GND\_Ux)

Port 165 (Type P)(Physical Group:VDD\_U3) (Side Die3) (Net VDD)(Reference Group:GND\_Ux)

Port 166 (Type P)(Physical Group:VDD\_BGA)(Side EMDpin)(Net VDD)(Reference Group:GND\_BGA)

…

Group VDD\_U1 (U1.4 U1.8 U1.17 U1.20 U1.33 U1.36 U1.40 U1.45 U1.49 U1.52 ...)

Group VDD\_U2 (U2.4 U2.8 U2.17 U2.20 U2.33 U2.36 U2.40 U2.45 U2.49 U2.52 ...)

Group VDD\_U3 (U3.4 U3.8 U3.17 U3.20 U3.33 U3.36 U3.40 U3.45 U3.49 U3.52 ...)

Group VDD\_BGA (BGA.A3 BGA.A4 BGA.A7 BGA.AB5 BGA.AB9 BGA.AB11 BGA.AB13 BGA.AC7 BGA.B1 BGA.B5...)

…

Group GND\_Ux (\*.2 \*.11 \*.15 \*.23 \*.38 \*.42 \*.43 \*.47 \*.50 \*.54 ...)

Group GND\_BGA (BGA.A5 BGA.A9 BGA.A11 BGA.A14 BGA.AA5 BGA.AA13 BGA.AC5 BGA.AC9 BGA.AC11 BGA.AC14...)

[End Port Map]

#3) An EMD-like model example with “per interface” referencing using **EMD rail signal names** (currently not supported by the EMD specification because only one reference connection is allowed for all ports):

[Begin Port Map]

Port 1 (Type S)(Physical U1.94)(Side Die1) (Net A0)(Reference U1.GND)

Port 2 (Type S)(Physical U2.94)(Side Die2) (Net A0)(Reference U2.GND)

Port 3 (Type S)(Physical U3.94)(Side Die3) (Net A0)(Reference U3.GND)

Port 4 (Type S)(Physical K2) (Side EMDpin)(Net A0)(Reference GND)

…

Port 7 (Type S)(Physical U1.95)(Side Die1) (Net A1)(Reference U1.GND)

Port 8 (Type S)(Physical U2.95)(Side Die2) (Net A1)(Reference U2.GND)

Port 9 (Type S)(Physical U3.95)(Side Die3) (Net A1)(Reference U3.GND)

Port 10 (Type S)(Physical J2) (Side EMDpin)(Net A1)(Reference GND)

…

Port 121 (Type S)(Physical U1.71)(Side Die1) (Net CLK\_c)(Reference U1.GND)(Diff\_port 123)

Port 122 (Type S)(Physical E2) (Side EMDpin)(Net CLK\_c)(Reference GND) (Diff\_port 124)

Port 123 (Type S)(Physical U3.70)(Side Die1) (Net CLK\_t)(Reference U1.GND)(Diff\_port 121)

Port 124 (Type S)(Physical D2) (Side EMDpin)(Net CLK\_t)(Reference GND) (Diff\_port 122)

…

Port 163 (Type P)(Physical U1.VDD)(Side Die1) (Net VDD)(Reference U1.GND)

Port 164 (Type P)(Physical U2.VDD)(Side Die2) (Net VDD)(Reference U2.GND)

Port 165 (Type P)(Physical U3.VDD)(Side Die3) (Net VDD)(Reference U3.GND)

Port 166 (Type P)(Physical VDD) (Side EMDpin)(Net VDD)(Reference GND)

[End Port Map]

#4) An EMD-like model example with one reference at all Designator pins and another at EMD pins using **EMD rail signal names with RefDes wildcards** (currently not supported by the EMD specification because only one reference connection is allowed for all ports):

[Begin Port Map]

Port 1 (Type S)(Physical U1.94)(Side Die1) (Net A0)(Reference \*.GND)

Port 2 (Type S)(Physical U2.94)(Side Die2) (Net A0)(Reference \*.GND)

Port 3 (Type S)(Physical U3.94)(Side Die3) (Net A0)(Reference \*.GND)

Port 4 (Type S)(Physical K2) (Side EMDpin)(Net A0)(Reference GND)

…

Port 7 (Type S)(Physical U1.95)(Side Die1) (Net A1)(Reference \*.GND)

Port 8 (Type S)(Physical U2.95)(Side Die2) (Net A1)(Reference \*.GND)

Port 9 (Type S)(Physical U3.95)(Side Die3) (Net A1)(Reference \*.GND)

Port 10 (Type S)(Physical J2) (Side EMDpin)(Net A1)(Reference GND)

…

Port 121 (Type S)(Physical U1.71)(Side Die1) (Net CLK\_c)(Reference \*.GND)(Diff\_port 123)

Port 122 (Type S)(Physical E2) (Side EMDpin)(Net CLK\_c)(Reference GND) (Diff\_port 124)

Port 123 (Type S)(Physical U3.70)(Side Die1) (Net CLK\_t)(Reference \*.GND)(Diff\_port 121)

Port 124 (Type S)(Physical D2) (Side EMDpin)(Net CLK\_t)(Reference GND) (Diff\_port 122)

…

Port 163 (Type P)(Physical U1.VDD)(Side Die1) (Net VDD)(Reference \*.GND)

Port 164 (Type P)(Physical U2.VDD)(Side Die2) (Net VDD)(Reference \*.GND)

Port 165 (Type P)(Physical U3.VDD)(Side Die3) (Net VDD)(Reference \*.GND)

Port 166 (Type P)(Physical VDD) (Side EMDpin)(Net VDD)(Reference GND)

[End Port Map]

#5) An EMD model example with a single reference for all ports using **EMD rail signal names** (This is currently the only referencing method supported by the EMD specification. While legal in EMD files, **it leaves the Designator ground pins floating!**):

[Begin Port Map]

Port 1 (Type S)(Physical U1.94)(Side Die1) (Net A0)(Reference GND)

Port 2 (Type S)(Physical U2.94)(Side Die2) (Net A0)(Reference GND)

Port 3 (Type S)(Physical U3.94)(Side Die3) (Net A0)(Reference GND)

Port 4 (Type S)(Physical K2) (Side EMDpin)(Net A0)(Reference GND)

…

Port 7 (Type S)(Physical U1.95)(Side Die1) (Net A1)(Reference GND)

Port 8 (Type S)(Physical U2.95)(Side Die2) (Net A1)(Reference GND)

Port 9 (Type S)(Physical U3.95)(Side Die3) (Net A1)(Reference GND)

Port 10 (Type S)(Physical J2) (Side EMDpin)(Net A1)(Reference GND)

…

Port 121 (Type S)(Physical U1.71)(Side Die1) (Net CLK\_c)(Reference GND)(Diff\_port 123)

Port 122 (Type S)(Physical E2) (Side EMDpin)(Net CLK\_c)(Reference GND)(Diff\_port 124)

Port 123 (Type S)(Physical U3.70)(Side Die1) (Net CLK\_t)(Reference GND)(Diff\_port 121)

Port 124 (Type S)(Physical D2) (Side EMDpin)(Net CLK\_t)(Reference GND)(Diff\_port 122)

…

Port 163 (Type P)(Physical U1.VDD)(Side Die1) (Net VDD)(Reference GND)

Port 164 (Type P)(Physical U2.VDD)(Side Die2) (Net VDD)(Reference GND)

Port 165 (Type P)(Physical U3.VDD)(Side Die3) (Net VDD)(Reference GND)

Port 166 (Type P)(Physical VDD) (Side EMDpin)(Net VDD)(Reference GND)

[End Port Map]

#6) An EMD model example with a single reference for all ports using **A\_gnd** (This is currently the only referencing method supported by the EMD specification. While legal in EMD files, **it doesn’t define any EMD or Designator ground pins, leaving the Designator ground pins floating!**):

[Begin Port Map]

Port 1 (Type S)(Physical U1.94)(Side Die1) (Net A0)(Reference A\_Gnd)

Port 2 (Type S)(Physical U2.94)(Side Die2) (Net A0)(Reference A\_Gnd)

Port 3 (Type S)(Physical U3.94)(Side Die3) (Net A0)(Reference A\_Gnd)

Port 4 (Type S)(Physical K2) (Side EMDpin)(Net A0)(Reference A\_Gnd)

…

Port 7 (Type S)(Physical U1.95)(Side Die1) (Net A1)(Reference A\_Gnd)

Port 8 (Type S)(Physical U2.95)(Side Die2) (Net A1)(Reference A\_Gnd)

Port 9 (Type S)(Physical U3.95)(Side Die3) (Net A1)(Reference A\_Gnd)

Port 10 (Type S)(Physical J2) (Side EMDpin)(Net A1)(Reference A\_Gnd)

…

Port 121 (Type S)(Physical U1.71)(Side Die1) (Net CLK\_c)(Reference A\_Gnd)(Diff\_port 123)

Port 122 (Type S)(Physical E2) (Side EMDpin)(Net CLK\_c)(Reference A\_Gnd)(Diff\_port 124)

Port 123 (Type S)(Physical U3.70)(Side Die1) (Net CLK\_t)(Reference A\_Gnd)(Diff\_port 121)

Port 124 (Type S)(Physical D2) (Side EMDpin)(Net CLK\_t)(Reference A\_Gnd)(Diff\_port 122)

…

Port 163 (Type P)(Physical U1.VDD)(Side Die1) (Net VDD)(Reference A\_Gnd)

Port 164 (Type P)(Physical U2.VDD)(Side Die2) (Net VDD)(Reference A\_Gnd)

Port 165 (Type P)(Physical U3.VDD)(Side Die3) (Net VDD)(Reference A\_Gnd)

Port 166 (Type P)(Physical VDD) (Side EMDpin)(Net VDD)(Reference A\_Gnd)

[End Port Map]

#7) An EMD model example with a single reference for all ports using **A\_gnd** and **additional ports to connect the EMD and Designator ground pins**. (This is legal in EMD files and provides a complete definition for all EMD and Designator ground pins**.)**:

[Begin Port Map]

Port 1 (Type S)(Physical U1.94)(Side Die1) (Net A0)(Reference A\_Gnd)

Port 2 (Type S)(Physical U2.94)(Side Die2) (Net A0)(Reference A\_Gnd)

Port 3 (Type S)(Physical U3.94)(Side Die3) (Net A0)(Reference A\_Gnd)

Port 4 (Type S)(Physical K2) (Side EMDpin)(Net A0)(Reference A\_Gnd)

…

Port 7 (Type S)(Physical U1.95)(Side Die1) (Net A1)(Reference A\_Gnd)

Port 8 (Type S)(Physical U2.95)(Side Die2) (Net A1)(Reference A\_Gnd)

Port 9 (Type S)(Physical U3.95)(Side Die3) (Net A1)(Reference A\_Gnd)

Port 10 (Type S)(Physical J2) (Side EMDpin)(Net A1)(Reference A\_Gnd)

…

Port 121 (Type S)(Physical U1.71)(Side Die1) (Net CLK\_c)(Reference A\_Gnd)(Diff\_port 123)

Port 122 (Type S)(Physical E2) (Side EMDpin)(Net CLK\_c)(Reference A\_Gnd)(Diff\_port 124)

Port 123 (Type S)(Physical U3.70)(Side Die1) (Net CLK\_t)(Reference A\_Gnd)(Diff\_port 121)

Port 124 (Type S)(Physical D2) (Side EMDpin)(Net CLK\_t)(Reference A\_Gnd)(Diff\_port 122)

…

Port 163 (Type P)(Physical U1.VDD)(Side Die1) (Net VDD)(Reference A\_Gnd)

Port 164 (Type P)(Physical U2.VDD)(Side Die2) (Net VDD)(Reference A\_Gnd)

Port 165 (Type P)(Physical U3.VDD)(Side Die3) (Net VDD)(Reference A\_Gnd)

Port 166 (Type P)(Physical VDD) (Side EMDpin)(Net VDD)(Reference A\_Gnd)

…

Port 200 (Type P)(Physical U1.GND)(Side Die1) (Net GND)(Reference A\_Gnd)

Port 201 (Type P)(Physical U2.GND)(Side Die2) (Net GND)(Reference A\_Gnd)

Port 202 (Type P)(Physical U3.GND)(Side Die3) (Net GND)(Reference A\_Gnd)

Port 203 (Type P)(Physical GND) (Side EMDpin)(Net GND)(Reference A\_Gnd)

[End Port Map]

#8) A Package example with pin rail grouping and using **pad names** (the model is between pin and pad):

[Begin Port Map]

Port 1 (Type S)(Physical A7)(Side Pin\_IO) (Net DM\_n)(Reference A\_gnd)

Port 2 (Type S)(Physical A7)(Side Pad\_IO) (Net DM\_n)(Reference A\_gnd)

Port 3 (Type S)(Physical C2)(Side Pin\_IO) (Net DQ0) (Reference A\_gnd)

Port 4 (Type S)(Physical C2)(Side Pad\_IO) (Net DQ0) (Reference A\_gnd)

Port 5 (Type S)(Physical B7)(Side Pin\_IO) (Net DQ1) (Reference A\_gnd)

Port 6 (Type S)(Physical B7)(Side Pad\_IO) (Net DQ1) (Reference A\_gnd)

Port 7 (Type S)(Physical D3)(Side Pin\_IO) (Net DQ2) (Reference A\_gnd)

Port 8 (Type S)(Physical D3)(Side Pad\_IO) (Net DQ2) (Reference A\_gnd)

Port 9 (Type S)(Physical B3)(Side Pin\_IO) (Net DQS\_c)(Reference A\_gnd) (Diff\_port 11)

Port 10 (Type S)(Physical B3)(Side Pad\_IO) (Net DQS\_c)(Reference A\_gnd) (Diff\_port 12)

Port 11 (Type S)(Physical C3)(Side Pin\_IO) (Net DQS\_t)(Reference A\_gnd) (Diff\_port 9)

Port 12 (Type S)(Physical C3)(Side Pad\_IO) (Net DQS\_t)(Reference A\_gnd) (Diff\_port 10)

Port 13 (Type P)(Physical VDDQ) (Side Pin\_Rail)(Net VDDQ)(Reference A\_gnd)

Port 14 (Type P)(Physical VDDQ\_DIE-4) (Side Pad\_Rail)(Net VDDQ)(Reference A\_gnd)

Port 15 (Type P)(Physical VDDQ\_DIE-8) (Side Pad\_Rail)(Net VDDQ)(Reference A\_gnd)

Port 16 (Type P)(Physical VDDQ\_DIE-13)(Side Pad\_Rail)(Net VDDQ)(Reference A\_gnd)

Port 17 (Type P)(Physical VSS) (Side Pin\_Rail)(Net VSS) (Reference A\_gnd)

Port 18 (Type P)(Physical VSS\_DIE-2) (Side Pad\_Rail)(Net VSS) (Reference A\_gnd)

Port 19 (Type P)(Physical VSS\_DIE-6) (Side Pad\_Rail)(Net VSS) (Reference A\_gnd)

Port 20 (Type P)(Physical VSS\_DIE-10) (Side Pad\_Rail)(Net VSS) (Reference A\_gnd)

[End Port Map]

#9) An On-die interconnect example using **pad names and buffer terminals** – without grouping

(the model is between pad and buffer terminals):

[Begin Port Map]

Port 1 (Type S)(Physical A7)(Side Pad\_IO) (Net DM\_n)(Reference A\_gnd)

Port 2 (Type S)(Physical A7)(Side Buf\_IO) (Net DM\_n)(Reference A\_gnd)

Port 3 (Type P)(Physical A7)(Side Buf\_PUref)(Net DM\_n)(Reference A\_gnd)

Port 4 (Type P)(Physical A7)(Side Buf\_PDref)(Net DM\_n)(Reference A\_gnd)

Port 5 (Type S)(Physical C2)(Side Pad\_IO) (Net DQ0) (Reference A\_gnd)

Port 6 (Type S)(Physical C2)(Side Buf\_IO) (Net DQ0) (Reference A\_gnd)

Port 7 (Type P)(Physical C2)(Side Buf\_PUref)(Net DQ0) (Reference A\_gnd)

Port 8 (Type P)(Physical C2)(Side Buf\_PDref)(Net DQ0) (Reference A\_gnd)

Port 9 (Type S)(Physical B7)(Side Pad\_IO) (Net DQ1) (Reference A\_gnd)

Port 10 (Type S)(Physical B7)(Side Buf\_IO) (Net DQ1) (Reference A\_gnd)

Port 11 (Type P)(Physical B7)(Side Buf\_PUref)(Net DQ1) (Reference A\_gnd)

Port 12 (Type P)(Physical B7)(Side Buf\_PDref)(Net DQ1) (Reference A\_gnd)

Port 13 (Type S)(Physical D3)(Side Pad\_IO) (Net DQ2) (Reference A\_gnd)

Port 14 (Type S)(Physical D3)(Side Buf\_IO) (Net DQ2) (Reference A\_gnd)

Port 15 (Type P)(Physical D3)(Side Buf\_PUref)(Net DQ2) (Reference A\_gnd)

Port 16 (Type P)(Physical D3)(Side Buf\_PDref)(Net DQ2) (Reference A\_gnd)

Port 17 (Type S)(Physical B3)(Side Pad\_IO) (Net DQS\_c)(Reference A\_gnd) (Diff\_port 21)

Port 18 (Type S)(Physical B3)(Side Buf\_IO) (Net DQS\_c)(Reference A\_gnd) (Diff\_port 22)

Port 19 (Type P)(Physical B3)(Side Buf\_PUref)(Net DQS\_c)(Reference A\_gnd)

Port 20 (Type P)(Physical B3)(Side Buf\_PDref)(Net DQS\_c)(Reference A\_gnd)

Port 21 (Type S)(Physical C3)(Side Pad\_IO) (Net DQS\_t)(Reference A\_gnd) (Diff\_port 17)

Port 22 (Type S)(Physical C3)(Side Buf\_IO) (Net DQS\_t)(Reference A\_gnd) (Diff\_port 18)

Port 23 (Type P)(Physical C3)(Side Buf\_PUref)(Net DQS\_t)(Reference A\_gnd)

Port 24 (Type P)(Physical C3)(Side Buf\_PDref)(Net DQS\_t)(Reference A\_gnd)

Port 25 (Type P)(Physical VDDQ\_DIE-4) (Side Pad\_Rail)(Net VDDQ)(Reference A\_gnd)

Port 26 (Type P)(Physical VDDQ\_DIE-8) (Side Pad\_Rail)(Net VDDQ)(Reference A\_gnd)

Port 27 (Type P)(Physical VDDQ\_DIE-13)(Side Pad\_Rail)(Net VDDQ)(Reference A\_gnd)

Port 28 (Type P)(Physical VSS\_DIE-2) (Side Pad\_Rail)(Net VSS) (Reference A\_gnd)

Port 29 (Type P)(Physical VSS\_DIE-6) (Side Pad\_Rail)(Net VSS) (Reference A\_gnd)

Port 30 (Type P)(Physical VSS\_DIE-10) (Side Pad\_Rail)(Net VSS) (Reference A\_gnd)

[End Port Map]

**BACKGROUND INFORMATION/HISTORY:**

TBD