#### 4 File Header Information

**Keyword** [IBIS Ver]

## **Required** Yes

## **Description**

Specifies the IBIS template version. This keyword informs electronic parsers of the kinds of data types that are present in the file.

### **Usage Rules**

[IBIS Ver] must be the first keyword in any IBIS file. It is normally on the first line of the file, but can be preceded by comment lines that must begin with a "|".

```
[IBIS Ver] 5.0 | Used for template variations
```

## Keyword [Comment Char]

#### **Required** No

### **Description**

Defines a new comment character to replace the default "|" (pipe) character, if desired.

#### **Usage Rules**

The new comment character to be defined must be followed by the underscore character and the letters "char".

For example:

"Lchar" redundantly redefines the comment character to be the pipe character. The new comment character is in effect only following the [Comment Char] keyword. The following characters MAY be used:

```
! " # $ % & ' ( ) * , : ; < > ? @ \ ^ ` { | } ~
```

#### **Other Notes**

The [Comment Char] keyword can be used anywhere in the file, as desired.

```
[Comment Char] | char
```

### **Keyword** [File Name]

## **Required** Yes

### **Description**

Specifies the name of the IBIS file.

#### **Usage Rules**

The file name must conform to the rules in paragraph 3 of Section 3, General Syntax Rules and Guidelines. In addition, the file name must use the extension ".ibs", ".pkg", or or ".ebd". The file name must be the actual name of the file.

```
[File Name] ver5_0.ibs
```

# **5 Component Description**

### **Keyword** [Component]

## **Required** Yes

#### **Description**

Marks the beginning of the IBIS description of the integrated circuit named after the keyword.

### **Sub-Params**

Si\_location, Timing\_location

### **Usage Rules**

If the .ibs file contains data for more than one component, each section must begin with a new [Component] keyword. The length of the component name must not exceed 40 characters, and blank characters are allowed.

NOTE: Blank characters are not recommended due to usability issues.

Si\_location and Timing\_location are optional and specify where the Signal Integrity and Timing measurements are made for the component. Allowed values for either subparameter are 'Die' or 'Pin'. The default location is at the 'Pin'.

```
[Component] 7403398 MC452
|
Si_location Pin | Optional subparameters to give measurement
Timing_location Die | location positions
```

### **Keyword** [Manufacturer]

#### **Required** Yes

#### **Description**

Specifies the name of the component's manufacturer.

#### **Usage Rules**

The length of the manufacturer's name must not exceed 40 characters (blank characters are allowed, e.g., Texas Instruments). In addition, each manufacturer must use a consistent name in all .ibs files.

```
[Manufacturer] Intel Corp.
```

### **Keyword** [Package]

### **Required** Yes

#### **Description**

Defines a range of values for the default packaging resistance, inductance, and capacitance of the component pins.

#### **Sub-Params**

R\_pkg, L\_pkg, C\_pkg

#### **Usage Rules**

The typical (typ) column must be specified. If data for the other columns are not available, they must be noted with "NA".

page 2 IBIS Version 5.0

#### **Other Notes**

If RLC parameters are available for individual pins, they can be listed in columns 4-6 under keyword [Pin]. The values listed in the [Pin] description section override the default values defined here. Use the [Package Model] keyword for more complex package descriptions. If defined, the [Package Model] data overrides the values in the [Package] keyword. Regardless, the data listed under the [Package] keyword must still contain valid data.

[Package]			
variable	typ	min	max
R_pkg	250.0m	225.0m	275.0m
L_pkg	15.0nH	12.0nH	18.0nH
C_pkg	18.0pF	15.0pF	20.0pF

## Keyword [Pin]

### **Required** Yes

## **Description**

Associates the component's I/O models to its various external pin names and signal names.

IBIS Version 5.0 page 3

#### 6 Model Statement

Keyword [Model]

**Required** Yes

## **Description**

Used to define a model, and its attributes.

#### **Sub-Params**

Model\_type, Polarity, Enable, Vinl, Vinh, C\_comp, C\_comp\_pullup, C\_comp\_pulldown, C\_comp\_power\_clamp, C\_comp\_gnd\_clamp, Vmeas, Cref, Rref, Vref

### **Usage Rules**

Each model type must begin with the keyword [Model]. The model name must match the one that is listed under a [Pin], [Model Selector] or [Series Pin Mapping] keyword and must not contain more than 40 characters. A .ibs file must contain enough [Model] keywords to cover all of the model names specified under the [Pin], [Model Selector] and [Series Pin Mapping] keywords, except for those model names that use reserved words (POWER, GND and NC).

Model\_type must be one of the following:

Input, Output, I/O, 3-state, Open\_drain, I/O\_open\_drain, Open\_sink, I/O\_open\_sink, Open\_source, I/O\_open\_source, Input\_ECL, Output\_ECL, I/O\_ECL, 3-state\_ECL, Terminator, Series, and Series switch.

For true differential models documented under Section 6b, Model\_type must be one of the following:

Input\_diff, Output\_diff, I/O\_diff, and 3-state\_diff

Special usage rules apply to the following. Some definitions are included for clarification:

```
Input, I/O, I/O_open_drain, I/O_open_sink, I/O_open_source
```

These model types must have Vinl and Vinh defined. If they are not defined, the parser issues a warning and the default values of Vinl = 0.8 V and Vinh = 2.0 V are assumed.

```
Input_ECL, I/O_ECL
```

These model types must have Vinl and Vinh defined. If they are not defined, the parser issues a warning and the default values of Vinl = -1.475 V and Vinh = -1.165 V are assumed.

#### **Terminator**

This model type is an input-only model that can have analog loading effects on the circuit being simulated but has no digital logic thresholds. Examples of terminators are: capacitors, termination diodes, and pullup resistors.

```
[bunch of stuff, including a diagram, left out for now. Ed.]

[Model] External_Model_Diff

Model_type I/O_diff | Requires [External Model]

Polarity Non-Inverting
Enable Active-High

| The [Diff Pin] vdiff value overrides the thresholds below
```

page 4 IBIS Version 5.0

Vinl = 0.8V	Input logic "low" DC voltage, if any	
Vinh = 2.0V	Input logic "high" DC voltage, if any	
	The true differential measurement point is at	
	the crossover voltage	
	The Vmeas value is overridden	
Vmeas = 1.5V	Reference voltage for timing measurements	
	Single-ended timing test load is still permitted	
Cref = 5pF	Timing specification test load capacitance value	
Rref = 500	Timing specification test load resistance value	
Vref = 0	Timing specification test load voltage	
	These new subparameters are permitted for	
	single-ended differential operation based on the	
	[Diff Pin] keyword	
Rref_diff = 100	Timing specification differential resistance value	
Cref_diff = 5pF	Timing specification differential capacitance value	

# Keyword [Model Spec]

## **Required** No

# **Sub-Params**

Vinh, Vinl, Vinh+, Vinh-, Vinl+, Vinl-, S\_overshoot\_high, S\_overshoot\_low, D\_overshoot\_high, D\_overshoot\_low, D\_overshoot\_time, D\_overshoot\_area\_h, D\_overshoot\_area\_l, D\_overshoot\_ampl\_h, D\_overshoot\_ampl\_l, Pulse\_high, Pulse\_low, Pulse\_time, Vmeas, Vref, Cref, Rref, Cref\_rising, C\_ref\_falling, Rref\_rising, Rref\_falling, Vref\_rising, Vref\_falling, Vmeas\_rising, Vmeas\_falling, Rref\_diff, Cref\_diff

# **Description**

The [Model Spec] keyword defines four columns under which specification subparameters are defined

IBIS Version 5.0 page 5