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| IBIS_logo | **EPEPS 2017 IBIS Summit Agenda** |
| |  |  | | --- | --- | | IBIS SUMMIT: | October 18, 2017 13:00-18:00 | |  |  | | LOCATION: | DoubleTree by Hilton Hotel 2050 Gateway Place San Jose, California | |  |  | | ROOM: | Monterey | |  |  | | SPONSORS: | IEEE EPEPS Keysight Technologies Synopsys |   **AGENDA (Order and times subject to change)**   |  |  | | --- | --- | | 13:00 | **REFRESHMENTS & SIGN IN** | | 13:10 | **OFFICIAL OPENING**   * Welcome to Summit * Introductions   Bob Ross, Teraspeed Labs | | 13:15 | **Go Big or Go Home: The First Transatlantic Telegraph Cable and the Birth of Electrical Engineering**  Thomas Lee, Stanford University | | 14:00 | **IBIS Update**  Mike LaBonte, SiSoft  [*Presented by Bob Ross, Teraspeed Labs*] | | 14:30 | **IBIS-AMI Modeling Using Scripts and Spice Models**  Wei-hsing Huang, SPISim | | 15:00 | **Equalization for Multi-level Signal** Nana Dikhaminjia, Ilia State University | | 15:30 | **BREAK, REFRESHMENTS (15 Minutes)** | | 15:45 | **Interconnect Modeling Using IBIS-ISS and Touchstone**  Michael Mirmak, Intel Corporation) [*Presented by Bob Ross, Teraspeed Labs*] | | 16:20 | **Interconnect Modeling: New Features for Rail Connections**  Bob Ross, Teraspeed Labs | | 16:50 | **OPEN DISCUSSION and CLOSING REMARKS** | | 16:50 | **CLOSING REMARKS**  Bob Ross, Teraspeed Labs | | 17:30 | **END OF MEETING**  *Next Open Forum Meeting: October 26, 2017* | | |