Asian IBIS Summit (TOKYO)

&

第8回 JEITA IBISセミナー

2019

11/8 金

@秋葉原UDX NEXT1にて 同日開催

東京都千代田区外神田4丁目14-1 秋葉原UDX 4F NEXT1

http://udx.jp/access/

第8回JEITA／IBISセミナー 10：00 スタート【9：30受付開始】

テーマ IBIS What's New!!（IBIS Ver5.0～Ver7.0の最新情報）

招待講演 高精度な回路解析を実現するための受動部品のSPICEモデル 株式会社 村田製作所様

Asian IBIS Summit（TOKYO） 13：00 スタート

テーマ IBISモデルに関する開発状況、今後の展望・課題、事例紹介等

●お申し込み方法および詳細はJEITA ECセンターのホームページ/イベント案内をご覧ください。

http://ec.jeita.or.jp/jp/modules/eguide/event.php?eid=41

一般社団法人 電子情報技術産業協会 ECセンター
Japan Electronics and Information Technology Industries Association EC Center

〒100-0004 東京都千代田区大手町1丁目1番3号 大手センタービル5F TEL：03-5218-1062 FAX：03-5218-1081 URL http://ec.jeita.or.jp/jp/

TABLE OF CONTENTS AND ORDER OF THE PRESENTATIONS

(The actual agenda might be modified)

I B I S   S U M M I T   M E E T I N G   A G E N D A

13:00 **SIGN IN**

TABLE OF CONTENTS AND ORDER OF THE PRESENTATIONS **1**

13:05 **MEETING WELCOMES** **3**
- Randy WOLFF (Chair, IBIS Open Forum) (Micron Technology, USA)
- Satoshi NAKAMIZO (Chair, JEITA EDA Model Specialty Committee) (Keysight Technologies Japan K K)

13:08 **2019 Asian IBIS Summit (TOKYO) Meeting Welcomes** **7**
Satoshi NAKAMIZO (Keysight Technologies Japan K K)

13:08 **Introduction of JEITA EC Center (for reference)** **11**
13:08 **Introduction of JEITA EC Center (Japanese)** **17**
Satoshi NAKAMIZO (Keysight Technologies Japan K K)

13:15 **IBIS Chair's Report** **23**
Randy WOLFF (Micron Technology USA)

13:**30** **Expectations for the New Package Model Specification of IBIS 7.0** **31**
Masaki KIRINAKA, Akiko TASUKADA
(Fujitsu Interconnect Technologies Limited, Japan)
[Presented by Masaki KIRINAKA
(Fujitsu Interconnect Technologies Limited, Japan]]

14:00 **The On Die Decap Modeling Proposal(BIRD198)** **44**
Megumi ONO*, Atsushi TOMISHIMA* (*Socionext Inc.,
**Toshiba Electronic Devices & Storage Corporation; Japan)
*[Presented by Megumi ONO (*Socionext Inc.)]*

14:35 **IBIS File Format Links** **60**
Bob ROSS (Teraspeed Labs, USA)
[Presented by Randy WOLFF (Micron Technology, USA)]

15:00 **BREAK**
- Reconvene at 15:20

TABLE OF CONTENTS AND ORDER OF THE PRESENTATIONS (CONTINUED)

15:20 **How to Obtain Buffer Impedance from IBIS 67**
Lance WANG (Zuken, USA)

15:50 **A Potential Application of IBIS Models to CISPR25 Based EMI Analysis of DCDC Converter 76**
Kazuyuki SAKATA*, Koji ICHIKAWA**, Miyoko GOTO***, Toshiki KANAMOTO****
[Renesas Electronics Corporation*, DENSO CORP.**, Ricoh Corp***, Hirosaki University****; Japan)
[Presented by Kazuyuki SAKATA (Renesas Electronics Corporation, Japan)]

16:10 **IBIS-AMI & COM Co-design for 25G Serdes 90**
Nan HOU#; Amy ZHANG#, Guohua WANG#, David ZHANG##, Anders EKHOLM## (Ericsson, #China, ##Sweden)
[Presented by Anders EKHOLM (Ericsson, Sweden)]

16:50 **CONCLUDING ITEMS**

17:00 **END OF SUMMIT**

WELCOME FROM RANDY WOLFF, IBIS OPEN FORUM

Ladies and Gentlemen,

As chair of the IBIS Open Forum it is my pleasure to welcome you to the 2019 Asian IBIS Summit in Tokyo and to thank you for your presentations and participation. This is our 14th Summit with Japan Electronics and Information Technology Industries Association (JEITA) since 2006. We are grateful to our sponsors JEITA, IBIS Open Forum, ANSYS, Apollo Giken Co., Keysight Technologies, Ricoh, Toshiba Corporation, and Zuken, for making this event possible.

Since 1993, IBIS has provided the digital electronics industry with specifications to make signal, timing, and power integrity analyses much easier and faster. With the introduction of IBIS-AMI in 2008, the IBIS community generated new energy for high speed electronic design. IBIS is now known by engineers worldwide and is a required technology for many applications. IBIS Version 7.0 was released in 2019, adding enhancements for IBIS-AMI and supporting advanced interconnect modeling.

Support for IBIS in Asia has been strong, and the IBIS Open Forum looks forward to continued innovation and contributions from technology companies in Asia.

Thank you!

Randy Wolff
Micron Technology
Chair, IBIS Open Forum

IBIS オープンフォーラムの RANDY WOLFF よりご挨拶

各位

IBIS オープンフォーラムの議長として、東京で開催される 2019 Asian IBIS Summit へのご講演ならびにご出席を歓迎するとともに御礼申し上げます。2006 年以来、日本電子情報技術産業協（JEITA）にご後援頂きながら、14 回目のサミットを開催する事が出来ました。JEITA をはじめ、アンシス・ジャパン、アポロ技研、キーサイト・テクノロジー、リコー、東芝、図研のご協力によって、このサミットが開催出来る事に感謝致します。

1993 年以来、IBIS はデジタルエレクトロニクス業界に信号生成、タイミング、およびパワーインテグリティの解析をより簡単かつ迅速にする為の仕様を提供してきました。2008 年の IBIS-AMI の導入により IBIS は高速デジタル伝送の設計に新しいエネルギーを生み出しました。IBIS は現在、世界中のエンジニアに知られており、多くのアプリケーションに必要な技術です。 2019 年にリリースされた IBIS バージョン 7.0 では IBIS-AMI の機能を拡張したと共に、高度なインターコネクトモデリングにも対応しました。

アジアでは IBIS に対し強力な支援を頂いております。IBIS オープンフォーラムではアジアのテクノロジー企業からの継続的な革新と貢献を期待しています。 ありがとうございます。

Randy Wolff
マイクロン・テクノロジー
IBIS オープンフォーラム 議長

WELCOME FROM JEITA/EC CENTER IBIS SPECIALITY COMMITTEE

Ladies and Gentlemen,

Thank you for joining us at the Asian IBIS Summit (TOKYO) again this year.

Since the establishment of the EDA Standard WG in 2004, and then the IBIS Promoting WG, we are today the EDA Model Specialty Committee. We are very happy to have supported the holding of the Summit by the IBIS Open Forum in Japan for 14 editions.

The EDA Model Specialty Committee works under the JEITA/EC Center for the purpose of improving utilization technologies for the EDA Model, including the IBIS Model, and promoting their distribution. These models and their specifications will be continually revised with the advent of new technologies and will also become more and more complex. Considering this situation, we will work to continue broadly providing information to all users of the EDA Model.

The Summit offers a platform to present information on new IBIS specifications. It is also a platform to discuss and exchange views with the IBIS Open Forum. I hope everyone here today will make the most of this opportunity.

Finally, we are putting out a broad invitation to anyone who is interested in working together with us on committee activities of the EDA Model Specialty Committee. If you are interested in joining the committee, please contact us. We hope to hear from you.

November 8, 2019

JEITA/EC Center

EDA Model Specialty Committee

JEITA/EC センター EDA モデル専門委員会よりご挨拶

各位

今年も Asian IBIS Summit (TOKYO)にご参加頂き、誠にありがとうございます。私共は 2004 年の EDA 標準 WG 発足以降、IBIS 標準 WG を経て現在の EDA モデル専門委員会に至りますが、これまで 14 回に渡って、IBIS Open Forum による日本でのサミットの開催に協力出来た事を大変嬉しく思います。

EDA モデル専門委員会は IBIS モデルを中心とした EDA モデルの活用技術の向上と流通の促進を目的に JEITA/EC センターの下で活動しておりますが、これらのモデルは新しい技術の登場に伴い、その仕様が次々と改訂され、複雑化の一途をたどっている側面もあります。この状況を踏まえ、EDA モデルを使用される皆様に向けて今後も幅広く情報を発信してゆきたいと考えております。

サミットは新しい IBIS の仕様の情報発信の場であると共に、IBIS Open Forum とディスカッション・意見交換が出来る場でもあります。今回ご参加頂きました皆様にはぜひこの機会をご活用頂けますと幸いです。

最後に、EDA モデル専門委員会ではご一緒に委員会活動をして頂ける方を広く募集しております。委員会への参加にご興味をお持ちの方は、ぜひお問い合わせ下さい。

2019 年 11 月 8 日
JEITA/EC センター
EDA モデル専門委員会

2019 Asian IBIS Summit (TOKYO) MEETING WELCOMES

November 8, 2019

Satoshi Nakamizo
mailto:edamodel@keysight.com
EDA Model Specialty Committee
EC Center / JEITA

中溝 哲士
mailto:edamodel@keysight.com
EDAモデル専門委員会
ECセンター / JEITA

1 All Rights Reserved, Copyright © 2019 JEITA ECALGA

About JEITA EDA Model Specialty Committee (EDAモデル専門委員会について)

- EDA Model Specialty Committee started in May 2017.
(2017年5月からEDAモデル専門委員会として発足しました。)

- We work under the JEITA/EC Center for the purpose of improving utilization technologies for the EDA Model, including the IBIS Model, and promoting their distribution.
(IBISモデルを中心としたEDAモデルの活用技術の向上と、流通の促進を目的にJEITA/ECセンターの下で活動しています。)

2 All Rights Reserved, Copyright © 2019 JEITA ECALGA

Current status of the EDA models and our objective (EDAモデルの現状と委員会の活動目標)

- EDA models and their specifications will be continually revised with the advent of new technologies and will also become more and more complex.
  (EDAモデルは新しい技術の登場に伴い、その仕様が次々と改訂され、複雑化の一途をたどっている側面があります。)

- Considering this situation, we will work to continue broadly providing information to all users of the EDA Model.
  (この状況を踏まえ、EDAモデルのユーザに向けて今後も幅広く情報を発信してゆきたいと考えています。)

Device Vendor

Manufacturer

IBIS 3.2?

IBIS 6.0?

SI/PI?

I-V Table?

ISSO?

IBIS-AMI?

3 All Rights Reserved, Copyright © 2019 JEITA

ECALGA

About Asian IBIS Summit (Asian IBIS Summitについて)

- The Summit offers a platform to present information on new IBIS specifications. It is also a platform to discuss and exchange views with the IBIS Open Forum.
  (サミットは新しいIBISの仕様の情報発信の場であると共に、
  IBIS Open Forumとディスカッション・意見交換が出来る場でもあります。)

- We hope everyone here today will make the most of this opportunity.
  (ぜひ、この機会を活用して下さい。)

2019 Asian IBIS Summit (JAPAN) Sponsors

RICOH

TOSHIBA

ZUKEN

4 All Rights Reserved, Copyright © 2019 JEITA

ECALGA

END

Electronic Commerce ALliance for Global business Activity

 All Rights Reserved, Copyright © 2019 JEITA ECALGA

Introduction of JEITA EC Center

Presented by Satoshi Nakamizo, Keysight Technologies
Asian IBIS Summit, Tokyo Japan
November 8, 2019

Japan Electronics and Information Technology Industries Association
EC Center Steering Committee

1 All Rights Reserved, Copyright © 2019 JEITA ECALGA

1. About JEITA
1-1. Overview of JEITA (1/2)

What is JEITA ?
The objective of the Japan Electronics and Information Technology Industries Association (JEITA) is to promote the healthy manufacturing, international trade and consumption of electronics products and components in order to contribute to the overall development of the electronics and information technology (IT) industries, and thereby further Japan's economic development and cultural prosperity.

The world is now connected via the Internet, and electronics technologies and IT have become widespread everywhere. With the evolution of electronics and progress of IT, technologies in information, communications, imaging and audio are converging to create new systems and products, which are bringing enormous changes that go beyond conventional frameworks, not only in our economic society, but also in our lives and culture.

JEITA's mission is to foster a digital network society for the 21st century, in which IT advancement brings fulfillment and a higher quality of life to everyone.

The Association is also actively promoting environmental preservation countermeasures, including those to combat global warming.

About JEITA (https://www.jeita.or.jp/english/about/what/index.htm)

2 All Rights Reserved, Copyright © 2019 JEITA ECALGA

1. About JEITA
1-1. Overview of JEITA (2/2)

What is EC Center ?

The JEITA/EC Center standardizes terms, and the types of information relating to trading, and maintains controls to make it possible electronically to exchange between companies, and to reuse trading information and technical information regarding electronic devices, and semiconductor and electronic components. Also, JEITA and the EC Center are involved in the following that relate to the popularization and promotion of electronic commercial trading.

Overview of Work

1. Study and embody strategic EC issues for the IT and electronics industries
2. Expand and maintain standards for EC-related information
3. Study and expand practical EC applications
4. Implement information exchanges with domestic and international organizations and associations; international collaboration and survey research

ECALGA

The name of the enterprise for attaining those goals, and the name of the standard are either ECALGA, or the ECALGA enterprise.

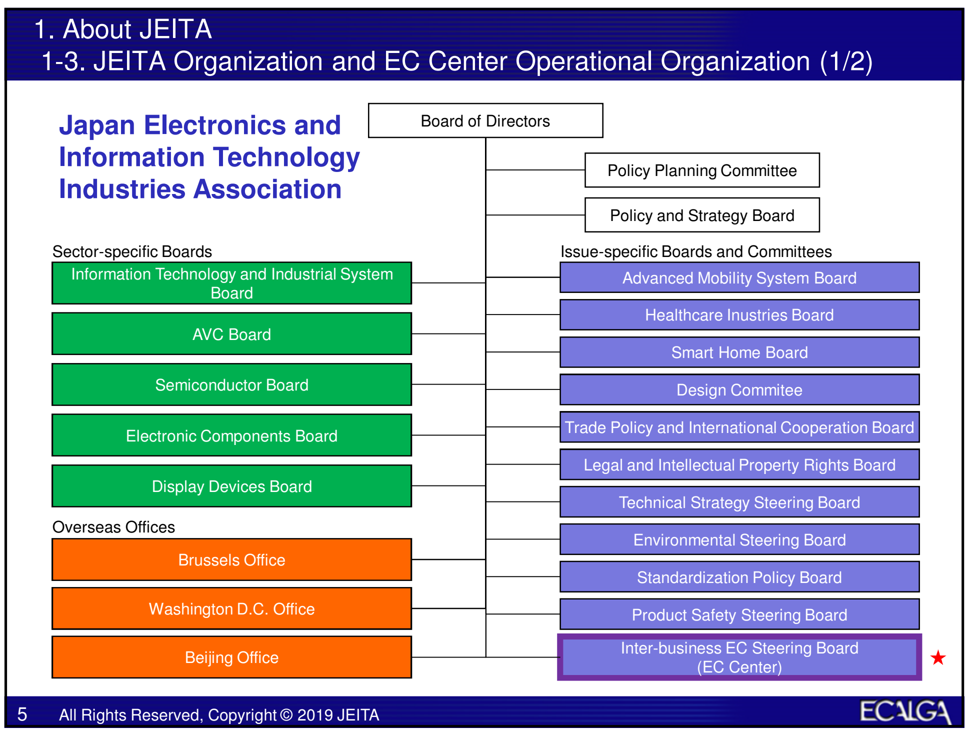
3 All Rights Reserved, Copyright © 2019 JEITA ECALGA

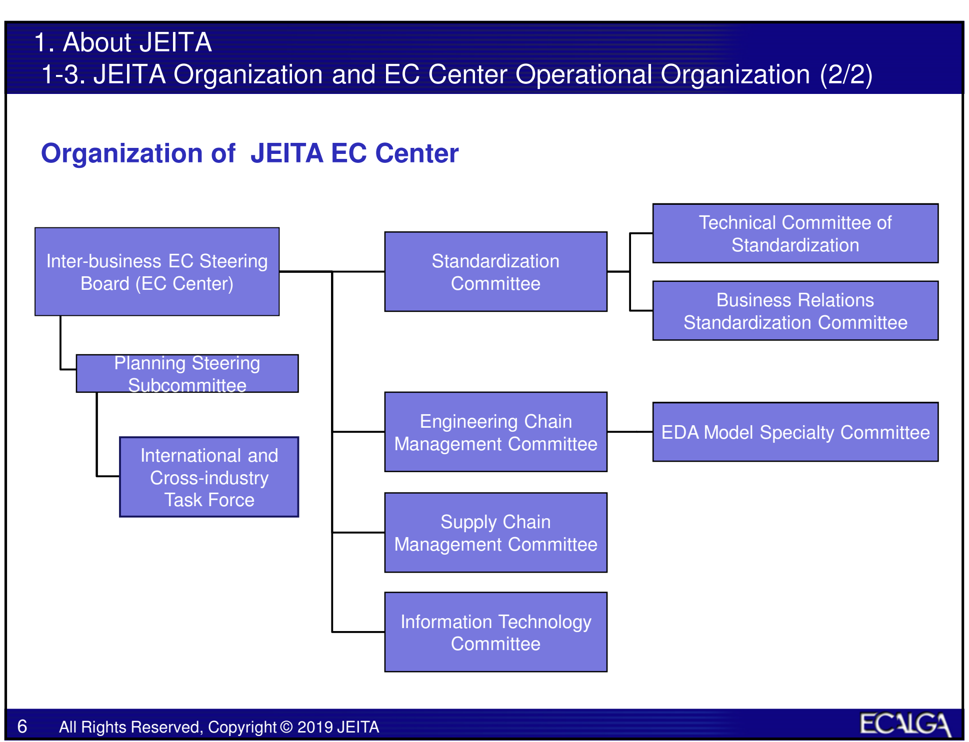
1. About JEITA
1-2. JEITA member Company

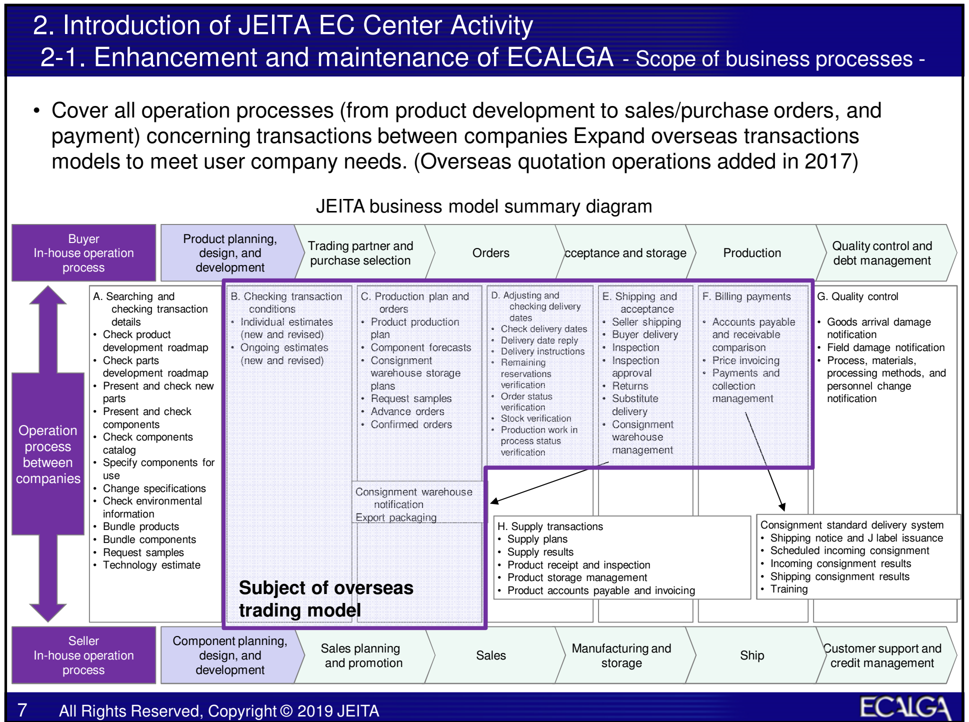
- JEITA member companies:
  - Total 382 (Full member 337, Associate member 45) as of Oct 23, 2019

*JEITA members (https://www.jeita.or.jp/cgi-bin/member/list.cgi?l=en&k=0)

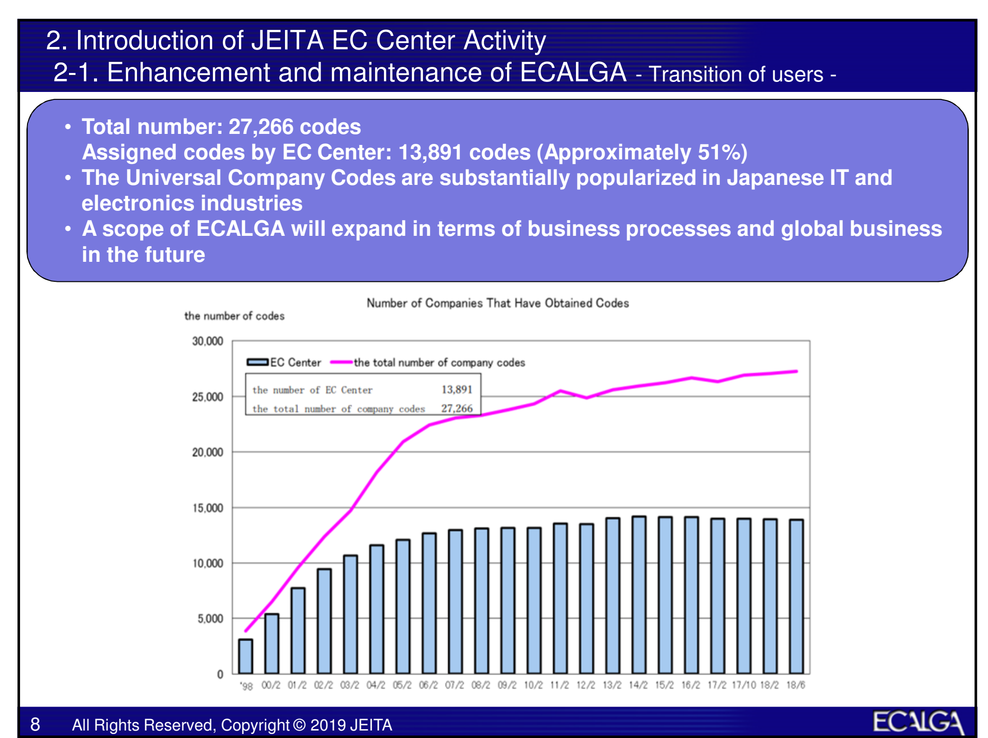
4 All Rights Reserved, Copyright © 2019 JEITA ECALGA


1. About JEITA
1-3. JEITA Organization and EC Center Operational Organization (1/2)
Japan Electronics and Information Technology Industries Association
Board of Directors
Policy Planning Committee
Policy and Strategy Board
Sector-specific Boards
Information Technology and Industrial System Board
AVC Board
Semiconductor Board
Electronic Components Board
Display Devices Board
Overseas Offices
Brussels Office
Washington D.C. Office
Beijing Office
Issue-specific Boards and Committees
Advanced Mobility System Board
Healthcare Inustries Board
Smart Home Board
Design Commitee
Trade Policy and International Cooperation Board
Legal and Intellectual Property Rights Board
Technical Strategy Steering Board
Environmental Steering Board
Standardization Policy Board
Product Safety Steering Board
Inter-business EC Steering Board (EC Center)
5
All Rights Reserved, Copyright © 2019 JEITA
ECALGA


1. About JEITA
1-3. JEITA Organization and EC Center Operational Organization (2/2)
Organization of JEITA EC Center
Inter-business EC Steering Board (EC Center)
Planning Steering Subcommittee
International and Cross-industry Task Force
Standardization Committee
Technical Committee of Standardization
Business Relations Standardization Committee
Engineering Chain Management Committee
EDA Model Specialty Committee
Supply Chain Management Committee
Information Technology Committee
6
All Rights Reserved, Copyright © 2019 JEITA
ECALGA



2. Introduction of JEITA EC Center Activity
2-1. Enhancement and maintenance of ECALGA - Scope of business processes -
• Cover all operation processes (from product development to sales/purchase orders, and payment) concerning transactions between companies Expand overseas transactions models to meet user company needs. (Overseas quotation operations added in 2017)
JEITA business model summary diagram
Buyer In-house operation process
Product planning, design, and development
Trading partner and purchase selection
Orders
cceptance and storage
Production
Quality control and debt management
Operation process between companies
A. Searching and checking transaction details
• Check product development roadmap
• Check parts development roadmap
• Present and check new parts
• Present and check components
• Check components catalog
• Specify components for use
• Change specifications
• Check environmental information
• Bundle products
• Bundle components
• Request samples
• Technology estimate
B. Checking transaction conditions
• Individual estimates (new and revised)
• Ongoing estimates (new and revised)
C. Production plan and orders
• Product production plan
• Component forecasts
• Consignment warehouse storage plans
• Request samples
• Advance orders
• Confirmed orders
D. Adjusting and checking delivery dates
• Check delivery dates
• Delivery date reply
• Delivery instructions
• Remaining reservations verification
• Order status verification
• Stock verification
• Production work in process status verification
E. Shipping and acceptance
• Seller shipping
• Buyer delivery
• Inspection
• Inspection approval
• Returns
• Substitute delivery
• Consignment warehouse management
F. Billing payments
• Accounts payable and receivable comparison
• Price invoicing
• Payments and collection management
G. Quality control
• Goods arrival damage notification
• Field damage notification
• Process, materials, processing methods, and personnel change notification
Consignment warehouse notification
Export packaging
H. Supply transactions
• Supply plans
• Supply results
• Product receipt and inspection
• Product storage management
• Product accounts payable and invoicing
Consignment standard delivery system
• Shipping notice and J label issuance
• Scheduled incoming consignment
• Incoming consignment results
• Shipping consignment results
• Training
Subject of overseas trading model
Seller In-house operation process
Component planning, design, and development
Sales planning and promotion
Sales
Manufacturing and storage
Ship
Customer support and credit management
7 All Rights Reserved, Copyright © 2019 JEITA
ECALGA



2. Introduction of JEITA EC Center Activity
2-1. Enhancement and maintenance of ECALGA - Transition of users -
• Total number: 27,266 codes
Assigned codes by EC Center: 13,891 codes (Approximately 51%)
• The Universal Company Codes are substantially popularized in Japanese IT and electronics industries
• A scope of ECALGA will expand in terms of business processes and global business in the future
Number of Companies That Have Obtained Codes
the number of codes
30,000
25,000
20,000
15,000
10,000
5,000
0
EC Center
the total number of company codes
the number of EC Center 13,891
the total number of company codes 27,266
'98 00/2 01/2 02/2 03/2 04/2 05/2 06/2 07/2 08/2 09/2 10/2 11/2 12/2 13/2 14/2 15/2 16/2 17/2 17/10 18/2 18/6
8 All Rights Reserved, Copyright © 2019 JEITA
ECALGA

2. Introduction of JEITA EC Center Activity
2-2. Cooperating with International standardization organization

- JEITA liaises with international standards bodies and cooperates in establishing international standards.

- IEC
  - IEC61360-4(CDD: Common Data Dictionary) and ECALS dictionary content supply
- eCl@ss
  - For cooperation on the d-m@p PJ (a mapping project for IEC and eCl@ss dictionaries)
- EDIFICE
  - Review and inspection of Electronic Component Package label international standards (IEC 62090)

9 All Rights Reserved, Copyright © 2019 JEITA ECALGA

2. Introduction of JEITA EC Center Activity
2-3. Research and analysis of next generation B2B integration

- Regularly implement surveys on advanced IoT examples and advanced effort examples, to spot the first shoots for the next standardization with coordination between companies.

#	Themes	Survey description
1	FY 2015 technological and industry trends	Survey of global (Germany, USA, China, Japan) IoT trends and technology trends within industries
2	Blockchain technology	Survey blockchain technology, explore use in coordination between companies
3	Industry 4.0 and IoT examples	Survey examples of individual companies in Industry 4.0 and the IoT, centering on the automobile industry
4	FY 2018 technological and industry trends	Update of #1 FY 2015 Technological and Industry Trend Survey

10 All Rights Reserved, Copyright © 2019 JEITA ECALGA

ECALGA
11 All Rights Reserved, Copyright © 2019 JEITA
ECALGA

JEITA ECセンター紹介

Presented by Satoshi Nakamizo, Keysight Technologies
Asian IBIS Summit, Tokyo Japan

2019年11月8日

Japan Electronics and Information Technology Industries Association
ECセンター企画部会

1 All Rights Reserved, Copyright © 2019 JEITA

1. JEITAについて
1-1. JEITA概要 (1/2)

JEITAとは?

JEITAは、電子機器、電子部品の健全な生産、貿易及び消費の増進を図ることにより、電子情報技術産業の総合的な発展に資し、わが国経済の発展と文化の興隆に寄与することを目的とした業界団体です。

現在、世界中がインターネットを介して接続されており、エレクトロニクス技術及びITはあらゆるところに普及しています。エレクトロニクスの進化とITの進歩に伴い、情報・通信・映像・音声の技術が融合し、新たなシステムや製品が生み出され、経済社会だけでなく、我々の生活や文化にまで、従来の枠組みを超えて大きな変化をもたらしています。

JEITAのミッションは、ITの進歩によってあらゆる人々に充実した生活がもたらされる21世紀のデジタルネットワーク社会を育成することです。また、当協会は、地球温暖化対策など、環境保全対策も積極的に推進しています。

About JEITA (https://www.jeita.or.jp/english/about/what/index.htm)

2 All Rights Reserved, Copyright © 2019 JEITA

1. JEITAについて
1-1. JEITA概要 (2/2)

JEITA ECセンターは、電子機器および半導体・電子部品等の商取引情報および技術情報を企業間で電子交換・再活用が可能となるよう、用語・取引に係わる情報の種類・形式を標準化し維持管理を行っています。また、その他電子商取引の普及・促進に関する以下の事業を行っています。

事業内容

1. IT・エレクトロニクス業界におけるEC戦略課題の検討および具体化
2. EC関係情報に関する標準の拡充と維持
3. EC実用化の検討並びに推進
4. 国内外関係機関および団体との情報交流、国際協調および調査研究

ECALGA

以上の目的を達成するための事業の総称および標準の総称をECALGAまたはECALGA事業と称します。

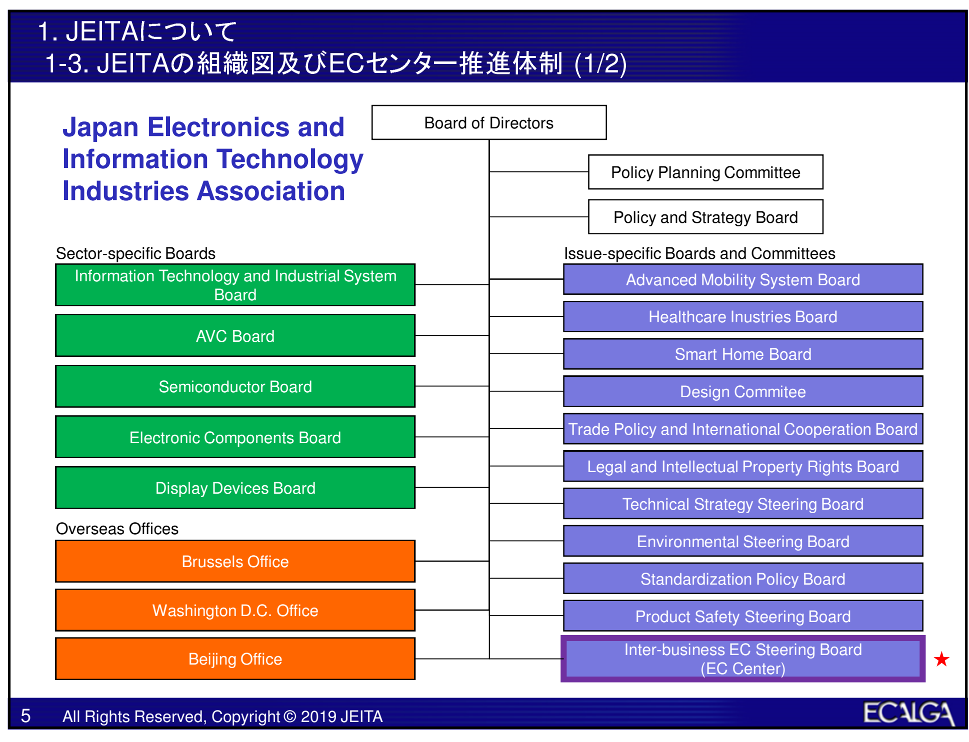
 All Rights Reserved, Copyright © 2019 JEITA ECALGA

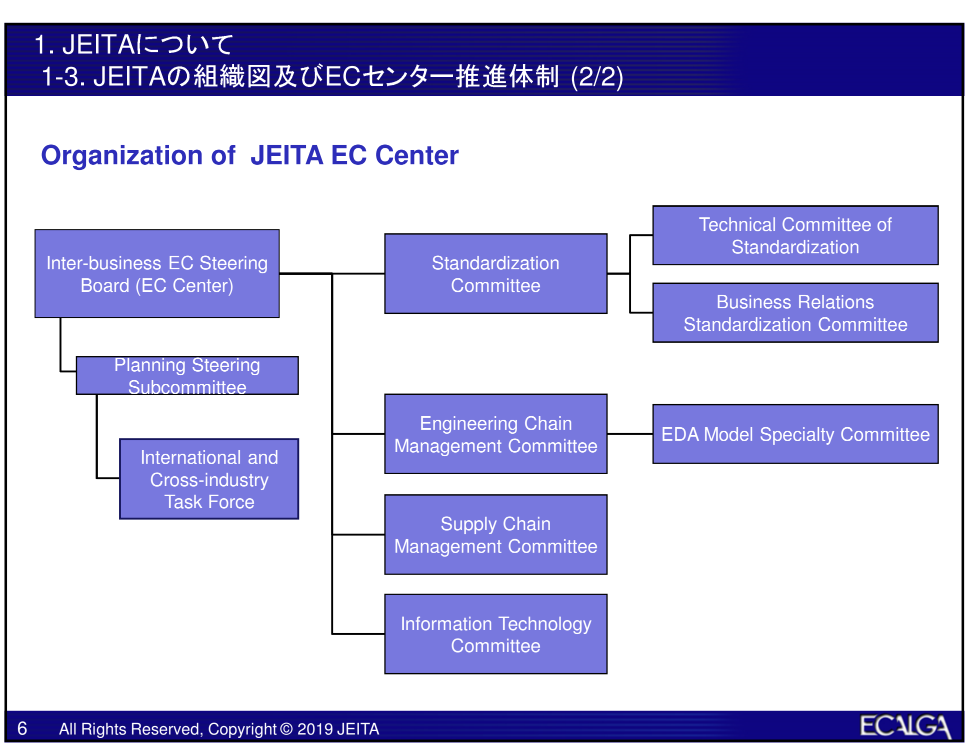
1. JEITAについて
1-2. JEITA会員企業

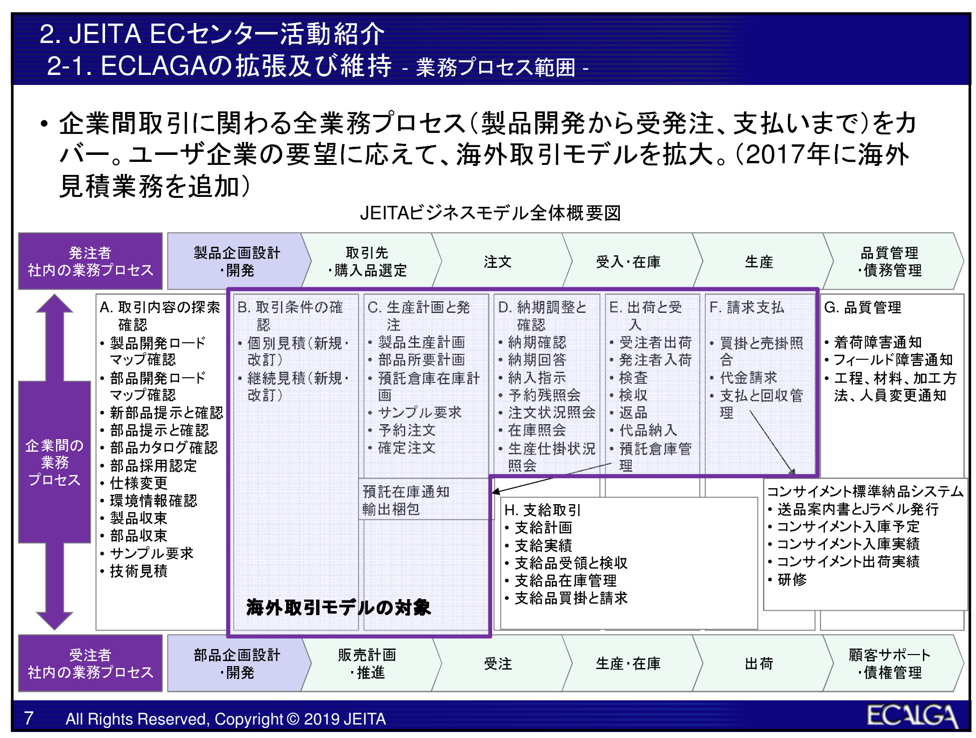
- JEITA会員企業:
  - 合計 382 (正会員 337, 賛助会員 45) 2019年10月23日時点

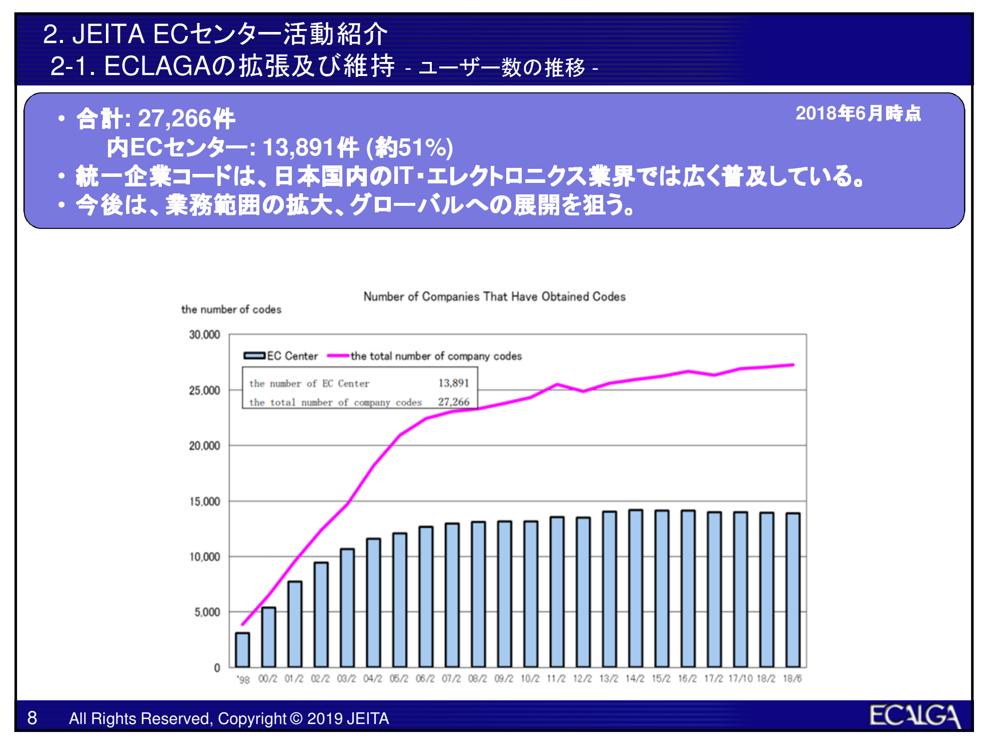
*会員一覧 (https://www.jeita.or.jp/cgi-bin/member/list.cgi)

 All Rights Reserved, Copyright © 2019 JEITA ECALGA


1. JEITAについて
1-3. JEITAの組織図及びECセンター推進体制 (1/2)
Japan Electronics and Information Technology Industries Association
Board of Directors
Policy Planning Committee
Policy and Strategy Board
Sector-specific Boards
Information Technology and Industrial System Board
AVC Board
Semiconductor Board
Electronic Components Board
Display Devices Board
Overseas Offices
Brussels Office
Washington D.C. Office
Beijing Office
Issue-specific Boards and Committees
Advanced Mobility System Board
Healthcare Inustries Board
Smart Home Board
Design Commitee
Trade Policy and International Cooperation Board
Legal and Intellectual Property Rights Board
Technical Strategy Steering Board
Environmental Steering Board
Standardization Policy Board
Product Safety Steering Board
Inter-business EC Steering Board (EC Center)
★
5 All Rights Reserved, Copyright © 2019 JEITA
ECALGA


1. JEITAについて
1-3. JEITAの組織図及びECセンター推進体制 (2/2)
Organization of JEITA EC Center
Inter-business EC Steering Board (EC Center)
Planning Steering Subcommittee
International and Cross-industry Task Force
Standardization Committee
Technical Committee of Standardization
Business Relations Standardization Committee
Engineering Chain Management Committee
EDA Model Specialty Committee
Supply Chain Management Committee
Information Technology Committee
6 All Rights Reserved, Copyright © 2019 JEITA
ECALGA


2. JEITA ECセンター活動紹介
2-1. ECLAGAの拡張及び維持 - 業務プロセス範囲 -
• 企業間取引に関わる全業務プロセス（製品開発から受発注、支払いまで）をカバー。ユーザ企業の要望に応えて、海外取引モデルを拡大。（2017年に海外見積業務を追加）
JEITAビジネスモデル全体概要図
発注者 社内の業務プロセス
製品企画設計 ・開発
取引先 ・購入品選定
注文
受入・在庫
生産
品質管理 ・債務管理
企業間の業務プロセス
A. 取引内容の探索確認
• 製品開発ロードマップ確認
• 部品開発ロードマップ確認
• 新部品提示と確認
• 部品提示と確認
• 部品カタログ確認
• 部品採用認定
• 仕様変更
• 環境情報確認
• 製品収束
• 部品収束
• サンプル要求
• 技術見積
B. 取引条件の確認
• 個別見積（新規・改訂）
• 継続見積（新規・改訂）
C. 生産計画と発注
• 製品生産計画
• 部品所要計画
• 預託倉庫在庫計画
• サンプル要求
• 予約注文
• 確定注文
D. 納期調整と確認
• 納期確認
• 納期回答
• 納入指示
• 予約残照会
• 注文状況照会
• 在庫照会
• 生産仕掛状況照会
E. 出荷と受入
• 受注者出荷
• 発注者入荷
• 検査
• 検収
• 返品
• 代品納入
• 預託倉庫管理
F. 請求支払
• 買掛と売掛照合
• 代金請求
• 支払と回収管理
G. 品質管理
• 着荷障害通知
• フィールド障害通知
• 工程、材料、加工方法、人員変更通知
預託在庫通知
輸出梱包
H. 支給取引
• 支給計画
• 支給実績
• 支給品受領と検収
• 支給品在庫管理
• 支給品買掛と請求
コンサイメント標準納品システム
• 送品案内書とJラベル発行
• コンサイメント入庫予定
• コンサイメント入庫実績
• コンサイメント出荷実績
• 研修
海外取引モデルの対象
受注者 社内の業務プロセス
部品企画設計 ・開発
販売計画 ・推進
受注
生産・在庫
出荷
顧客サポート ・債権管理
7
All Rights Reserved, Copyright © 2019 JEITA
ECALGA


2. JEITA ECセンター活動紹介
2-1. ECLAGAの拡張及び維持 - ユーザー数の推移 -
• 合計: 27,266件
内ECセンター: 13,891件 (約51%)
2018年6月時点
• 統一企業コードは、日本国内のIT・エレクトロニクス業界では広く普及している。
• 今後は、業務範囲の拡大、グローバルへの展開を狙う。
Number of Companies That Have Obtained Codes
the number of codes
30,000
25,000
20,000
15,000
10,000
5,000
0
EC Center
the total number of company codes
the number of EC Center 13,891
the total number of company codes 27,266
'98 00/2 01/2 02/2 03/2 04/2 05/2 06/2 07/2 08/2 09/2 10/2 11/2 12/2 13/2 14/2 15/2 16/2 17/2 17/10 18/2 18/6
8
All Rights Reserved, Copyright © 2019 JEITA
ECALGA

2. JEITA ECセンター活動紹介
2-2. 国際標準化団体との連携

- JEITAは国際標準化団体と連携し、国際標準の策定に協力。

- IEC
  - IEC61360-4(CDD: Common Data Dictionary)とECALS辞書コンテンツ提供
- eCl@ss
  - d-m@p PJ（IECとeCl@ssの辞書マッピングプロジェクト）への協力
- EDIFICE
  - Electronic Component Package label国際標準(IEC 62090)の見直し検討

9 All Rights Reserved, Copyright © 2019 JEITA ECALGA

2. JEITA ECセンター活動紹介
2-3. 次世代企業間連携の調査・検討

- 企業間連携の次の標準化の芽を見極めるため、IoT先進事例や先進的な取組事例の調査を定期的に実施。

#	テーマ	調査内容
1	2015年度テクノロジー・業界トレンド	グローバル（ドイツ・米国・中国・日本）のIoT動向や各業界の技術動向の調査
2	Blockchain技術	Blockchain技術の調査及び活用の企業間連携における活用検討
3	Industri4.0・IoT事例	自動車業界を中心にIndustrie4.0・IoTの個社事例を調査
4	2018年度テクノロジー・業界トレンド	『#1. 2015年度テクノロジー・業界トレンド調査』のアップデート

10 All Rights Reserved, Copyright © 2019 JEITA ECALGA

ECALGA
11
All Rights Reserved, Copyright © 2019 JEITA
ECALGA

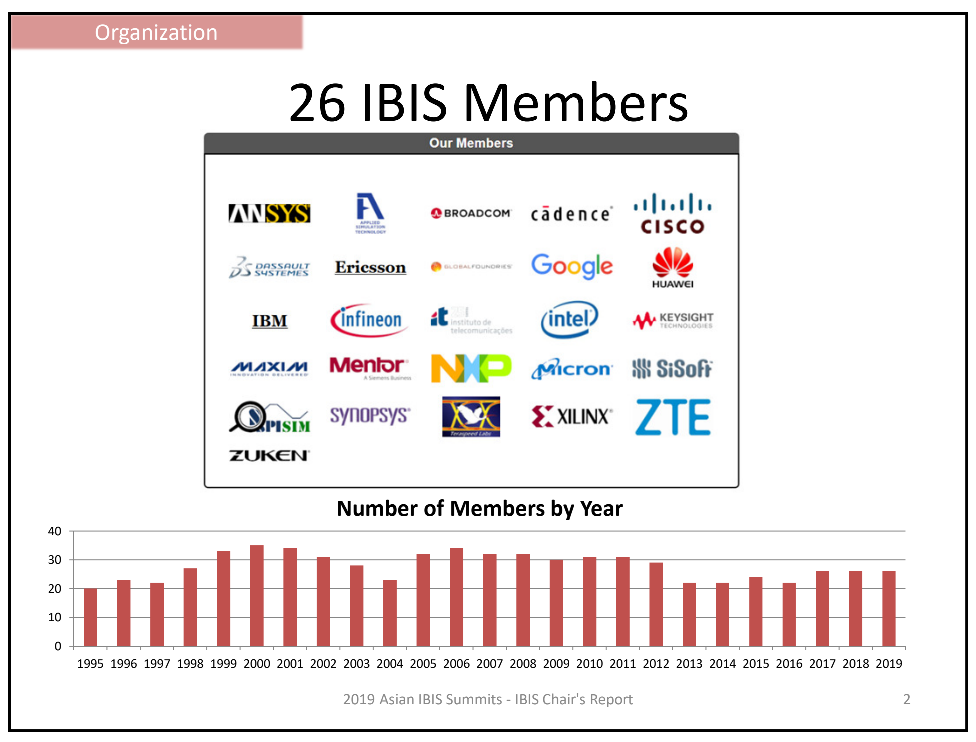
IBIS Chair’s Report

Randy Wolff
Micron Technology
Chair, IBIS Open Forum

2019 Asian IBIS Summits
Tokyo, Japan
November 8, 2019

http://www.ibis.org/

2019 Asian IBIS Summits - IBIS Chair's Report 1



Organization

IBIS Officers 2019-2020

Chair:	*Randy Wolff, Micron Technology*
Vice-Chair:	*Lance Wang, Zuken USA*
Secretary:	*Curtis Clark, ANSYS*
Treasurer:	*Bob Ross, Teraspeed Labs*
Librarian:	*Anders Ekholm, Ericsson*
Postmaster:	*Mike LaBonte, SiSoft (MathWorks)*
Webmaster:	*Steve Parker, GlobalFoundries*

Organization

IBIS Meetings

- Weekly teleconferences
  - Quality Task Group (Tuesdays)
  - Advanced Technology Modeling Task Group (Tuesdays)
  - Interconnect Task Group (Wednesdays)
  - Editorial Task Group (some Fridays)
- IBIS Open Forum teleconference every 3 weeks
  - 502 meetings so far
- IBIS Summit meetings: DesignCon, IEEE SPI, Shanghai, Taipei, Tokyo

Organization

SAE ITC

- SAE Industry Technologies Consortia is the parent organization of the IBIS Open Forum
- IBIS is assisted by SAE employees José Godoy, Phyllis Gross, Laurie Strom
- SAE ITC provides financial, legal, and other services
- http://www.sae-itc.org/

Organization

Task Groups

- Interconnect Task Group
  - Chair: Michael Mirmak, Intel
  - http://ibis.org/interconn_wip/
  - Develop on-die/package/module/connector interconnect modeling BIRDs
- Advanced Technology Modeling Task Group
  - Chair: Arpad Muranyi, Mentor, A Siemens Business
  - http://ibis.org/atm_wip/
  - Develop most other technical BIRDs
- Quality Task Group
  - Chair: Mike LaBonte, SiSoft (MathWorks)
  - http://ibis.org/quality_wip/
  - Oversee IBISCHK parser testing and development
- Editorial Task Group
  - Chair: Michael Mirmak, Intel
  - http://ibis.org/editorial_wip/
  - Produce IBIS Specification documents

BIRD = Buffer Issue Resolution Document

Specification Development

IBIS Milestones

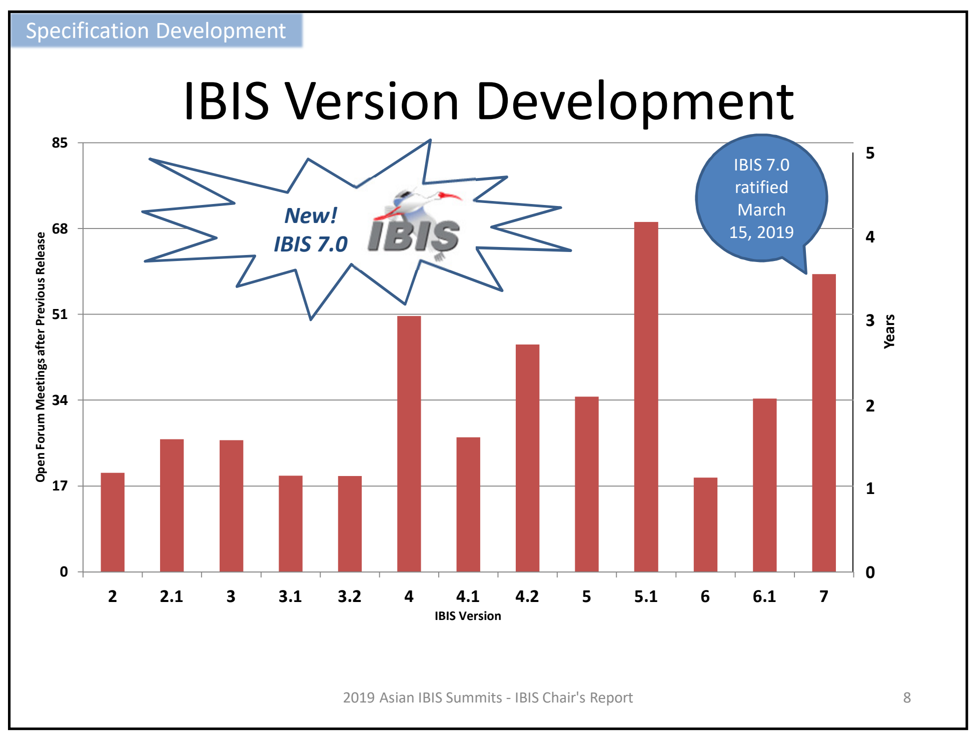
<u>I/O Buffer Information Specification</u>

- 1993-1994 **IBIS 1.0-2.1**:
  - Behavioral buffer model (fast simulation)
  - Component pin map (easy EDA import)
- 1997-1999 **IBIS 3.0-3.2**:
  - Package models
  - Electrical Board Description (EBD)
  - Dynamic buffers
- 2002-2006 **IBIS 4.0-4.2**:
  - Receiver models
  - AMS languages
- 2007-2012 **IBIS 5.0-5.1**:
  - IBIS-AMI SerDes models
  - Power aware
- 2013-2015 **IBIS 6.0-6.1**:
  - PAM4 multi-level signaling
  - Power delivery package models
- 2019 **IBIS 7.0**:
  - Back-channel support
  - Interconnect modeling using IBIS-ISS and Touchstone

<u>Other Work</u>

- 1995: **ANSI/EIA-656**
  - IBIS 2.1
- 1999: **ANSI/EIA-656-A**
  - IBIS 3.2
- 2001: **IEC 62014-1**
  - IBIS 3.2
- 2003: **ICM 1.0**
  - Interconnect Model Specification
- 2006: **ANSI/EIA-656-B**
  - IBIS 4.2
- 2009: **Touchstone 2.0**
- 2011: **IBIS-ISS 1.0**
  - Interconnect SPICE Subcircuit specification

2019 Asian IBIS Summits - IBIS Chair's Report 7



Specification Development

IBISCHK7 Version 7.0.0

- Executables available at www.ibis.org/ibischk7/
  - Interconnect Model syntax
  - Subdirectory references
  - Bus_label definitions
  - Etc.
- Contact treasurer@ibis.org for Source Code License purchase ($3,000)

Beyond IBIS 7.0

- Currently 5 BIRDs in discussion
  - 2 about redriver flow (BIRD166.4, BIRD190)
  - 1 editorial (BIRD181.1)
  - 1 to support single-ended IBIS-AMI (BIRD197.4)
  - 1 for on-die PDN modeling (BIRD198)
- EBD update supporting IBIS-ISS and Touchstone
  - Improved module and multi-chip package modeling
- BIRD200 approved: C_comp model supporting IBIS-ISS and Touchstone
- BIRD195.1 approved: [Rgnd] and [Rpower] for IBIS-AMI Input models
- What other new ideas do you have for IBIS?

What Else Could IBIS Be Used For?

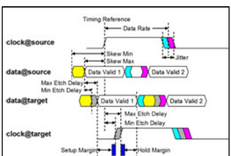
- IBIS is nominally about I/O buffers, used to:
  - Solve signal quality problems like loss, inter-symbol interference (ISI) and crosstalk
  - Generate waveforms used in timing analysis
- But engineers also:
  - Insure proper timing between pins
  - Insure sufficient power distribution
  - Include optical links in analyses
  - Analyze channel operating margin (COM), forward error correction (FEC), etc.
  - Comply with any other new requirements posed by JEDEC, etc.

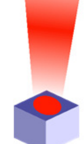
- What other data might IBIS formats convey?

New Directions for IBIS?

- IBIS VRM models
- IBIS chip power models
- IBIS timing models
- IBIS waveform analysis language
- Data probability distributions (or at least more than 3 corners)
- IBIS-ISS [Test Load], external [Test Data]
- Optical Model_type(s) for Vertical Cavity Surface Emitting Laser (VCSEL), etc.

IN OUT
REF





Submitting Your Idea – BIRD Process

- BIRD – Buffer Issue Resolution Document
  - Official method for submitting a proposed change to the IBIS specification
- BIRD Template found on IBIS website
  - Standardized method to describe your idea
- Submit BIRD to chair@ibis.org
- BIRDs discussed in Open Forum meetings
  - Eventual vote by members for approval
- Idea not ready for an official BIRD?
  - Join an IBIS Task Group meeting for technical discussion

BIRD Link on IBIS Website

IBIS

Welcome to the IBIS Open Forum

NEW 2019 IBIS Touchstone Survey Report : Touchstone Survey

NEW IBIS Version 7.0 has been ratified : IBIS 7.0

Upcoming Events
Past Summits

Open Forum
Minutes
Regional Forums
China
Task Groups
ATM
Quality
Interconnect
Editorial
Members
Roster

Specifications
BIRDs
Models

Our Specifications

I/O Buffer Information Specification	(IBIS 7.0) (SAE/EIA-STD-656-B) (IEC-62014-1)
IBIS Interconnect Modeling Specification	(ICM 1.1) (SAE/GEIA-STD-0001)
IBIS Interconnect SPICE Subcircuit Specification	(IBIS-ISS 1.0)
Touchstone® File Format Specification	(Touchstone 2.0)

Our Members

Link to BIRDs webpage

BIRD Template Link on the BIRD Webpage

Buffer Issue Resolution Documents (BIRD)

To submit a BIRD to the IBIS Open Forum, please use the BIRD Template, Rev. 1.3.

ID#	Issue Title	Requester	Date Submitted	Date Accepted	Supporting Version
200	C_comp Model Using IBIS-ISS or Touchstone	Randy Wolff, Micron Technology, Inc. Walter Katz, Signal Integrity Software, Inc.	July 9, 2019	September 27, 2019	
199	Fix Rx_Receiver_Sensitivity Inconsistencies	Arpad Muranyi, Mentor a Siemens Business	March 19, 2019	June 7, 2019	
198	Keyword additions for On Die PDN (Power Distribution Network) Modeling	Kazuki Murata; Ricoh Co., Ltd.; Miyoko Goto; Ricoh Co., Ltd.; Kazuyuki Sakata; Renesas Electronics Corporation; Kazunori Yamada; Renesas Electronics Corporation; Kouji Ichikawa; Denso Corporation; Atsushi Tomishima; Toshiba Electronic Devices & Storage Corporation; Takashi Hasegawa; Sony LSI Design Inc.; Koichi Seko, Panasonic Industrial Devices Systems and Technology Co., Ltd.; Toshiki Kanamoto; Hirosaki University Megumi Ono; Socionext Inc.	March 11, 2019		
197.4	New AMI Reserved Parameters DC_Offset and NRZ_Threshold	Walter Katz, SiSoft, Ambrish Varma, Cadence Design Systems, Randy Wolff, Micron Technology, Justin Butterfield, Micron Technology, Fangyi Rao, Keysight Technologies	November 27, 2018, December 4, 2018, January 15, 2019, June 25, 2019, July 23, 2019		
196.1	Prohibit Periods at the End of File Names	Arpad Muranyi, Mentor Graphics, A Siemens Business	September 25, 2018, October 12, 2018	October 12, 2018	7.0
195.1	Enabling [Rgnd] and [Rpower] Keywords for Input Models	Michael Mirmak, Intel Corp.	June 19, 2018, June 29, 2018	August 31, 2018	

[Thank You]

IBIS Open Forum:
Web: http://www.ibis.org
Email: ibis-info@freelists.org

We welcome participation by all IBIS model makers, EDA tool vendors, IBIS model users, and interested parties.

Agenda

- Introduction
- IBIS 7.0 INTERCONNECT MODELING Outline
- Expectations for IBIS7.0 INTERCONNECT MODELING
- Post-layout simulator issues when using the IBIS 7.0 INTERCONNECT MODEL
- Summary

2

Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED

Introduction

- In March this year, a new interconnect modeling specification was released in IBIS 7.0.
- Therefore, this time, we predicted the superiority of this specification in SI analysis and PI analysis by comparing with the conventional model.
- It also describes the predicted post-layout simulator issues when using the IBIS 7.0 INTERCONNECT MODEL.

IBIS

(I/O Buffer Information Specification)

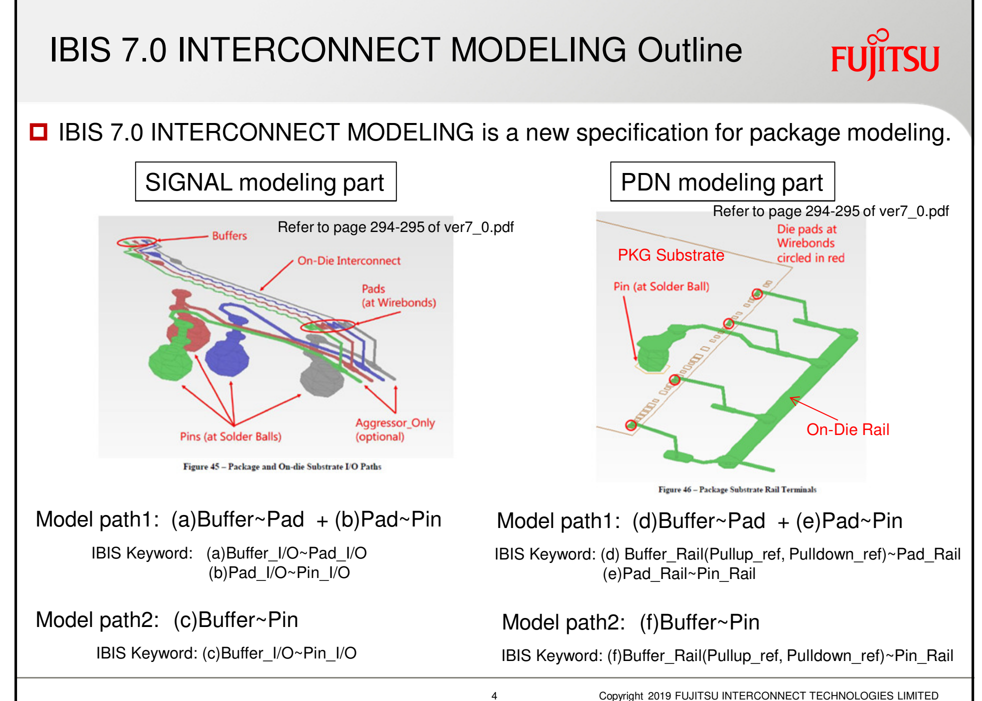
Version 7.0

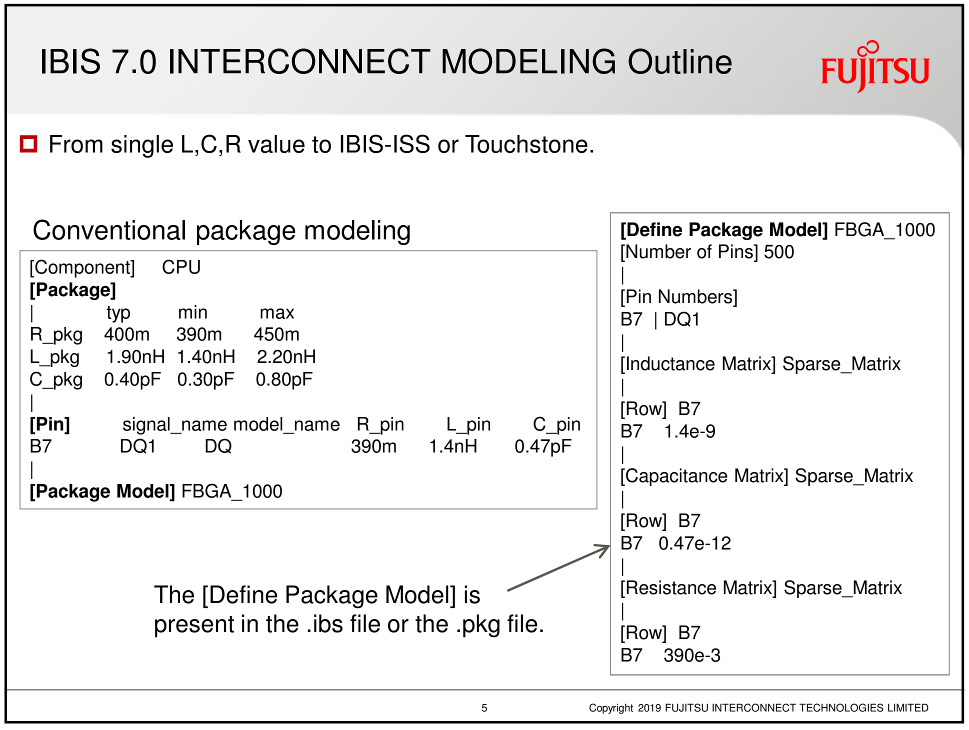
Ratified March 15, 2019

© IBIS Open Forum 2019

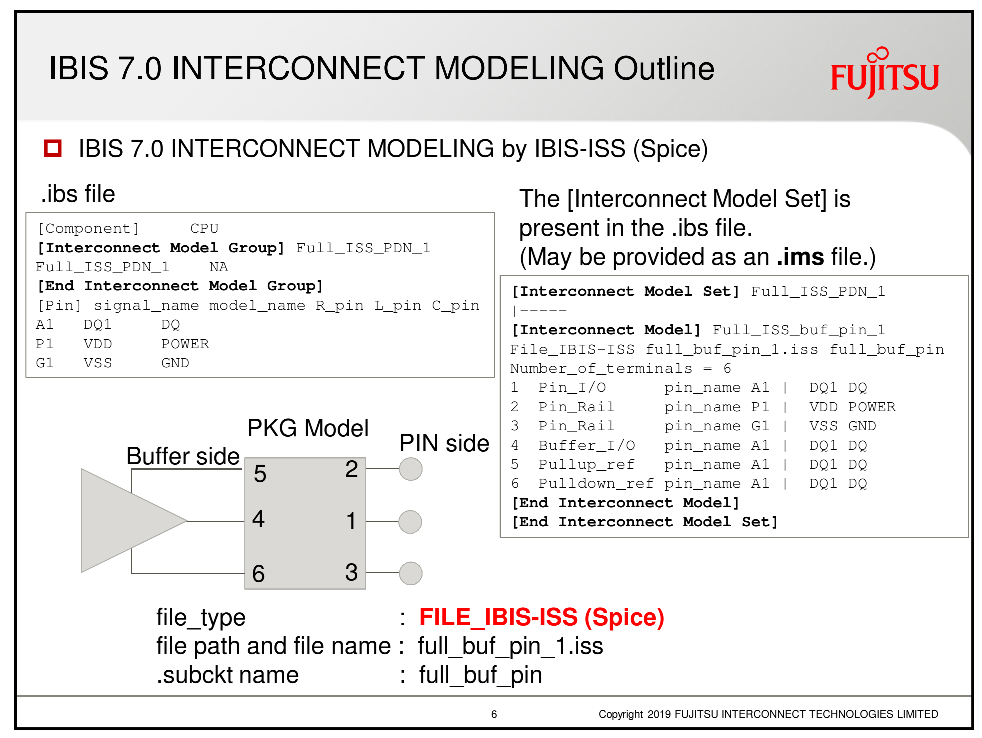
3

Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED

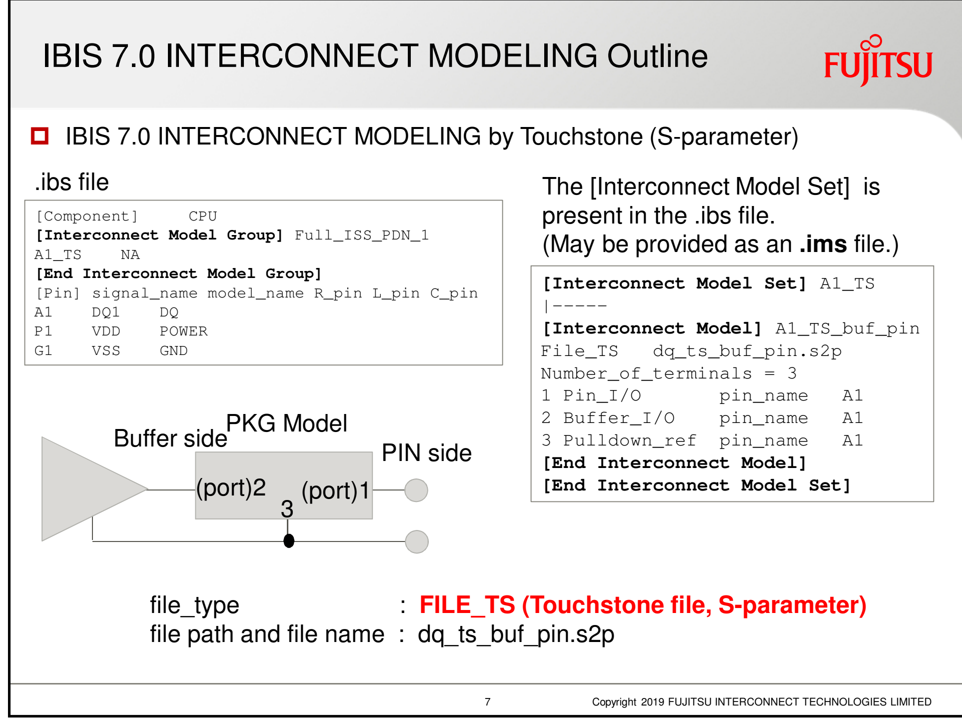




IBIS 7.0 INTERCONNECT MODELING Outline
FUJITSU
From single L,C,R value to IBIS-ISS or Touchstone.
Conventional package modeling
[Component] CPU
[Package]
| typ min max
R_pkg 400m 390m 450m
L_pkg 1.90nH 1.40nH 2.20nH
C_pkg 0.40pF 0.30pF 0.80pF
|
[Pin] signal_name model_name R_pin L_pin C_pin
B7 DQ1 DQ 390m 1.4nH 0.47pF
|
[Package Model] FBGA_1000
[Define Package Model] FBGA_1000
[Number of Pins] 500
|
[Pin Numbers]
B7 | DQ1
|
[Inductance Matrix] Sparse_Matrix
|
[Row] B7
B7 1.4e-9
|
[Capacitance Matrix] Sparse_Matrix
|
[Row] B7
B7 0.47e-12
|
[Resistance Matrix] Sparse_Matrix
|
[Row] B7
B7 390e-3
The [Define Package Model] is present in the .ibs file or the .pkg file.
5
Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED



IBIS 7.0 INTERCONNECT MODELING Outline
FUJITSU
IBIS 7.0 INTERCONNECT MODELING by IBIS-ISS (Spice)
.ibs file
[Component] CPU
[Interconnect Model Group] Full_ISS_PDN_1
Full_ISS_PDN_1 NA
[End Interconnect Model Group]
[Pin] signal_name model_name R_pin L_pin C_pin
A1 DQ1 DQ
P1 VDD POWER
G1 VSS GND
The [Interconnect Model Set] is present in the .ibs file.
(May be provided as an .ims file.)
[Interconnect Model Set] Full_ISS_PDN_1
|-----
[Interconnect Model] Full_ISS_buf_pin_1
File_IBIS-ISS full_buf_pin_1.iss full_buf_pin
Number_of_terminals = 6
1 Pin_I/O pin_name A1 | DQ1 DQ
2 Pin_Rail pin_name P1 | VDD POWER
3 Pin_Rail pin_name G1 | VSS GND
4 Buffer_I/O pin_name A1 | DQ1 DQ
5 Pullup_ref pin_name A1 | DQ1 DQ
6 Pulldown_ref pin_name A1 | DQ1 DQ
[End Interconnect Model]
[End Interconnect Model Set]
PKG Model
Buffer side
PIN side
5
2
4
1
6
3
file_type : FILE_IBIS-ISS (Spice)
file path and file name : full_buf_pin_1.iss
.subckt name : full_buf_pin
6
Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED



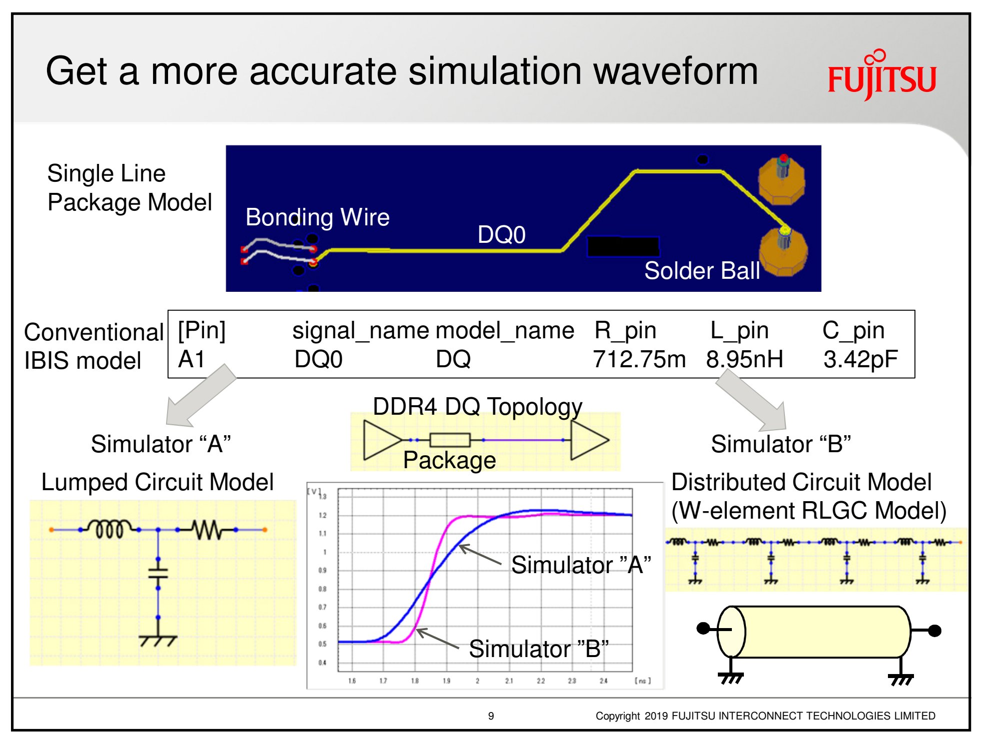
FUJITSU

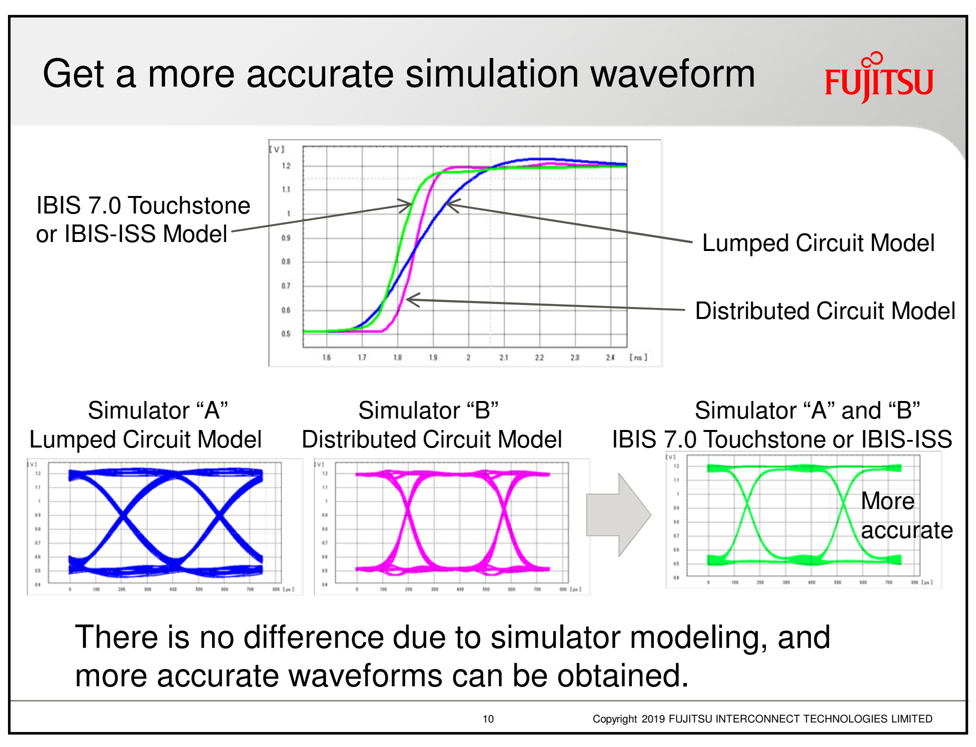
Expectations for IBIS7.0 INTERCONNECT MODELING

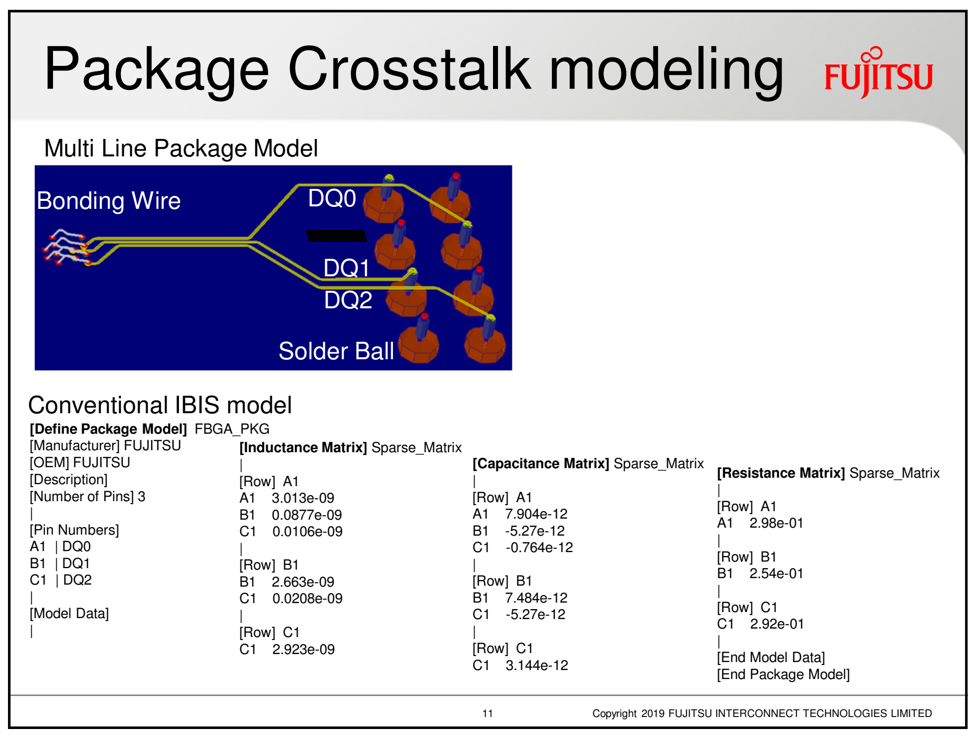
- Get a more accurate simulation waveform
- Package Crosstalk modeling
- Package PDN modeling

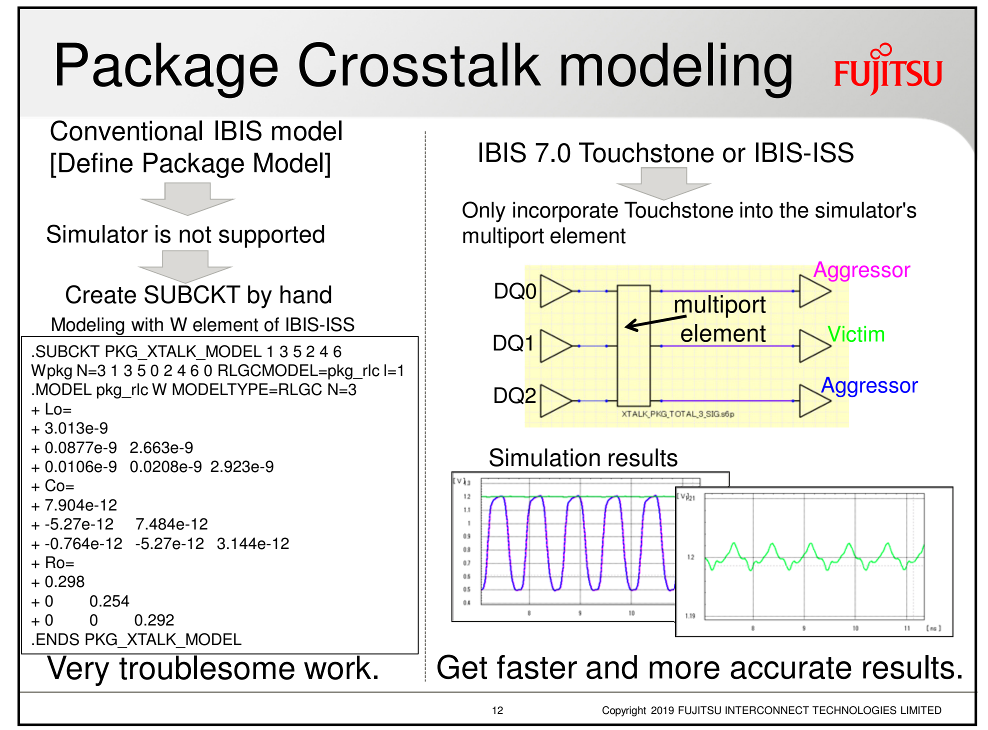
8

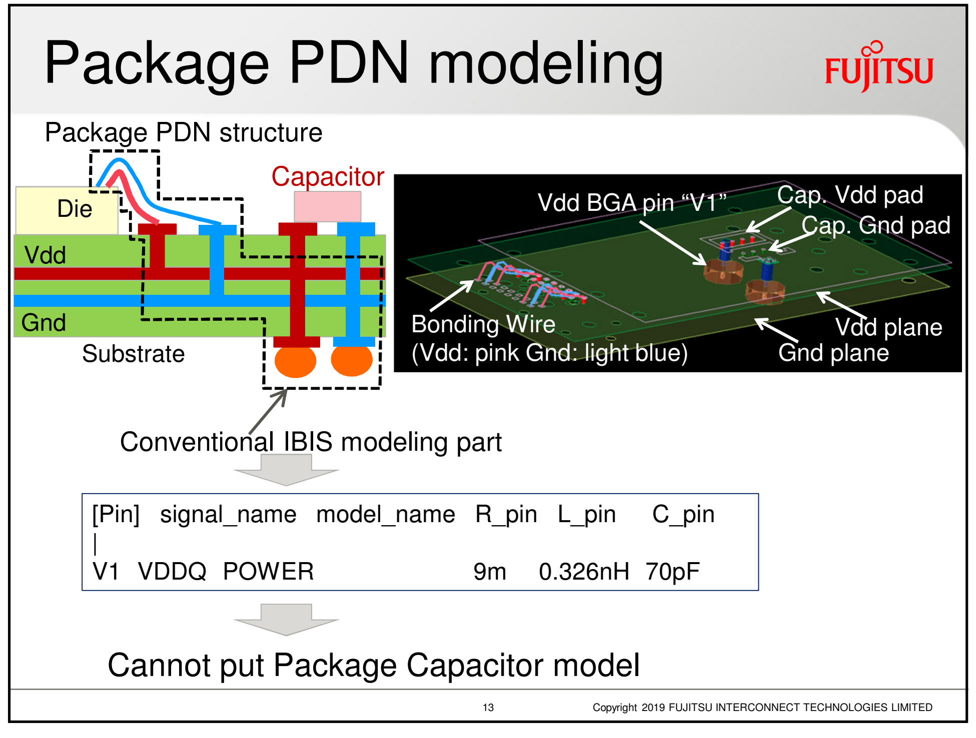
Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED

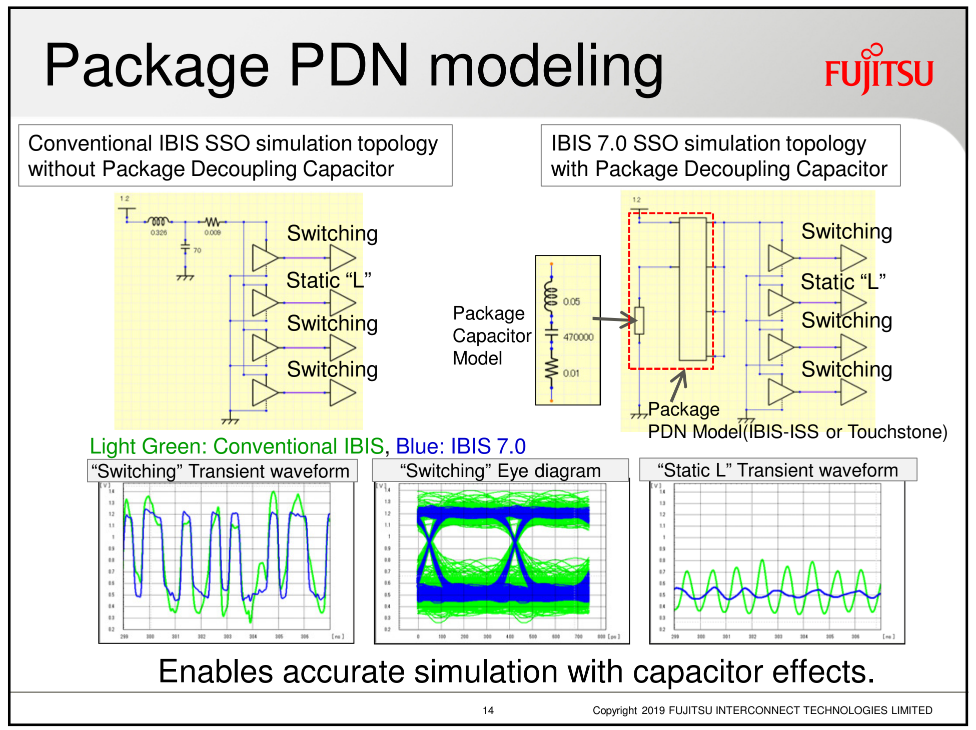

Get a more accurate simulation waveform
FUJITSU
Single Line
Package Model
Bonding Wire
DQ0
Solder Ball
Conventional
IBIS model
[Pin] signal_name model_name R_pin L_pin C_pin
A1 DQ0 DQ 712.75m 8.95nH 3.42pF
DDR4 DQ Topology
Package
Simulator "A"
Lumped Circuit Model
Simulator "B"
Distributed Circuit Model
(W-element RLGC Model)
Simulator "A"
Simulator "B"
9
Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED


Get a more accurate simulation waveform
FUJITSU
IBIS 7.0 Touchstone
or IBIS-ISS Model
Lumped Circuit Model
Distributed Circuit Model
Simulator "A"
Lumped Circuit Model
Simulator "B"
Distributed Circuit Model
Simulator "A" and "B"
IBIS 7.0 Touchstone or IBIS-ISS
More
accurate
There is no difference due to simulator modeling, and
more accurate waveforms can be obtained.
10
Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED


Package Crosstalk modeling
FUJITSU
Multi Line Package Model
Bonding Wire
DQ0
DQ1
DQ2
Solder Ball
Conventional IBIS model
[Define Package Model] FBGA_PKG
[Manufacturer] FUJITSU
[OEM] FUJITSU
[Description]
[Number of Pins] 3
|
[Pin Numbers]
A1 | DQ0
B1 | DQ1
C1 | DQ2
|
[Model Data]
|
[Inductance Matrix] Sparse_Matrix
|
[Row] A1
A1 3.013e-09
B1 0.0877e-09
C1 0.0106e-09
|
[Row] B1
B1 2.663e-09
C1 0.0208e-09
|
[Row] C1
C1 2.923e-09
[Capacitance Matrix] Sparse_Matrix
|
[Row] A1
A1 7.904e-12
B1 -5.27e-12
C1 -0.764e-12
|
[Row] B1
B1 7.484e-12
C1 -5.27e-12
|
[Row] C1
C1 3.144e-12
[Resistance Matrix] Sparse_Matrix
|
[Row] A1
A1 2.98e-01
|
[Row] B1
B1 2.54e-01
|
[Row] C1
C1 2.92e-01
|
[End Model Data]
[End Package Model]
11
Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED


Package Crosstalk modeling
FUJITSU
Conventional IBIS model
[Define Package Model]
Simulator is not supported
Create SUBCKT by hand
Modeling with W element of IBIS-ISS
.SUBCKT PKG_XTALK_MODEL 1 3 5 2 4 6
Wpkg N=3 1 3 5 0 2 4 6 0 RLGCMODEL=pkg_rlc l=1
.MODEL pkg_rlc W MODELTYPE=RLGC N=3
+ Lo=
+ 3.013e-9
+ 0.0877e-9 2.663e-9
+ 0.0106e-9 0.0208e-9 2.923e-9
+ Co=
+ 7.904e-12
+ -5.27e-12 7.484e-12
+ -0.764e-12 -5.27e-12 3.144e-12
+ Ro=
+ 0.298
+ 0 0.254
+ 0 0 0.292
.ENDS PKG_XTALK_MODEL
Very troublesome work.
IBIS 7.0 Touchstone or IBIS-ISS
Only incorporate Touchstone into the simulator's multiport element
DQ0
DQ1
DQ2
multiport element
Aggressor
Victim
Aggressor
Simulation results
Get faster and more accurate results.
12
Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED


Package PDN modeling
FUJITSU
Package PDN structure
Capacitor
Die
Vdd
Gnd
Substrate
Vdd BGA pin "V1"
Cap. Vdd pad
Cap. Gnd pad
Bonding Wire
(Vdd: pink Gnd: light blue)
Vdd plane
Gnd plane
Conventional IBIS modeling part
[Pin] signal_name model_name R_pin L_pin C_pin
|
V1 VDDQ POWER 9m 0.326nH 70pF
Cannot put Package Capacitor model
13
Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED


Package PDN modeling
FUJITSU
Conventional IBIS SSO simulation topology without Package Decoupling Capacitor
IBIS 7.0 SSO simulation topology with Package Decoupling Capacitor
Switching
Static "L"
Switching
Switching
Package Capacitor Model
Package PDN Model(IBIS-ISS or Touchstone)
Light Green: Conventional IBIS, Blue: IBIS 7.0
"Switching" Transient waveform
"Switching" Eye diagram
"Static L" Transient waveform
Enables accurate simulation with capacitor effects.
14
Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED

Post-layout simulator issues when using the IBIS7.0 INTERCONNECT MODEL

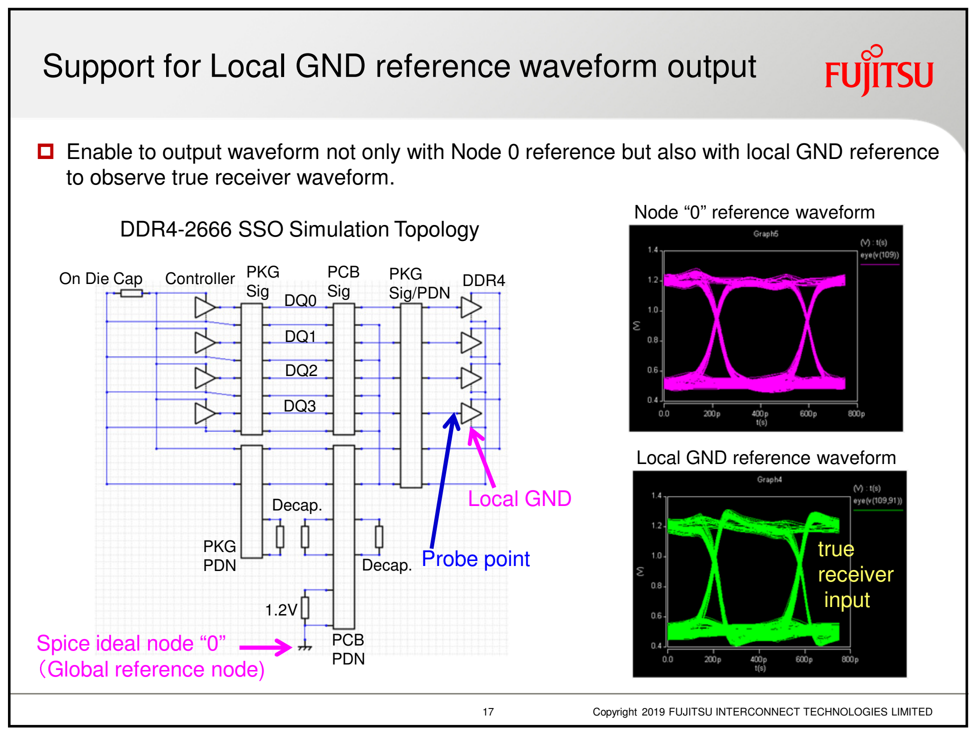
- Post-layout simulator issues
- Support for Local GND reference waveform output
- Support for Touchstone Version 2.0
- Support for S-element with N reference nodes

15 Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED

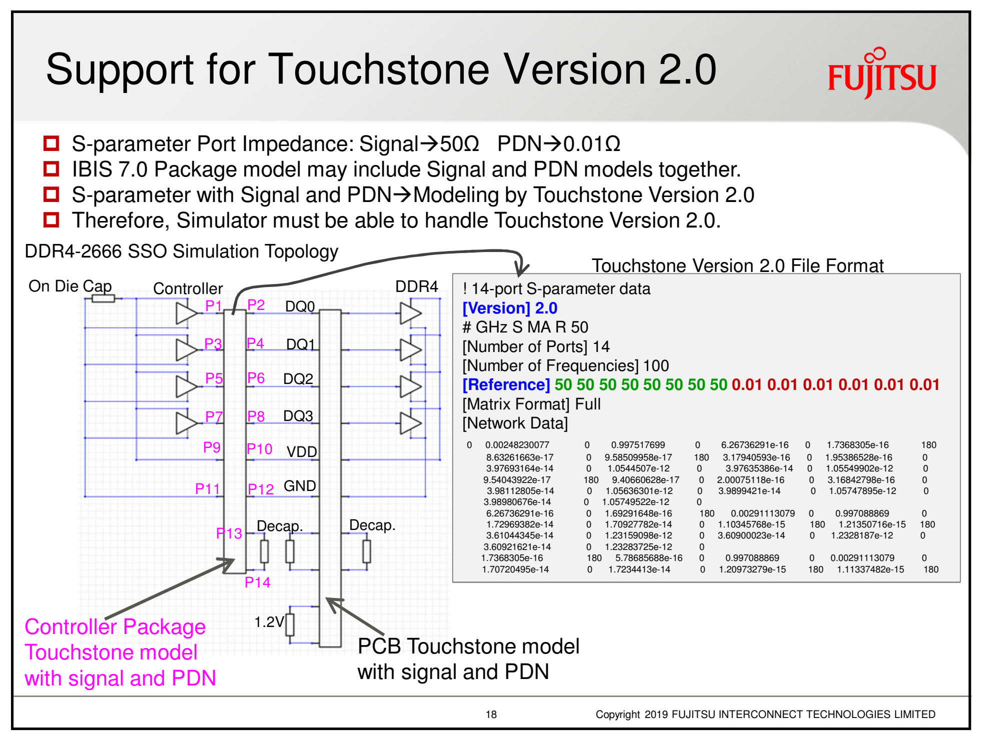
Post-layout simulator issues

- The post-layout simulator verifies a large number of nets in a short time. Therefore, the power and GND nets are treated as an ideal, and the transmission waveform viewed from the ideal GND (node 0 in Spice) is output.
- However, since the IBIS 7.0 INTERCONNECT MODEL includes a high-accuracy Package PDN model, SI simulation considering PI (power-aware simulation) is possible.
- Therefore, the functions required for the simulator in the post-layout simulation using the IBIS 7.0 INTERCONNECT MODEL are described below.

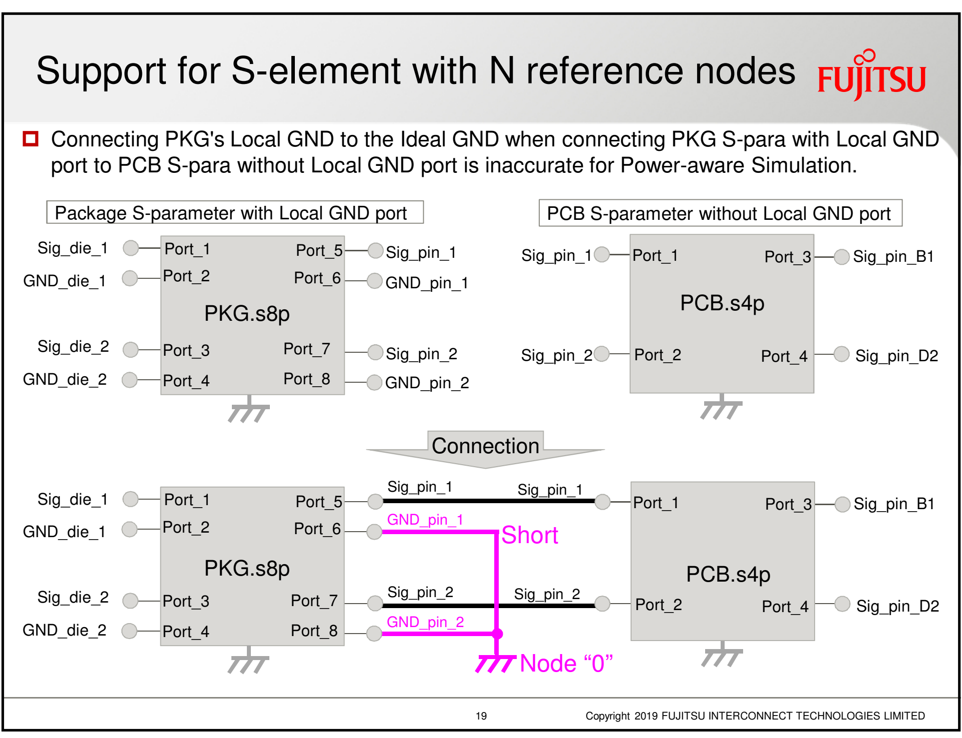
16 Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED



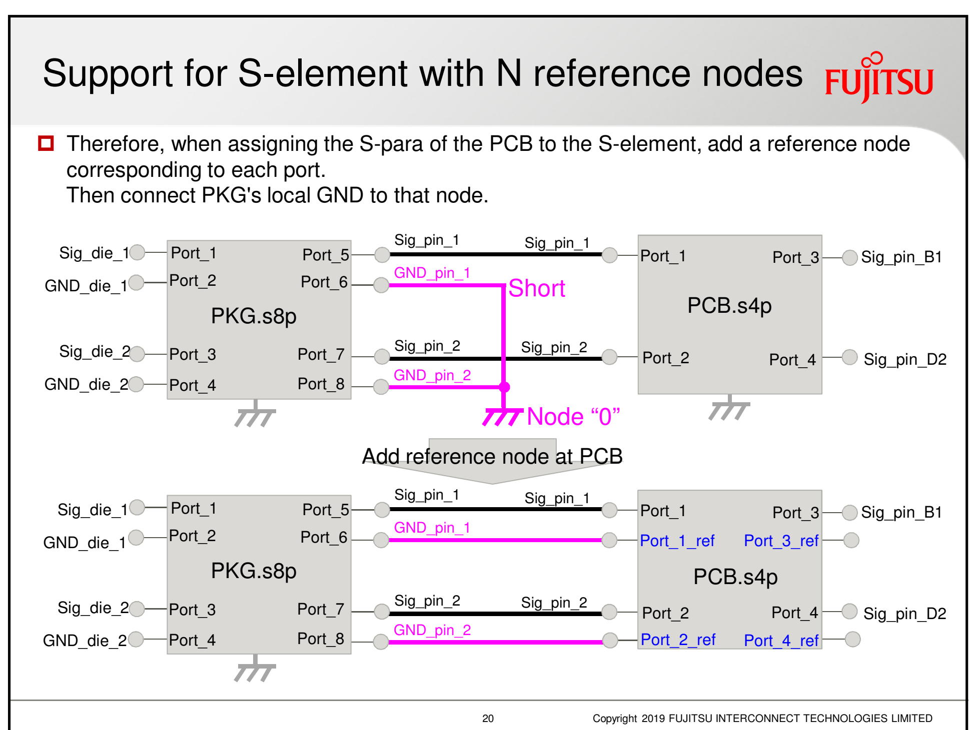
Support for Local GND reference waveform output
FUJITSU
Enable to output waveform not only with Node 0 reference but also with local GND reference to observe true receiver waveform.
DDR4-2666 SSO Simulation Topology
On Die Cap
Controller
PKG Sig
PCB Sig
PKG Sig/PDN
DDR4
DQ0
DQ1
DQ2
DQ3
Decap.
PKG PDN
Decap.
1.2V
PCB PDN
Local GND
Probe point
Spice ideal node "0"
(Global reference node)
Node "0" reference waveform
Local GND reference waveform
true receiver input
17
Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED



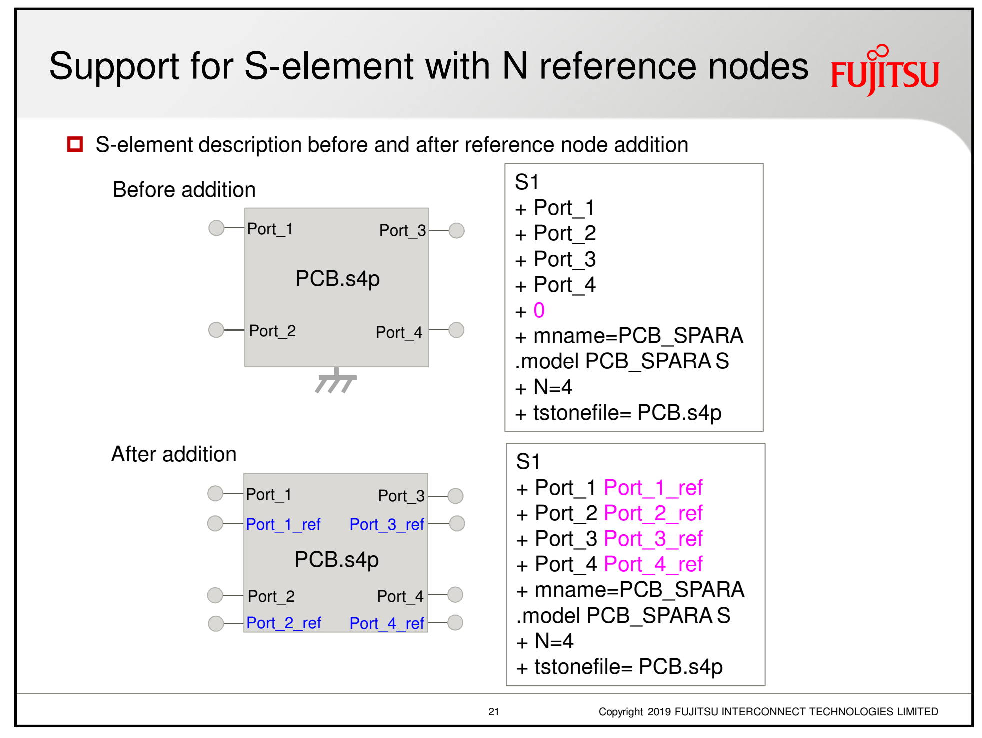
Support for Touchstone Version 2.0
FUJITSU
S-parameter Port Impedance: Signal→50Ω PDN→0.01Ω
IBIS 7.0 Package model may include Signal and PDN models together.
S-parameter with Signal and PDN→Modeling by Touchstone Version 2.0
Therefore, Simulator must be able to handle Touchstone Version 2.0.
DDR4-2666 SSO Simulation Topology
On Die Cap
Controller
DDR4
P1
P2
DQ0
P3
P4
DQ1
P5
P6
DQ2
P7
P8
DQ3
P9
P10
VDD
P11
P12
GND
P13
Decap.
Decap.
P14
1.2V
Controller Package Touchstone model with signal and PDN
PCB Touchstone model with signal and PDN
Touchstone Version 2.0 File Format
! 14-port S-parameter data
[Version] 2.0
GHz S MA R 50
[Number of Ports] 14
[Number of Frequencies] 100
[Reference] 50 50 50 50 50 50 50 50 0.01 0.01 0.01 0.01 0.01 0.01
[Matrix Format] Full
[Network Data]
18
Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED

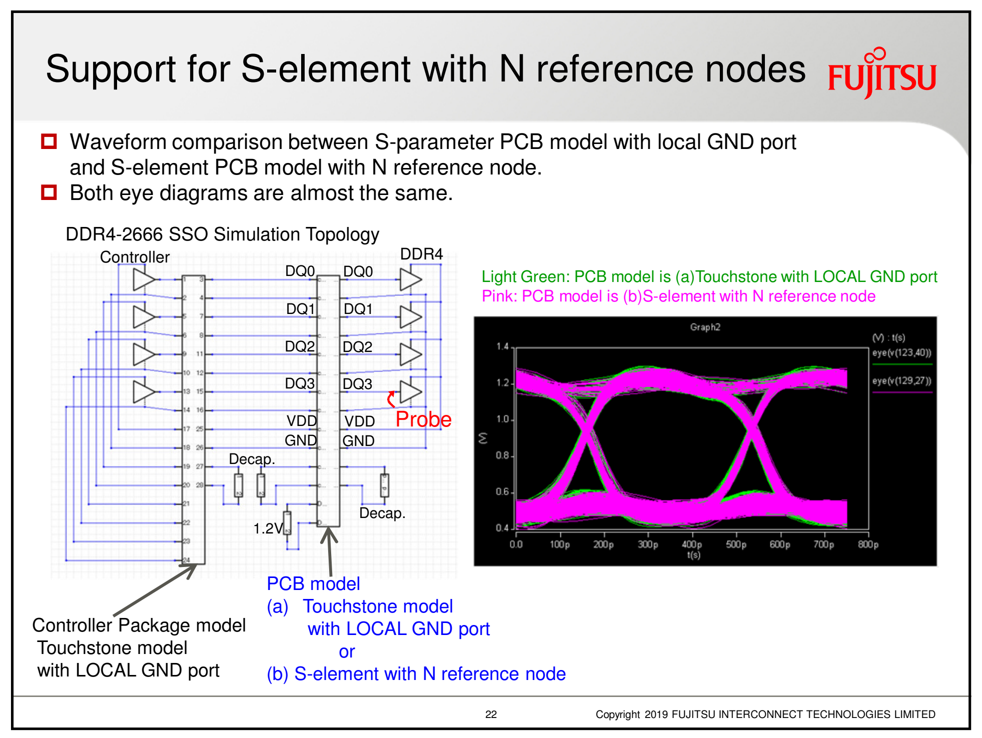


Support for S-element with N reference nodes
FUJITSU
Connecting PKG's Local GND to the Ideal GND when connecting PKG S-para with Local GND port to PCB S-para without Local GND port is inaccurate for Power-aware Simulation.
Package S-parameter with Local GND port
PCB S-parameter without Local GND port
Sig_die_1
GND_die_1
Sig_die_2
GND_die_2
Port_1
Port_2
Port_3
Port_4
Port_5
Port_6
Port_7
Port_8
PKG.s8p
Sig_pin_1
GND_pin_1
Sig_pin_2
GND_pin_2
PCB.s4p
Sig_pin_B1
Sig_pin_D2
Connection
Short
Node “0”
19
Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED



Support for S-element with N reference nodes
FUJITSU
Therefore, when assigning the S-para of the PCB to the S-element, add a reference node corresponding to each port.
Then connect PKG's local GND to that node.
Sig_die_1
GND_die_1
Sig_die_2
GND_die_2
PKG.s8p
Sig_pin_1
GND_pin_1
Sig_pin_2
GND_pin_2
Short
Node “0”
PCB.s4p
Sig_pin_B1
Sig_pin_D2
Add reference node at PCB
Port_1_ref
Port_2_ref
Port_3_ref
Port_4_ref
20
Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED


Support for S-element with N reference nodes
FUJITSU
S-element description before and after reference node addition
Before addition
Port_1
Port_3
PCB.s4p
Port_2
Port_4
S1
+ Port_1
+ Port_2
+ Port_3
+ Port_4
+ 0
+ mname=PCB_SPARA
.model PCB_SPARA S
+ N=4
+ tstonefile= PCB.s4p
After addition
Port_1
Port_3
Port_1_ref
Port_3_ref
PCB.s4p
Port_2
Port_4
Port_2_ref
Port_4_ref
S1
+ Port_1 Port_1_ref
+ Port_2 Port_2_ref
+ Port_3 Port_3_ref
+ Port_4 Port_4_ref
+ mname=PCB_SPARA
.model PCB_SPARA S
+ N=4
+ tstonefile= PCB.s4p
21
Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED


Support for S-element with N reference nodes
FUJITSU
Waveform comparison between S-parameter PCB model with local GND port and S-element PCB model with N reference node.
Both eye diagrams are almost the same.
DDR4-2666 SSO Simulation Topology
Controller
DDR4
DQ0
DQ1
DQ2
DQ3
VDD
GND
Probe
Decap.
1.2V
Light Green: PCB model is (a)Touchstone with LOCAL GND port
Pink: PCB model is (b)S-element with N reference node
Graph2
PCB model
(a) Touchstone model with LOCAL GND port
or
(b) S-element with N reference node
Controller Package model
Touchstone model
with LOCAL GND port
22
Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED

Summary

- Highly accurate simulation results are expected by the package model based on the IBIS 7.0 INTERCONNECT MODEL.
- The IBIS 7.0 package model can be applied to power-aware simulation. Therefore, the post-layout simulator must also support power-aware simulation.

23 Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED

References

- “IBIS (I/O Buffer Information Specification) Version 7.0”, IBIS Open Forum March 15, 2019 https://ibis.org/ver7.0/ver7_0.pdf
- “Touchstone® File Format Specification Version 2.0”, IBIS Open Forum April 24, 2009 https://ibis.org/touchstone_ver2.0/touchstone_ver2_0.pdf
- “IBIS Interconnect SPICE Subcircuit (IBIS-ISS) Specification Version 1.0”, IBIS Open Forum October 7, 2011 https://ibis.org/ibis-iss_ver1.0/ibis-iss_ver1_0.pdf

24 Copyright 2019 FUJITSU INTERCONNECT TECHNOLOGIES LIMITED

FUJITSU
shaping tomorrow with you

Asian IBIS Summit
Tokyo, JAPAN
November 8th, 2019

The On Die Decap modeling proposal (BIRD198)

JEITA

Semiconductor & System design technical committee

Semiconductor design technology subcommittee

Presenter : Megumi Ono (Socionext Inc).
Co-Author: Atsushi Tomishima (Toshiba Electronic Devices & Storage Corporation)

Copyright© JEITA SD-TC All Rights Reserved 2019

Agenda

- Background
- Proposal for On die De-cap model
- Feedback and updating
- Conclusion

Copyright© JEITA SD-TC All Rights Reserved 2019

Agenda

- **Background**
- Proposal for On die De-cap model
- Feedback and updating
- Conclusion

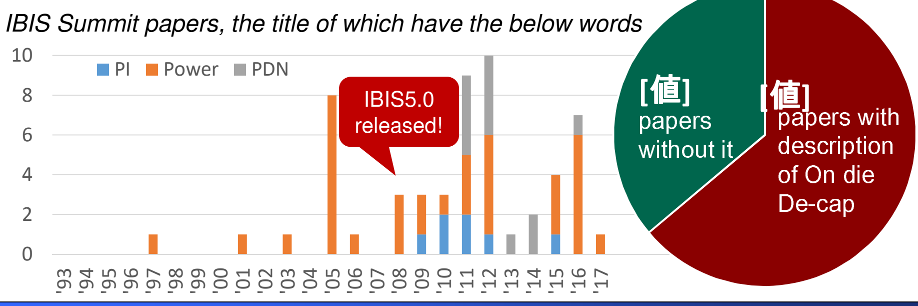
Copyright© JEITA SD-TC All Rights Reserved 2019

Chip PDN characteristic

- Chip PDN characteristic
  - On die Resistance affects IR-Drop and Q factor
  - On die De-cap affects High frequency power-supply noise

Many papers reported in IBIS Summit describe importance of On die De-cap, because it is one of the few solution that reduce high frequency power-supply noise

IBIS Summit papers, the title of which have the below words



Copyright© JEITA SD-TC All Rights Reserved 2019

A Survey of On die De-cap model

- However, board and system designers can hardly obtain On die De-cap model

A Survey by JEITA LPB-SC MDL-WG @LPB developers workshop 2017.9.2

Respondents

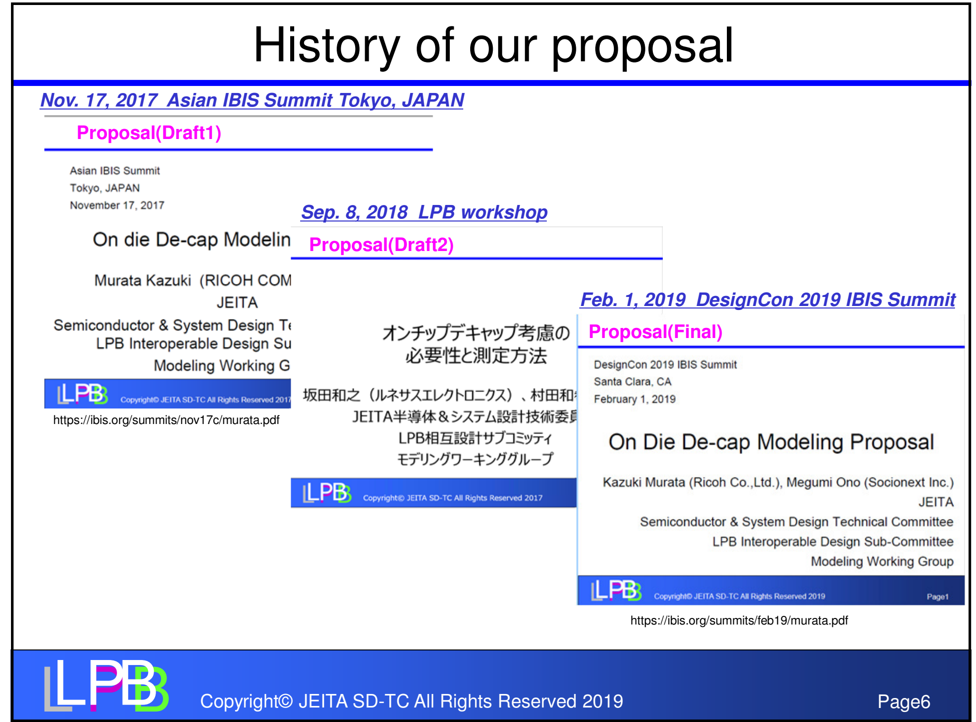
EDA
LSI designer
Board
PKG

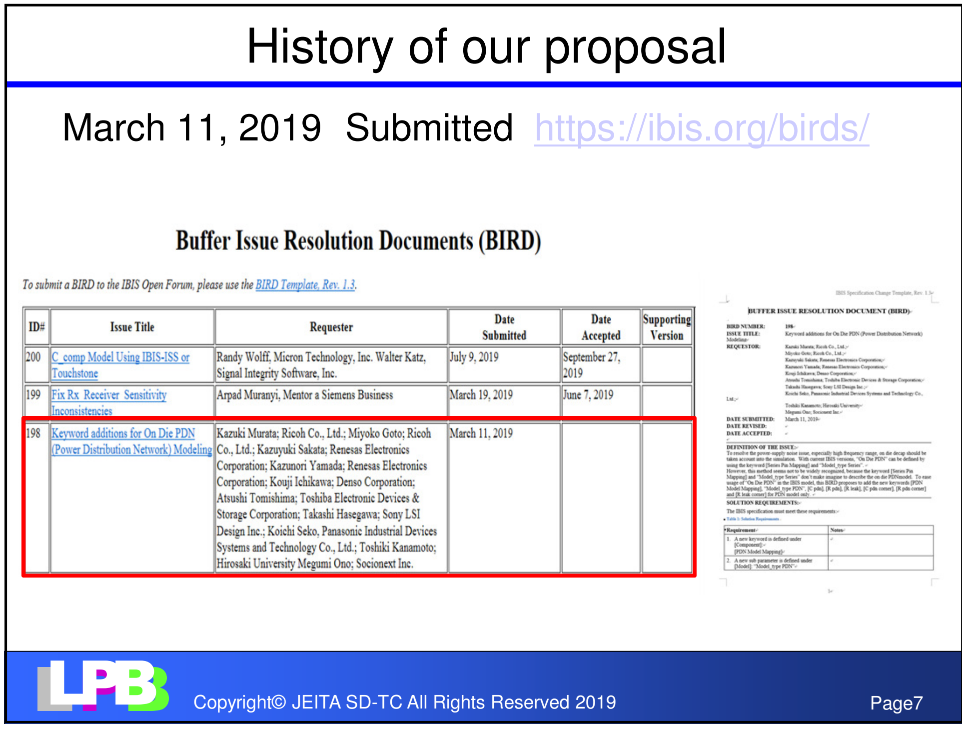
Q1. to All
"Can you obtain information about Chip PDN?"
Answer

Guideline documents: No / Yes
Target Z: No / Yes
On die De-cap model: Yes / No
PKG PDN model: No / Yes

Q2. to LSI designer
"What are you concerned about when you offer PDN model"
Answer
"Which model format is suitable for our customer?"

Copyright© JEITA SD-TC All Rights Reserved 2019





History of our proposal

March 11, 2019 Submitted https://ibis.org/birds/

Buffer Issue Resolution Documents (BIRD)

To submit a BIRD to the IBIS Open Forum, please use the BIRD Template, Rev. 1.3.

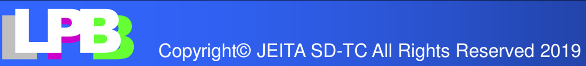
ID#	Issue Title	Requester	Date Submitted	Date Accepted	Supporting Version
200	C_comp Model Using IBIS-ISS or Touchstone	Randy Wolff, Micron Technology, Inc. Walter Katz, Signal Integrity Software, Inc.	July 9, 2019	September 27, 2019	
199	Fix Rx_Receiver_Sensitivity Inconsistencies	Arpad Muranyi, Mentor a Siemens Business	March 19, 2019	June 7, 2019	
198	Keyword additions for On Die PDN (Power Distribution Network) Modeling	Kazuki Murata; Ricoh Co., Ltd.; Miyoko Goto; Ricoh Co., Ltd.; Kazuyuki Sakata; Renesas Electronics Corporation; Kazunori Yamada; Renesas Electronics Corporation; Kouji Ichikawa; Denso Corporation; Atsushi Tomishima; Toshiba Electronic Devices & Storage Corporation; Takashi Hasegawa; Sony LSI Design Inc.; Koichi Seko, Panasonic Industrial Devices Systems and Technology Co., Ltd.; Toshiki Kanamoto; Hirosaki University Megumi Ono; Socionext Inc.	March 11, 2019		

Copyright© JEITA SD-TC All Rights Reserved 2019

Page7

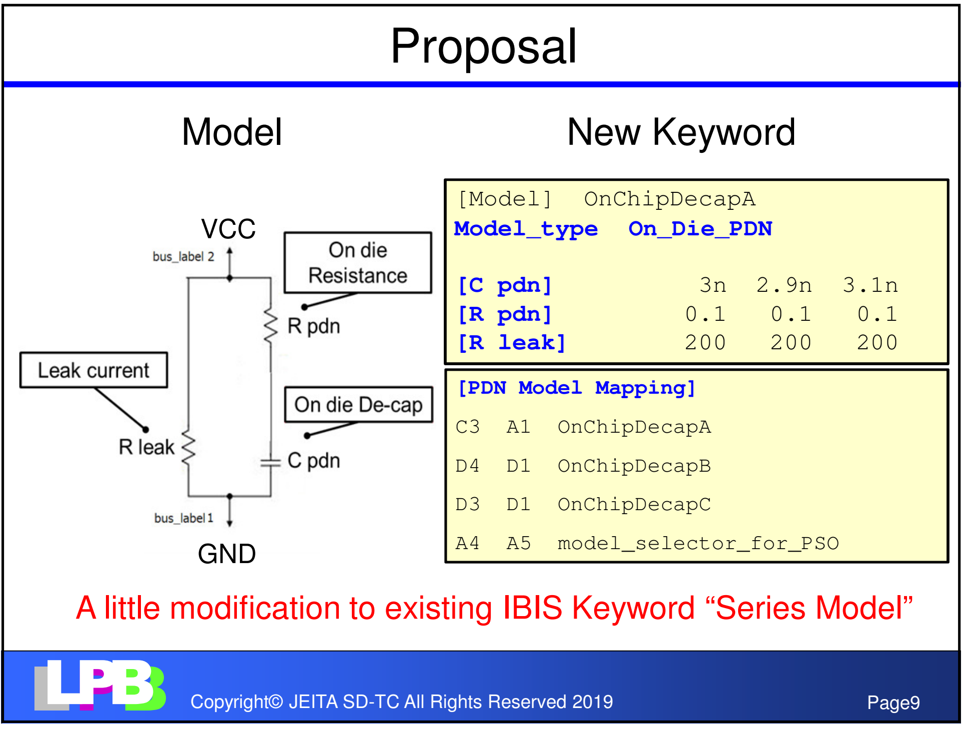
Agenda

- Background
- **Proposal for On die De-cap model**
- Feedback and updating
- Conclusion

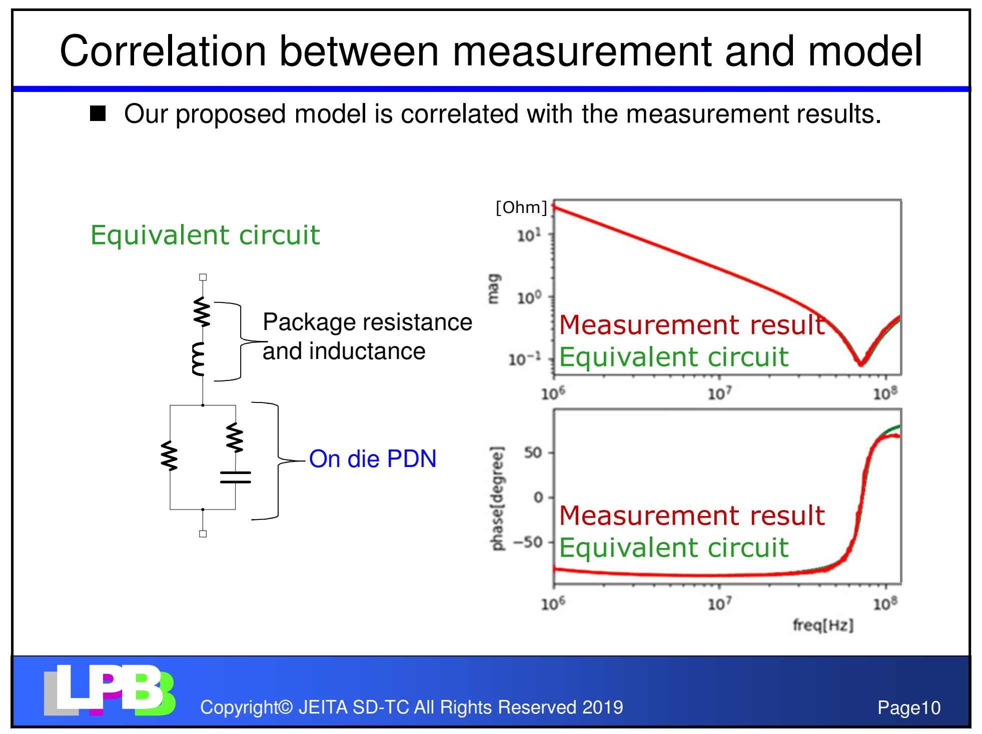


Copyright© JEITA SD-TC All Rights Reserved 2019

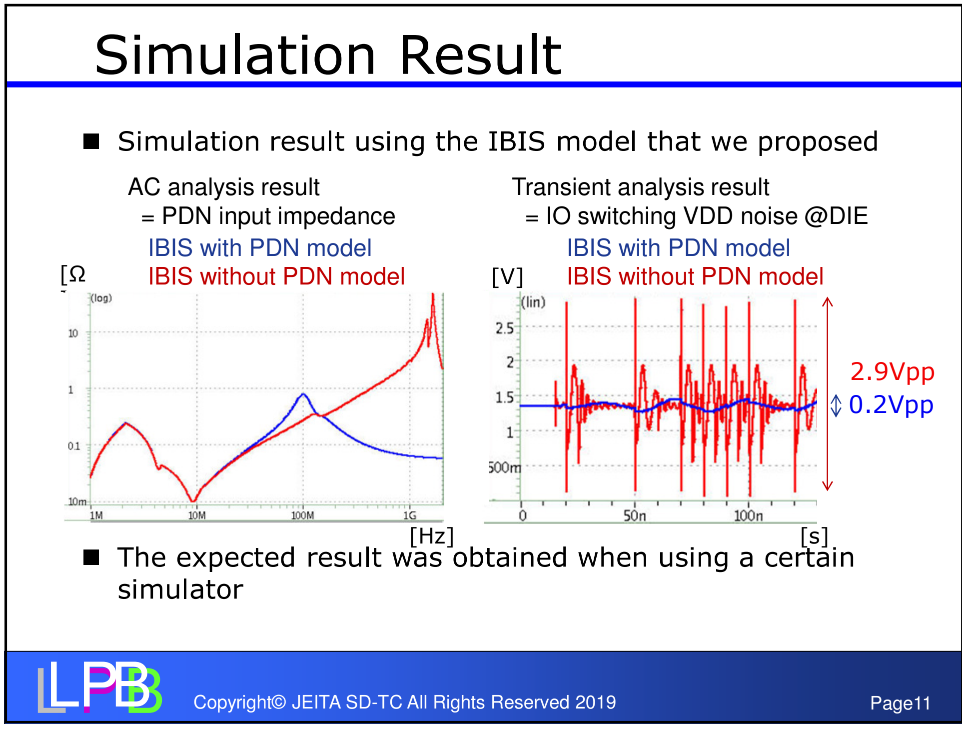
Page8



Proposal
Model
New Keyword
VCC
bus_label 2
On die Resistance
R pdn
Leak current
R leak
On die De-cap
C pdn
bus_label 1
GND
[Model] OnChipDecapA
Model_type On_Die_PDN
[C pdn] 3n 2.9n 3.1n
[R pdn] 0.1 0.1 0.1
[R leak] 200 200 200
[PDN Model Mapping]
C3 A1 OnChipDecapA
D4 D1 OnChipDecapB
D3 D1 OnChipDecapC
A4 A5 model_selector_for_PSO
A little modification to existing IBIS Keyword "Series Model"
Copyright© JEITA SD-TC All Rights Reserved 2019
Page9



Correlation between measurement and model
Our proposed model is correlated with the measurement results.
Equivalent circuit
Package resistance and inductance
On die PDN
[Ohm]
mag
Measurement result
Equivalent circuit
phase[degree]
freq[Hz]
Copyright© JEITA SD-TC All Rights Reserved 2019
Page10



Agenda

- Background
- Proposal for On die De-cap model
- **Feedback and updating**
- Conclusion

Copyright© JEITA SD-TC All Rights Reserved 2019

List of syntax candidates

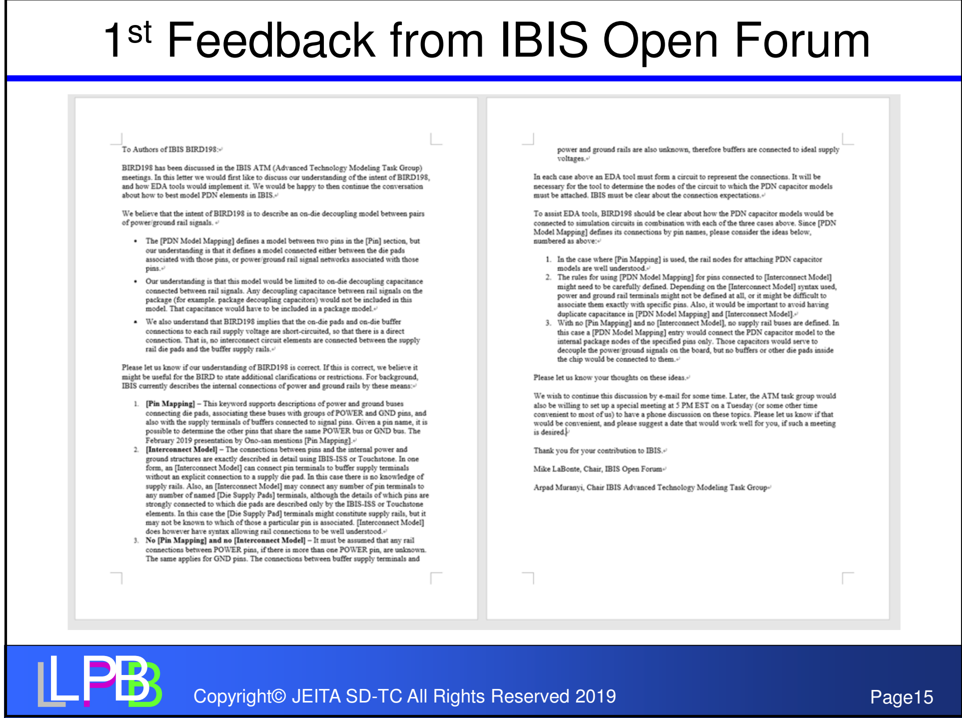
	Syntax A	Syntax B	Syntax C
	Updated BIRD198	New Proposal from IBIS Open Forum (Ex.1)	New Proposal from IBIS Open Forum (Ex.2)
Connection	Bus_label	Bus_label	Bus_label
Parent	[Model]	[Component]	[Component]
Model selecting Method	✓ [Model Selector]	✓ Alternative method	✓ Alternative method
Corner definition	The order of the values does not have to be typ / min / max	Define for C/R parameter names aligned by corner (C_pdn_corner, etc.) or not related to a corner (C_pdn, etc.).	Define typ / min / max values separately each in [PDN Model]
Base structure	Series Model	[Interconnect Model]	[Interconnect Model]
EDA Vendor	Difficult implementation	easy implementation	easy implementation

LPB Copyright© JEITA SD-TC All Rights Reserved 2019 Page13

List of syntax candidates

	Syntax A	Syntax B	Syntax C
	Updated BIRD198	New Proposal from IBIS Open Forum (Ex.1)	New Proposal from IBIS Open Forum (Ex.2)
Connection	Bus_label	Bus_label	Bus_label
Parent	[Model]	[Component]	[Component]
Model selecting Method	✓ [Model Selector]	✓ Alternative method	✓ Alternative method
Corner definition	The order of the values does not have to be typ / min / max	Define for C/R parameter names aligned by corner (C_pdn_corner, etc.) or not related to a corner (C_pdn, etc.).	Define typ / min / max values separately each in [PDN Model]
Base structure	Series Model	[Interconnect Model]	[Interconnect Model]
EDA Vendor	Difficult implementation	easy implementation	easy implementation

LPB Copyright© JEITA SD-TC All Rights Reserved 2019 Page14



To Authors of IBIS BIRD198:

BIRD198 has been discussed in the IBIS ATM (Advanced Technology Modeling Task Group) meetings. In this letter we would first like to discuss our understanding of the intent of BIRD198, and how EDA tools would implement it. We would be happy to then continue the conversation about how to best model PDN elements in IBIS.

We believe that the intent of BIRD198 is to describe an on-die decoupling model between pairs of power/ground rail signals.

- The [PDN Model Mapping] defines a model between two pins in the [Pin] section, but our understanding is that it defines a model connected either between the die pads associated with those pins, or power/ground rail signal networks associated with those pins.
- Our understanding is that this model would be limited to on-die decoupling capacitance connected between rail signals. Any decoupling capacitance between rail signals on the package (for example. package decoupling capacitors) would not be included in this model. That capacitance would have to be included in a package model.
- We also understand that BIRD198 implies that the on-die pads and on-die buffer connections to each rail supply voltage are short-circuited, so that there is a direct connection. That is, no interconnect circuit elements are connected between the supply rail die pads and the buffer supply rails.

Please let us know if our understanding of BIRD198 is correct. If this is correct, we believe it might be useful for the BIRD to state additional clarifications or restrictions. For background, IBIS currently describes the internal connections of power and ground rails by these means:

1. **[Pin Mapping]** – This keyword supports descriptions of power and ground buses connecting die pads, associating these buses with groups of POWER and GND pins, and also with the supply terminals of buffers connected to signal pins. Given a pin name, it is possible to determine the other pins that share the same POWER bus or GND bus. The February 2019 presentation by Ono-san mentions [Pin Mapping].
2. **[Interconnect Model]** – The connections between pins and the internal power and ground structures are exactly described in detail using IBIS-ISS or Touchstone. In one form, an [Interconnect Model] can connect pin terminals to buffer supply terminals without an explicit connection to a supply die pad. In this case there is no knowledge of supply rails. Also, an [Interconnect Model] may connect any number of pin terminals to any number of named [Die Supply Pads] terminals, although the details of which pins are strongly connected to which die pads are described only by the IBIS-ISS or Touchstone elements. In this case the [Die Supply Pad] terminals might constitute supply rails, but it may not be known to which of those a particular pin is associated. [Interconnect Model] does however have syntax allowing rail connections to be well understood.
3. **No [Pin Mapping] and no [Interconnect Model]** – It must be assumed that any rail connections between POWER pins, if there is more than one POWER pin, are unknown. The same applies for GND pins. The connections between buffer supply terminals and power and ground rails are also unknown, therefore buffers are connected to ideal supply voltages.

In each case above an EDA tool must form a circuit to represent the connections. It will be necessary for the tool to determine the nodes of the circuit to which the PDN capacitor models must be attached. IBIS must be clear about the connection expectations.

To assist EDA tools, BIRD198 should be clear about how the PDN capacitor models would be connected to simulation circuits in combination with each of the three cases above. Since [PDN Model Mapping] defines its connections by pin names, please consider the ideas below, numbered as above:

1. In the case where [Pin Mapping] is used, the rail nodes for attaching PDN capacitor models are well understood.
2. The rules for using [PDN Model Mapping] for pins connected to [Interconnect Model] might need to be carefully defined. Depending on the [Interconnect Model] syntax used, power and ground rail terminals might not be defined at all, or it might be difficult to associate them exactly with specific pins. Also, it would be important to avoid having duplicate capacitance in [PDN Model Mapping] and [Interconnect Model].
3. With no [Pin Mapping] and no [Interconnect Model], no supply rail buses are defined. In this case a [PDN Model Mapping] entry would connect the PDN capacitor model to the internal package nodes of the specified pins only. Those capacitors would serve to decouple the power/ground signals on the board, but no buffers or other die pads inside the chip would be connected to them.

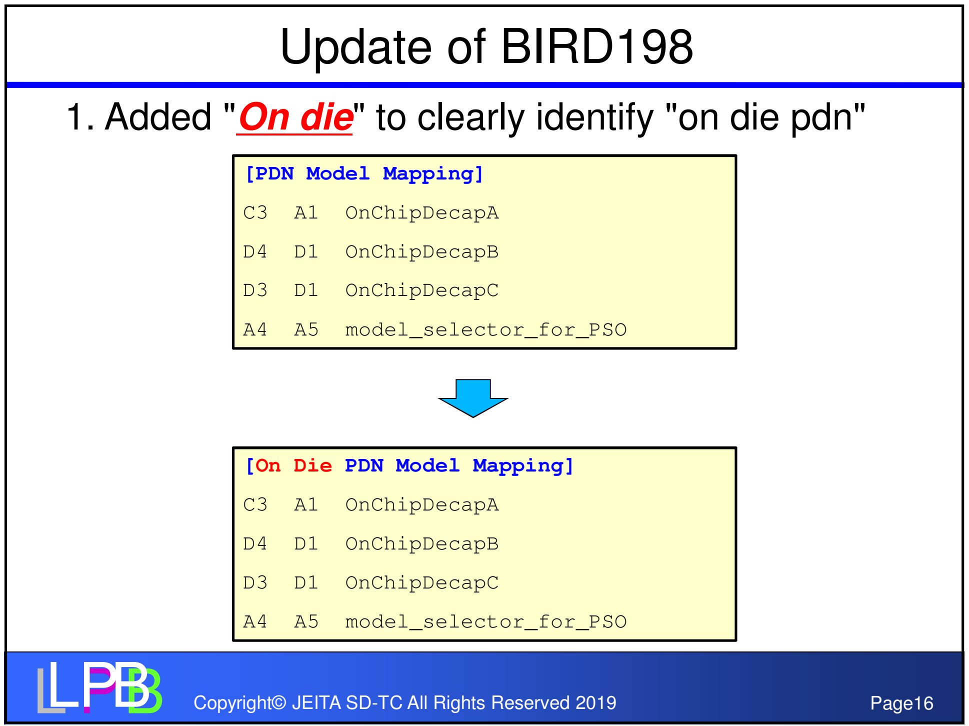
Please let us know your thoughts on these ideas.

We wish to continue this discussion by e-mail for some time. Later, the ATM task group would also be willing to set up a special meeting at 5 PM EST on a Tuesday (or some other time convenient to most of us) to have a phone discussion on these topics. Please let us know if that would be convenient, and please suggest a date that would work well for you, if such a meeting is desired.

Thank you for your contribution to IBIS.

Mike LaBonte, Chair, IBIS Open Forum

Arpad Muranyi, Chair IBIS Advanced Technology Modeling Task Group



Update of BIRD198

2. Pin name → **Bus label** (required description from IBIS7.0)

```
[PDN Model Mapping]
C3   A1   OnChipDecapA
D4   D1   OnChipDecapB
D3   D1   OnChipDecapC
A4   A5   model_selector_for_PSO
```

```
[On Die PDN Model Mapping]
VDDA   VSS    OnChipDecapA
VDDB   VSSB   OnChipDecapB
VDDA   VSSB   OnChipDecapC
VDP    VSSC   model_selector_for_PSO
```

LPB

Copyright© JEITA SD-TC All Rights Reserved 2019

Update of BIRD198

3. [Model Selector] support

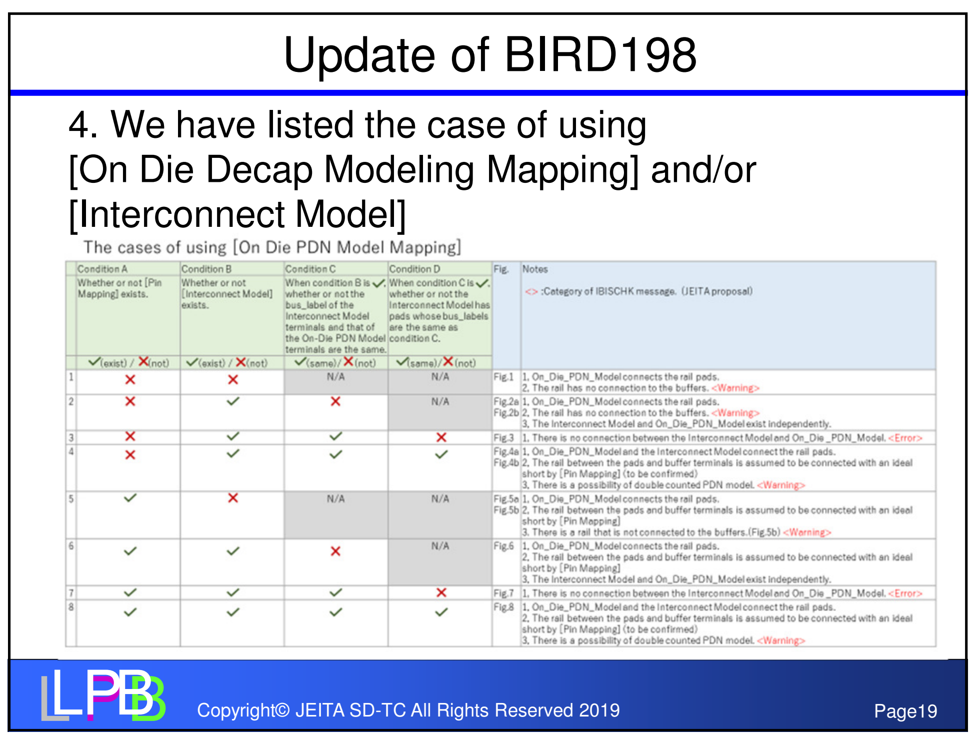
```
[Component]    AAA
    [Pin Mapping]
        pin_name1    NC             bus_label1
        pin_name2    bus_label2     NC
    [On Die PDN Model Mapping]
        bus_label1    bus_label2    DDRRAIL
[Model Selector]    DDRRAIL
    DDR3_mode
    DDR4_mode
[Model]    DDR3_mode
    Model_Type    On_Die_PDN
    [C pdn]    3.0n    3.6n    2.1n
    [R pdn]    0.02    0.03    0.01
    [R leak]   15k     15k     15k
[Model]    DDR4_mode
    Model_Type    On_Die_PDN
    [C pdn]    2.0n    2.5n    0.9n
    [R pdn]    0.02    0.03    0.01
    [R leak]   15k     15k     15k
```

Almost the same as "Series model“

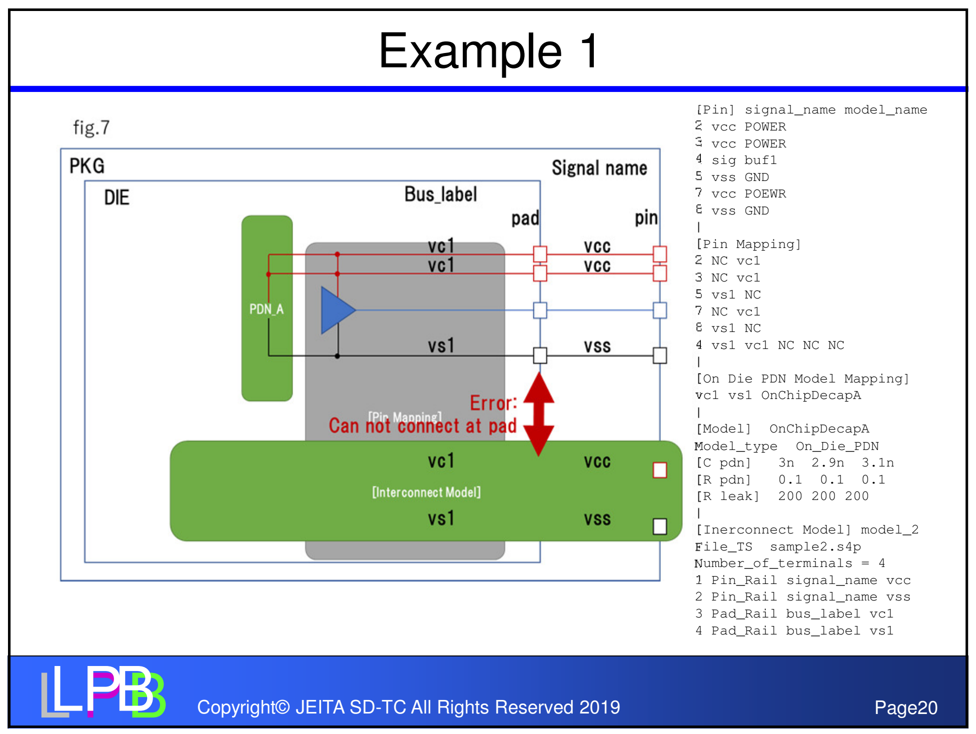
The order of the values does not have to be typ / min / max

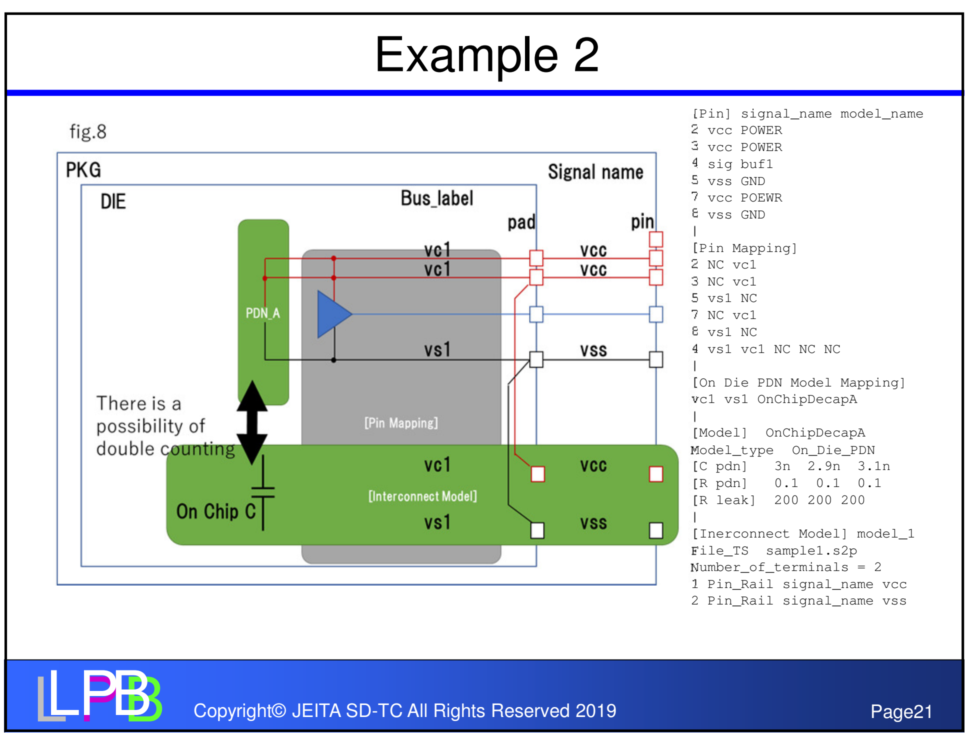
LPB

Copyright© JEITA SD-TC All Rights Reserved 2019



	Condition A	Condition B	Condition C	Condition D	Fig.	Notes
	Whether or not [Pin Mapping] exists.	Whether or not [Interconnect Model] exists.	When condition B is ✓, whether or not the bus_label of the Interconnect Model terminals and that of the On-Die PDN Model terminals are the same.	When condition C is ✓, whether or not the Interconnect Model has pads whose bus_labels are the same as condition C.		<> :Category of IBISCHK message. (JEITA proposal)
	✓(exist) / ✗(not)	✓(exist) / ✗(not)	✓(same)/ ✗(not)	✓(same)/ ✗(not)		
1	✗	✗	N/A	N/A	Fig.1	1. On_Die_PDN_Model connects the rail pads. 2. The rail has no connection to the buffers. <Warning>
2	✗	✓	✗	N/A	Fig.2a Fig.2b	1. On_Die_PDN_Model connects the rail pads. 2. The rail has no connection to the buffers. <Warning> 3. The Interconnect Model and On_Die_PDN_Model exist independently.
3	✗	✓	✓	✗	Fig.3	1. There is no connection between the Interconnect Model and On_Die _PDN_Model. <Error>
4	✗	✓	✓	✓	Fig.4a Fig.4b	1. On_Die_PDN_Model and the Interconnect Model connect the rail pads. 2. The rail between the pads and buffer terminals is assumed to be connected with an ideal short by [Pin Mapping] (to be confirmed) 3. There is a possibility of double counted PDN model. <Warning>
5	✓	✗	N/A	N/A	Fig.5a Fig.5b	1. On_Die_PDN_Model connects the rail pads. 2. The rail between the pads and buffer terminals is assumed to be connected with an ideal short by [Pin Mapping] 3. There is a rail that is not connected to the buffers.(Fig.5b) <Warning>
6	✓	✓	✗	N/A	Fig.6	1. On_Die_PDN_Model connects the rail pads. 2. The rail between the pads and buffer terminals is assumed to be connected with an ideal short by [Pin Mapping] 3. The Interconnect Model and On_Die_PDN_Model exist independently.
7	✓	✓	✓	✗	Fig.7	1. There is no connection between the Interconnect Model and On_Die _PDN_Model. <Error>
8	✓	✓	✓	✓	Fig.8	1. On_Die_PDN_Model and the Interconnect Model connect the rail pads. 2. The rail between the pads and buffer terminals is assumed to be connected with an ideal short by [Pin Mapping] (to be confirmed) 3. There is a possibility of double counted PDN model. <Warning>





List of syntax candidates

	Syntax A	Syntax B	Syntax C
	Updated BIRD198	New Proposal from IBIS Open Forum (Ex.1)	New Proposal from IBIS Open Forum (Ex.2)
Connection	Bus_label	Bus_label	Bus_label
Parent	[Model]	[Component]	[Component]
Model selecting Method	✓ [Model Selector]	✓ Alternative method	✓ Alternative method
Corner definition	The order of the values does not have to be typ / min / max	Define for C/R parameter names aligned by corner (C_pdn_corner, etc.) or not related to a corner (C_pdn, etc.).	Define typ / min / max values separately each in [PDN Model]
Base structure	Series Model	[Interconnect Model]	[Interconnect Model]
EDA Vendor	Difficult implementation	easy implementation	easy implementation

LPB

Copyright© JEITA SD-TC All Rights Reserved 2019

Page22

2nd Feedback from IBIS Open Forum

We were very impressed with your detailed solutions to address previous comments as well as your thorough descriptions of BIRD198 and BIRD189 interactions in the PowerPoint document. We have now had two good discussions on the BIRD198.1 draft proposal. I will attempt to summarize our questions, comments, and an alternate syntax idea proposed by Walter Katz.

Questions/comments:

1. We are wondering why the BIRD allows use of [Model Selector] for the [Model] name included in the [On Die PDN Model Mapping] keyword. Is this for consistency with all other [Model] types or is there a real technical need for it? If the latter, do you have an example for where more than one selection of an On Die PDN Model could be useful?
2. Are the [R pdn], [C pdn], [R leak] and [R pdn corner], [C pdn corner], [R leak corner] keywords included for consistency with the existing structures for C_comp modeling ([Model] C_comp* subparameters vs. [C Comp Corner] C_comp* subparameters)? We think it would be simpler to have only one method of including these keywords. The 'corner' method to associate the values with the typ/min/max corners rather than by magnitude seems like the better approach to ensure consistent use of the model in simulation.
3. Interactions between BIRD189 and BIRD198 were discussed. There was agreement that allowing both to co-exist would simplify rules and IBISCHK parsing. Language could be added to the BIRD to clarify that it is the burden of the model maker to ensure that on-die decoupling is not double counted. The examples in Fig. 3 and Fig. 7 of the bird198p1_fig_20190820.pptx document would not be errors in this case. These cases could be real examples where a model maker is modeling on-package decoupling with BIRD189 syntax and on-die decoupling with BIRD198 syntax.
4. Requiring the existence of [Pin Mapping] seems appropriate and would simplify parser checking.

Some of the EDA vendors expressed their opposition to the addition of a new [Model] type to represent the on-die PDN model. Implementing a new type of [Model] in existing EDA software is rather difficult, requiring major code changes, schematic symbol changes, GUI changes, etc. Walter Katz proposed a simplified alternative syntax which would place the on-die PDN models under the scope of the [Component] keyword with the addition of a few simple keywords, such as [R pdn], [C pdn], [R leak]. This appears to be easier to implement and support in EDA tools. Putting the keywords under the [Component] scope is also good because (unlike [Model]) this structure is bus_label centric, not pin-centric.

Walter's draft syntax proposal looks like this:

```
[On Die PDN Models]

[PDN Model] VDDAVSS
[Rail Bus Labels]  VDDA VSS    | (Note) Bus_Labels can be Rail signal_names
[C pdn]  3n   2.9n  3.1
[R pdn]  0.1  0.1   0.1
[R leak] 200  200   200
[End PDN Model]

[PDN Model] VDDBVSS
[Rail Bus Labels]  VDDB VSS
[C pdn]  3n   3.1n  2.9n
[R pdn]  0.1  0.1   0.1
[R leak] 200  200   200
[End PDN Model]
```

A new syntax proposal from the IBIS Open Forum for easy implementation by EDA vendors.

Copyright© JEITA SD-TC All Rights Reserved 2019

3rd Feedback from IBIS Open Forum

We have had a lot of discussion about the meaning of corner cases for the C_pdn, R_pdn, and R_leak parameters. In my experience, there is not typically a correlation between the PDN corner parameters and the transistor corner parameters. The PDN decoupling capacitance can be fabricated with many technologies such as MOS cap, MIM cap, DRAM storage cap, etc. So, the min/max values of the PDN capacitance usually are not related to the same slow/fast (min/max) transistor process corners. It's also difficult to say what becomes the best/worst case model for the PDN, since this can have a lot to do with the resonant frequency of the PDN C with package L, and what frequency the buffer is switching at. For example, in a SSO simulation, you might need to sweep all the PDN corners with the slow/fast transistor model corners to see what corner case generates the worst simultaneous switching noise.

So, we think it is necessary to include syntax supporting:

1. A PDN model with C_pdn, R_pdn, and R_leak parameters for 3 corners, where the corners are correlated with the Model typ/min/max corners.
2. Multiple PDN models (like the Model Selector concept) with single C_pdn, R_pdn, and R_leak parameter values (not supporting corners, not correlated to Model typ/min/max corners). The EDA tool would see these models as selected by group.

We also discussed another syntax proposal from Walter that would align better to the BIRD189 syntax. We would like your feedback on the idea presented below:

Notes:

1. The [PDN Group] is scoped under [Component].
2. Multiple [PDN Model] sections can exist with a [PDN Group]/[End PDN Group] section, for example to model VDD-VSS and VDDQ-VSS.
3. There is different syntax for C/R parameter names aligned by corner (C_pdn_corner, etc.) or not related to a corner (C_pdn, etc.).
4. If there are "corners" not correlated with process, then we can have one [PDN Group] for each of these uncorrelated "corners". There could be 1 PDN corner, 2 PDN corners, 3 PDN corners, and more than 3 PDN corners (implemented as separate [PDN Group]s).
5. This syntax also changes some keywords to subparameters within the [PDN Model]/[End PDN Model] section.
6. The EDA tool would have a single PDN Group selector. Once any group is selected then all is automatic.

```
| Example 1, one group correlated with typ/slow/fast IV/VT
curves - one group, three corners
|-------------------------------------------------------------
----------------------------
[PDN Group] ProcessCorners
[PDN Model] VDDVSS_Corner
Rail_Bus_Labels VDD VSS
C_pdn_corner    100f   150f   50f
R_pdn_corner     0.1   0.05   0.15
R_leak_corner    200   300    100
[End PDN Model]
[End PDN Group]


| Example 2, two groups, not correlated with process corners
|-------------------------------------------------------------
----------------------------
[PDN Group] LargeCap
[PDN Model] VDDVSS_LargeCap
Rail_Bus_Labels VDD VSS
C_pdn = 150f
R_pdn = 0.05
R_leak = 300
[End PDN Model]
[End PDN Group]

[PDN Group] SmallCap
[PDN Model] VDDVSS_SmallCap
Rail_Bus_Labels VDD VSS
C_pdn = 50f
R_pdn = 0.15
R_leak = 100
[End PDN Model]
[End PDN Group]
```

Copyright© JEITA SD-TC All Rights Reserved 2019

3rd Feedback from IBIS Open Forum

Syntax B: 3rd feedback (Example 1)

```
[Component]    AAA
    [PDN Group] PDN_for_DDR3
        [PDN Model] VDDVSS_for_Core
            Rail_Bus_Labels VDD VSS
            C_pdn_corner     100n    150n    50n
            R_pdn_corner      0.1    0.05    0.15
            R_leak_corner     200     300    100
        [End PDN Model]
        [PDN Model] VDDQVSS_for_DDRIO
            Rail_Bus_Labels VDDQ VSS
            C_pdn_corner      10n     2n    25n
            R_pdn_corner      10m    15m    5m
            R_leak_corner     500    800    50
        [End PDN Model]
    [End PDN Group]
    [PDN Group] PDN_for_DDR4
        [PDN Model] VDDVSS_for_Core
            Rail_Bus_Labels VDD VSS
…
```

1. The [PDN Group] is scoped under [Component].
2. Multiple [PDN Model] sections can exist with a [PDN Group]/[End PDN Group] section, for example to model VDD-VSS and VDDQ-VSS.
3. There is different syntax for C/R parameter names aligned by corner (C_pdn_corner, etc.) or not related to a corner (C_pdn, etc.).
4. This syntax also changes some keywords to subparameters within the [PDN Model]/[End PDN Model] section.
5. The EDA tool would have a single PDN Group selector. Once any group is selected then all is automatic.

Copyright© JEITA SD-TC All Rights Reserved 2019

Page25

3rd Feedback from IBIS Open Forum

Syntax C: 3rd feedback (Example 2)

```
[Component]    AAA
    [PDN Group] LargeCap_for_DDR3
        [PDN Model] VDDVSS_for_core
            Rail_Bus_Labels VDD VSS
            C_pdn = 150n
            R_pdn = 0.05
            R_leak = 300
        [End PDN Model]
        [PDN Model] VDDQVSS_for_DDRIO
            Rail_Bus_Labels VDDQ VSS
            C_pdn = 25n
            R_pdn = 15m
            R_leak = 800
        [End PDN Model]
    [End PDN Group]
    [PDN Group] SmallCap_for_DDR3
        [PDN Model] VDDVSS_for_core
            Rail_Bus_Labels VDD VSS
            C_pdn = 50n
…
```

1. The [PDN Group] is scoped under [Component].
2. Multiple [PDN Model] sections can exist with a [PDN Group]/[End PDN Group] section, for example to model VDD-VSS and VDDQ-VSS.
3. If there are “corners” not correlated with process, then we can have one [PDN Group] for each of these uncorrelated “corners”. There could be 1 PDN corner, 2 PDN corners, 3 PDN corners, and more than 3 PDN corners (implemented as separate [PDN Group]s).
4. This syntax also changes some keywords to subparameters within the [PDN Model]/[End PDN Model] section.
5. The EDA tool would have a single PDN Group selector. Once any group is selected then all is automatic.

LPB

Copyright© JEITA SD-TC All Rights Reserved 2019

Page26

List of syntax candidates

	Syntax A	Syntax B	Syntax C
	Updated BIRD198	New Proposal from IBIS Open Forum (Ex.1)	New Proposal from IBIS Open Forum (Ex.2)
Connection	Bus_label	Bus_label	Bus_label
Parent	[Model]	[Component]	[Component]
Model selecting Method	✓ [Model Selector]	✓ Alternative method	✓ Alternative method
Corner definition	The order of the values does not have to be typ / min / max	Define for C/R parameter names aligned by corner (C_pdn_corner, etc.) or not related to a corner (C_pdn, etc.).	Define typ / min / max values separately each in [PDN Model]
Base structure	Series Model	[Interconnect Model]	[Interconnect Model]
EDA Vendor	Difficult implementation	easy implementation	easy implementation

Copyright© JEITA SD-TC All Rights Reserved 2019

Agenda

- Background
- Proposal for On die De-cap model
- Feedback and updating
- **Conclusion**

Copyright© JEITA SD-TC All Rights Reserved 2019

Conclusion

Chip PDN model is still not widespread. Therefore, we proposed to add an explicit keyword of chip PDN to IBIS.

Our proposal was registered as BIRD198 and it has been discussing in IBIS Open Forum since this March.

We will continue to work to accept BIRD198 in the next version of IBIS.

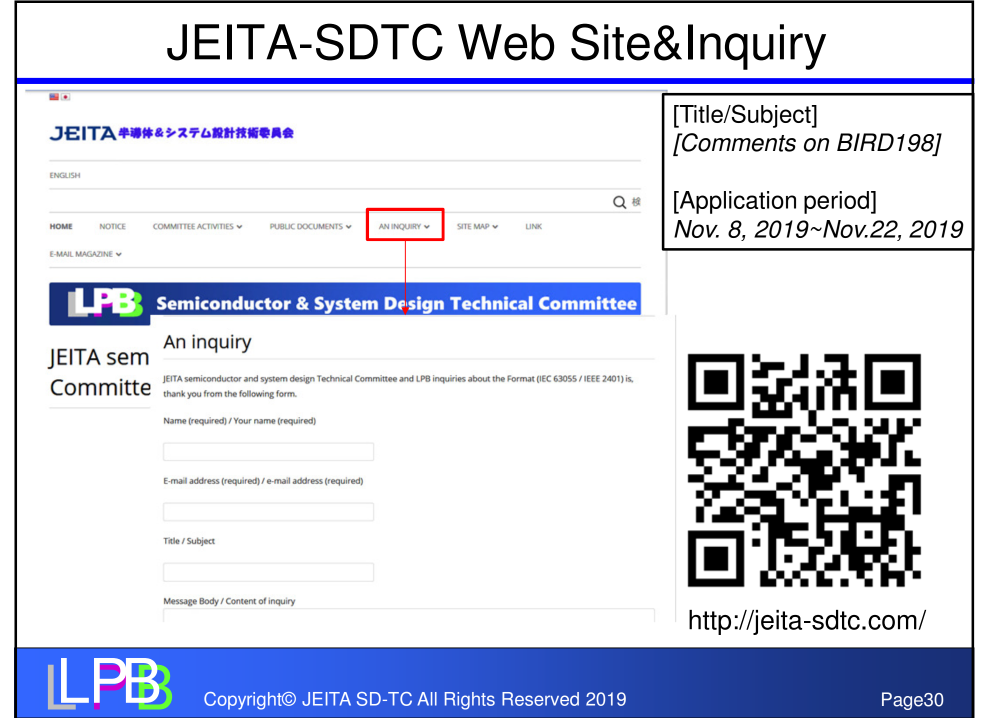
We would like to get your feedback from JAPANESE USER!

Please access “JEITA semiconductor and system design Technical Committee (JEITA-SDTC)” Web site and send comment!

Thank you!

Copyright© JEITA SD-TC All Rights Reserved 2019

JEITA-SDTC Web Site&Inquiry



Copyright© JEITA SD-TC All Rights Reserved 2019

Thank you for your support and feedback!
We really appreciate all of the IBIS Open Forum members

Copyright© JEITA SD-TC All Rights Reserved 2019

Reference: Series Model

```
[Component]   AAA
    [Pin Mapping]
        pin_name1   NC    bus_label1
        pin_name2   bus_label2   NC
    [Series Pin Mapping]
        pin_name1 pin_name2 CCC
[Model Selector]    CCC
    DDD
    EEE
[Model]   DDD
    Model_Type    Series
    [R Series]    100 80 120
     …

[Model]   EEE
    Model_Type    Series
    [R Series]    120 100 140
     …
```

Copyright© JEITA SD-TC All Rights Reserved 2019

IBIS File Format Links

Bob Ross, Teraspeed Labs
bob@teraspeedlabs.com

Asian IBIS Summit
Tokyo, Japan
November 8, 2019

(Updated from June 21, 2019 version)
(Presented by Randy Wolff, Micron Technology)

Copyright 2019 Teraspeed Labs

1

Story of IBIS

- In the beginning … (1993) 1 file format, 8 pages
- Then a committee got involved …
- (2019) … 17 or more formats or links to formats:
  - IBIS Version 7.0 (331 pages)
  - Touchstone 2.0 (34 pages)
  - IBIS-ISS (58 pages)
- Story of file formats given here

Copyright 2019 Teraspeed Labs

2

File Format Legend

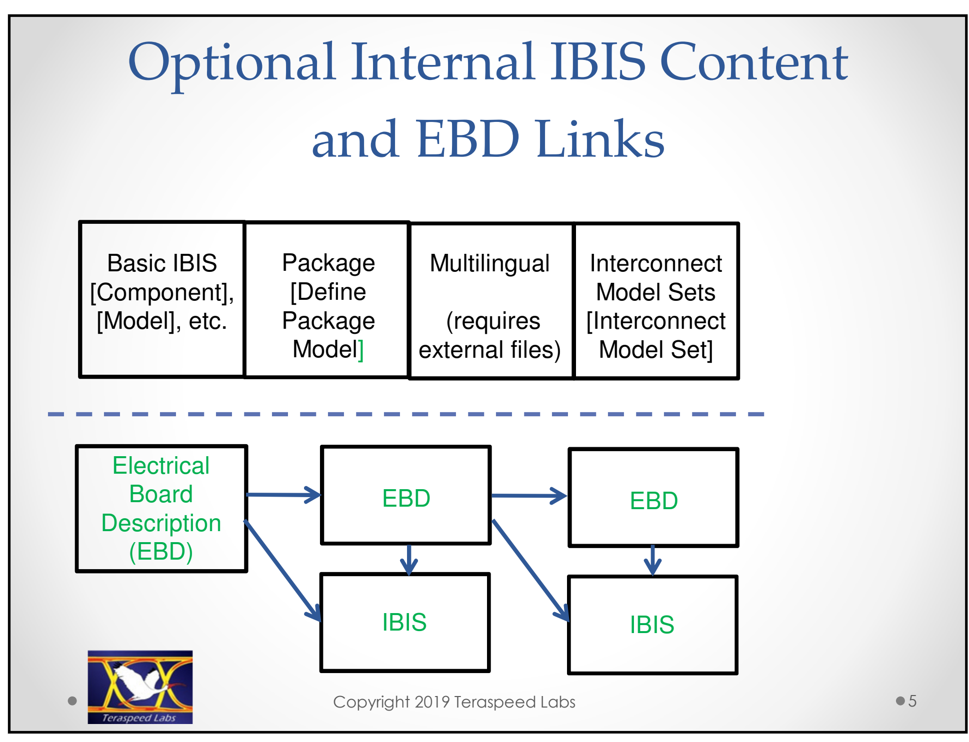
- Green – Official IBIS formats (ebd, ibs, pkg, ami, ims, Touchstone, Ts4file, executable models, “txt”)
  - Checked by ibischk7 (with/without flags) or separately with tschk2
  - Content referenced in EBD and IBIS files are usually parsed (or checked for connectivity only)
  - Note, tschk2 is an independent checker, separate from ibischk7
- Red – Official IBIS format, but no parser (IBIS-ISS)
- Black – Format managed by other specifications or standards
- Touchstone means official Touchstone 1.0 and Touchstone 2.0

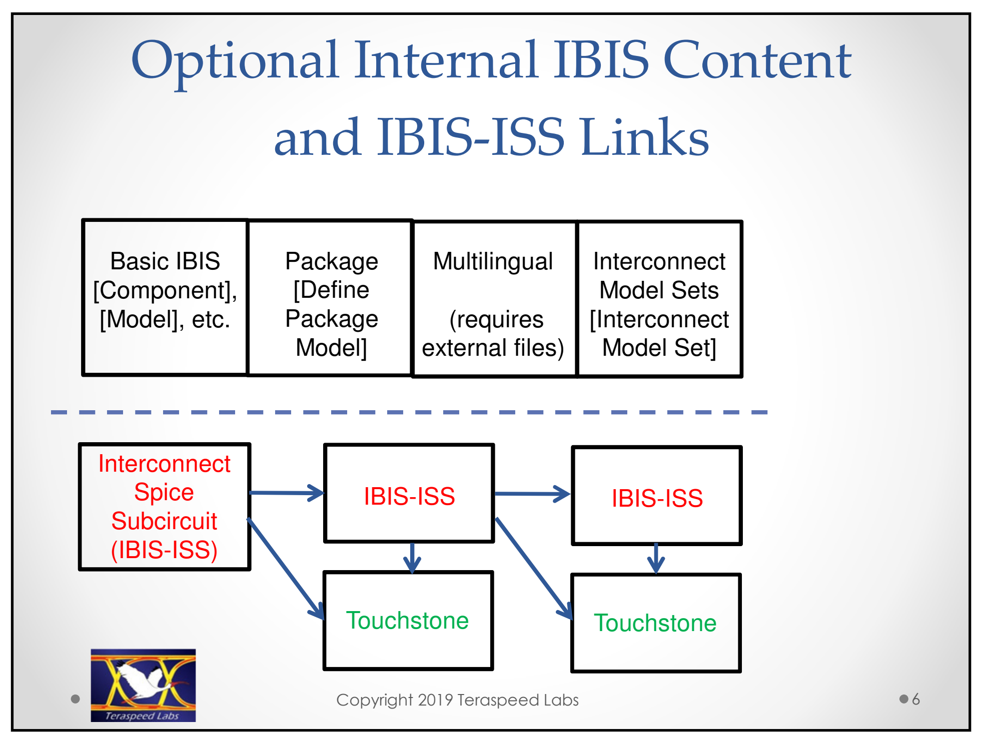
Copyright 2019 Teraspeed Labs

File Name and Extension Reference

- I/O Buffer Information Specification (IBIS) Version 7.0
  - Electrical Board Description (ebd) Section 8
  - IBIS (ibs) Sections 4-6, 12
  - Package Modeling (pkg) Section 7
  - IBIS-AMI (ami), Ts4File (usually s4p),Section 10
  - executable models (usually so, dll) Section 6
  - Interconnect Model Set (ims) Section 11
- Touchstone File Format Specification Version 2.0
  - Touchstone 1.0 (usually sNp)
  - Touchstone 2.0 (usually sNp)
  - Ts4file (usually s4p)
- IBIS Interconnect SPICE Subcircuit (IBIS-ISS) Specification Version 1.0
  - IBIS-ISS (usually iss)

Copyright 2019 Teraspeed Labs


Optional Internal IBIS Content and EBD Links
Basic IBIS [Component], [Model], etc.
Package [Define Package Model]
Multilingual (requires external files)
Interconnect Model Sets [Interconnect Model Set]
Electrical Board Description (EBD)
EBD
EBD
IBIS
IBIS
Copyright 2019 Teraspeed Labs
5


Optional Internal IBIS Content and IBIS-ISS Links
Basic IBIS [Component], [Model], etc.
Package [Define Package Model]
Multilingual (requires external files)
Interconnect Model Sets [Interconnect Model Set]
Interconnect Spice Subcircuit (IBIS-ISS)
IBIS-ISS
IBIS-ISS
Touchstone
Touchstone
Copyright 2019 Teraspeed Labs
6

Basic IBIS External File Links

Basic IBIS [Component], [Model], etc.	Package [Define Package Model]	Multilingual (requires external files)	Interconnect Model Sets [Interconnect Model Set]

ami
Ts4file (subset of Touchstone under ami)
Executable models (dll, so, etc.)

Copyright 2019 Teraspeed Labs

Optional External Package File Link

Basic IBIS [Component], [Model], etc.	Package [Define Package Model]	Multilingual (requires external files)	Interconnect Model Sets [Interconnect Model Set]

pkg

Copyright 2019 Teraspeed Labs

Multilingual External File Links

Basic IBIS [Component], [Model], etc.	Package [Define Package Model]	Multilingual (requires external files)	Interconnect Model Sets [Interconnect Model Set]

ami (for passing parameters)
"txt" (text file for passing parameters)
IBIS-ISS (can call Touchstone and other files)
SPICE (Berkeley Version 3F5)
VHDL-AMS
Verilog-AMS
VHDL-A(MS)
Verilog-A(MS)

Copyright 2019 Teraspeed Labs

Interconnect Model Set External File Links

Basic IBIS [Component], [Model], etc.	Package [Define Package Model]	Multilingual (requires external files)	Interconnect Model Sets [Interconnect Model Set]

ims
IBIS-ISS
Touchstone

Copyright 2019 Teraspeed Labs

File Formats With IBIS

- ebd
- ibs
- ami
- Executable models (dll, so, etc.)
- Ts4file
- pkg
- ami (for parameter passing)
- "txt" text format (for parameter passing)
- IBIS-ISS
- SPICE
- VHDL-AMS, Verilog-AMS, VHDL-A(MS), Verilog-A(MS)
- ims
- Touchstone 1.0, Touchstone 2.0

Copyright 2019 Teraspeed Labs 11

Example of EBD to IBIS to IMS Linkage (Without Details)

```
abc.ebd
U1.23 …
U1.24 …
[Reference Designator Map]
U1    def.ibs    DEF
```

```
def.ibs
[Component] DEF
[Pin]
23 IO1 IO_Buf
24 IO2 IO_Buf
[Interconnect Model Group]
GHI    ghi.ims
[End Interconnect Model Group]
```

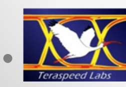
```
ghi.ims
[Interconnect Model Set] GHI
[Interconnect Model] Pin23
File_IBIS-ISS   jkl.iss  pin23
1 pin_name 23
[End Interconnect Model]
|
[Interconnect Model] Pin24
File_TS              mno.s1p
1 pin_name 24
2 A_gnd
[End Interconnect Model]
[End Interconnect Model Set]
```

EBD: Pins 23, 24 in abc.ebd → def.ibs → ghi.ims
and terminal 1 used for 23 in ghi.ims → jkl.iss
and terminal 1 used for 24 in ghi.ims → mno.s1p

```
jkl.iss
.subckt pin23 1
R_term 1 0
.ends
```

```
mno.s1p
…
0 1 0
2 0.9 0.005
…
```

ibischk7 –ebd abc.ebd checks abc.ebd, def.ibs, ghi.ims



Copyright 2019 Teraspeed Labs 12

Observations

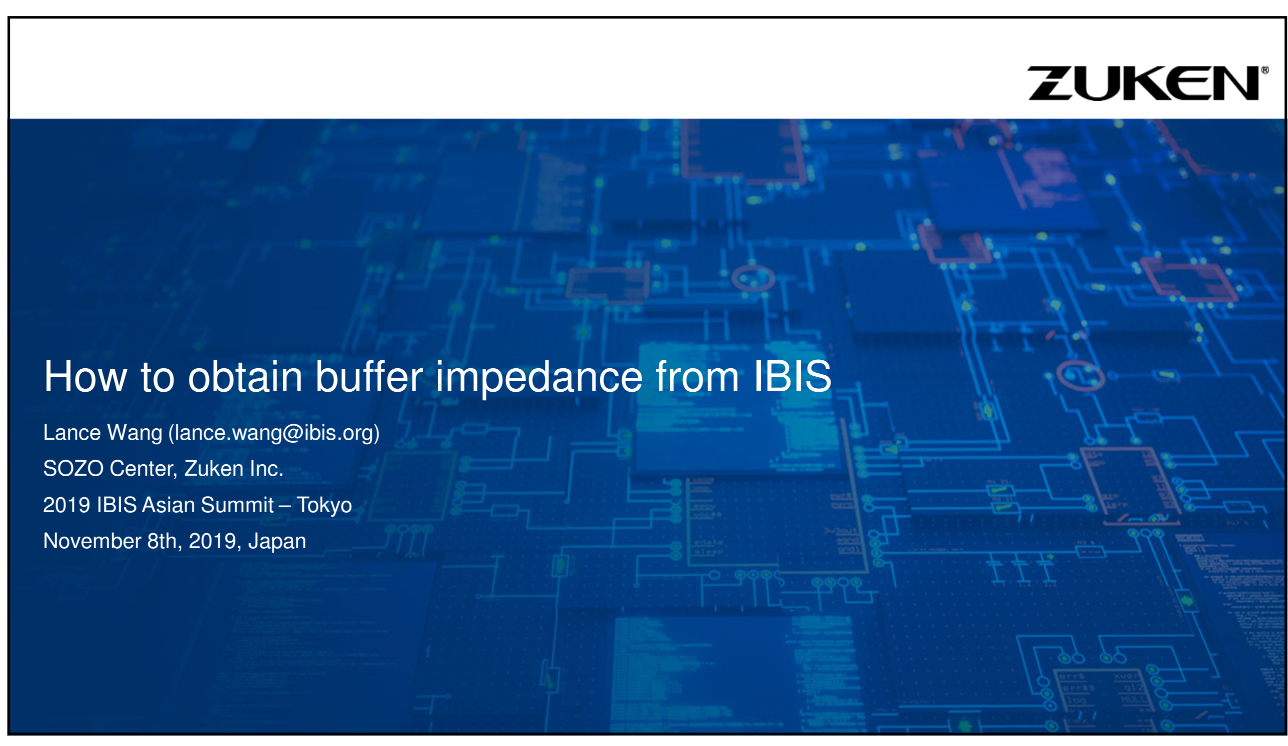
- 17 or more file format links in IBIS
- 12 or more file formats supported by IBIS Specifications or by format restrictions
  - Restrictions means requirements in certain files such as executable models, parameter passing formats and Ts4file
- ibischk7 and tschk2 check syntax and content of files
  - Individual files by flags –ebd, -pkg, -ami, -ims
  - Top level files AND linked files
  - tschk2 conversions: Touchstone 1.0 ←→ Touchstone 2.0
- Some checking or linking is not defined (e.g., to Touchstone, IBIS-ISS)

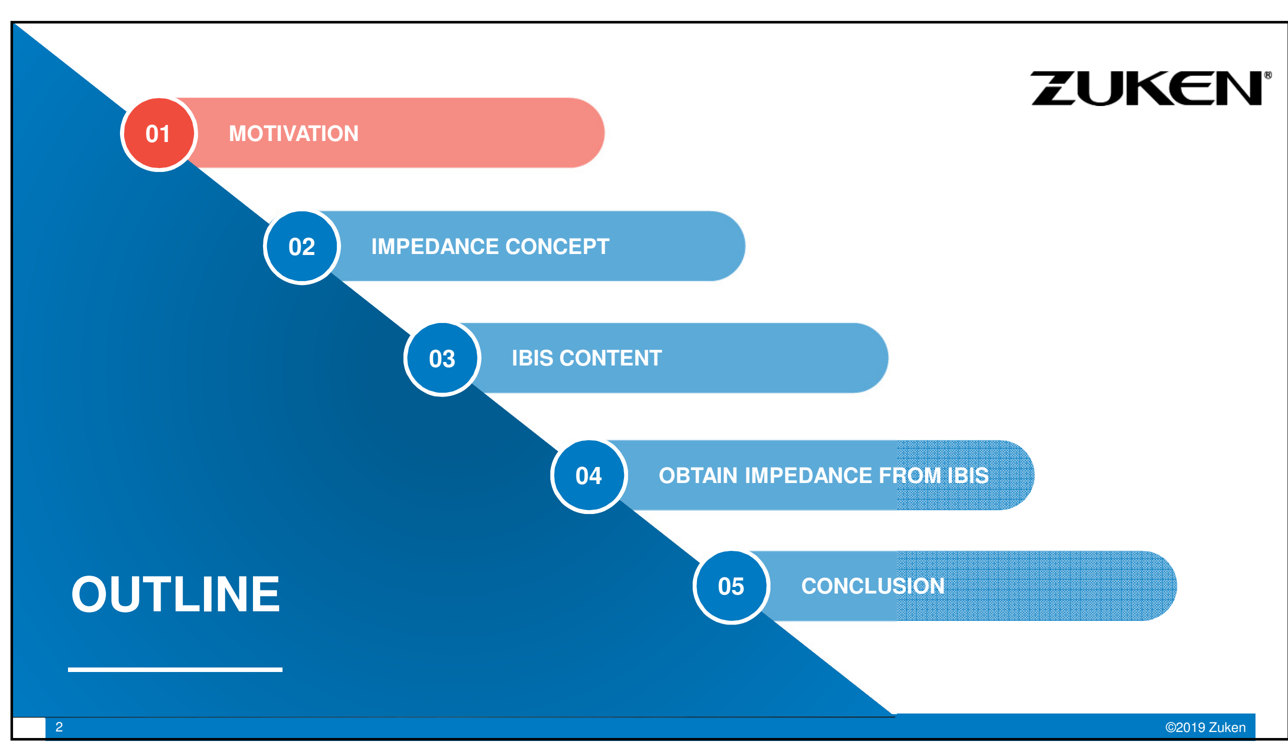
Copyright 2019 Teraspeed Labs

Past and Future File Formats

- Past (unused formats)
  - Rail Version 1.2 (ral) and railchk1 (for timing)
  - IBIS Interconnect Modeling Specification (ICM) Version 1.1 (typically icm) and icmchk1
- Possible future file formats and links
  - Electrical Module Description (EMD) with links to emd, ems, ibs, IBIS-ISS, and Touchstone
  - Touchstone advances
- A lot has happened and is happening in the IBIS Committee

Copyright 2019 Teraspeed Labs


ZUKEN
How to obtain buffer impedance from IBIS
Lance Wang (lance.wang@ibis.org)
SOZO Center, Zuken Inc.
2019 IBIS Asian Summit – Tokyo
November 8th, 2019, Japan


ZUKEN
01 MOTIVATION
02 IMPEDANCE CONCEPT
03 IBIS CONTENT
04 OBTAIN IMPEDANCE FROM IBIS
05 CONCLUSION
OUTLINE
2
©2019 Zuken

Motivation

ZUKEN

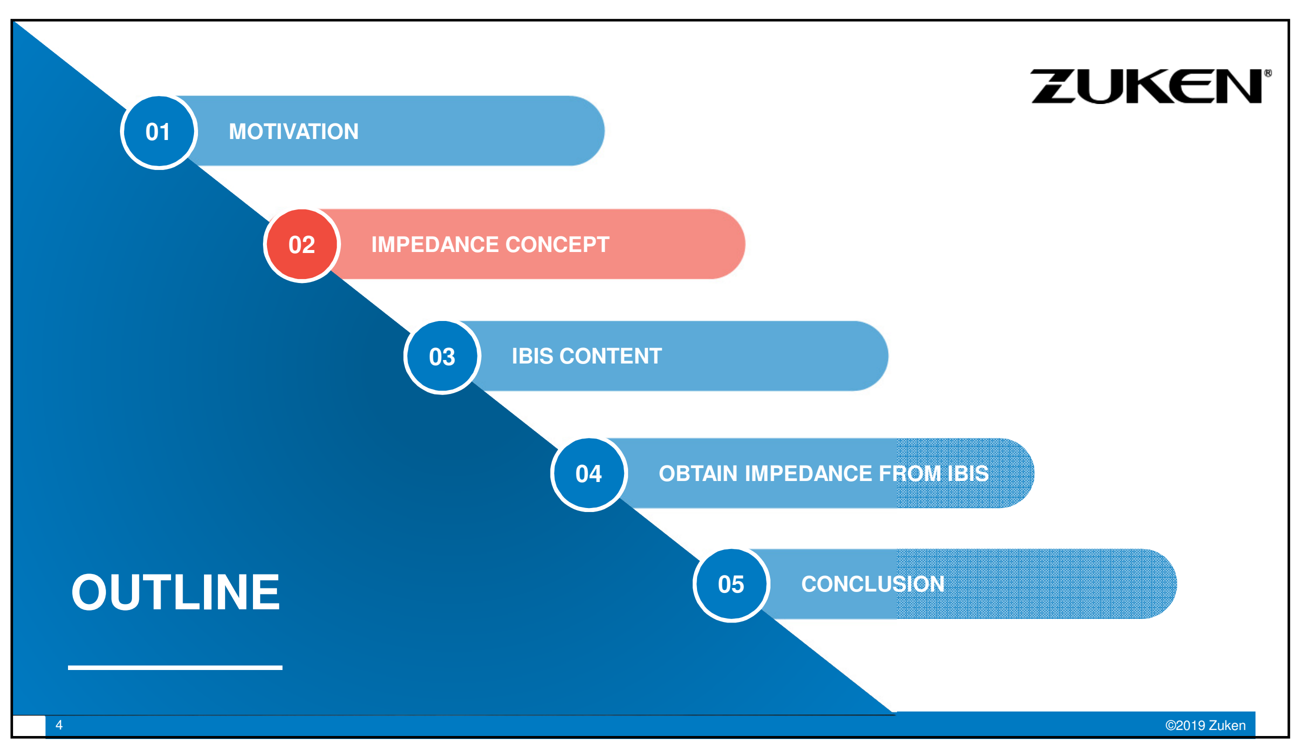
- Impedance matching is the biggest task for Signal Integrity engineer and high-speed PCB/PKG designers.
  - Unmatched impedance may cause unpredictable reflection that reduces the signal quality for high-speed circuit design.
- Interconnects, such as, trace, via, connector, package, etc., are under our radar already.
  - Field Solver helps
- Interconnect impedance also needs to match buffer Output/Input impedance in order to keep good signal quality

How to obtain I/O buffer impedance?

Matched impedance

Unmatched impedance

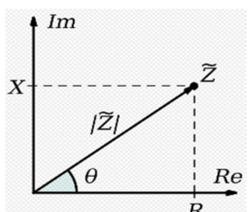
3 ©2019 Zuken



Impedance Concept

ZUKEN

- The impedance of a two-terminal circuit element is represented as a complex quantity Z. The polar form conveniently captures both magnitude and phase characteristics as $Z = |Z|e^{j\,arg(Z)}$
- where the magnitude *|Z|* represents the ratio of the voltage difference amplitude to the current amplitude, while the argument *arg(Z)* (commonly given the symbol *θ* gives the phase difference between voltage and current). *j* is the imaginary unit and is used instead of *i* in this context to avoid confusion with the symbol for electric current.
- In Cartesian form, impedance is defined as $Z = R + jX$
- where the real part of impedance is the resistance *R* and the imaginary part is the reactance *X*.



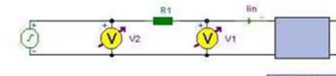
For a high-speed I/O buffer, the buffer inductance and capacitance are specially designed. It is close to minimum for the reactance X. So, in this case, the resistance R is the main factor for impedance matching.

5

©2019 Zuken

Measuring Impedance – Input Impedance

- From the AC impedance triangle, the input or output impedance of a two terminal network can be determined by measuring the small signal AC currents and voltages.
  - The voltage is measured across the input terminals and the current measured by inserting the meter in series with the signal generator.



  - An easy way to measure small input currents, is to use a fixed resistor, as in the diagram above. Measure the AC voltage at points V1 and V2, then the input current, I_{in} becomes:

$$I_{in} = \frac{V_2 - V_1}{R_1}$$

  - The input impedance Z_{in} of the circuit under test is then found by:

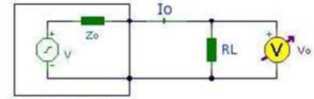
$$Z_{in} = \frac{V_1}{I_{in}}$$

6

©2019 Zuken

Measuring Impedance – Output Impedance

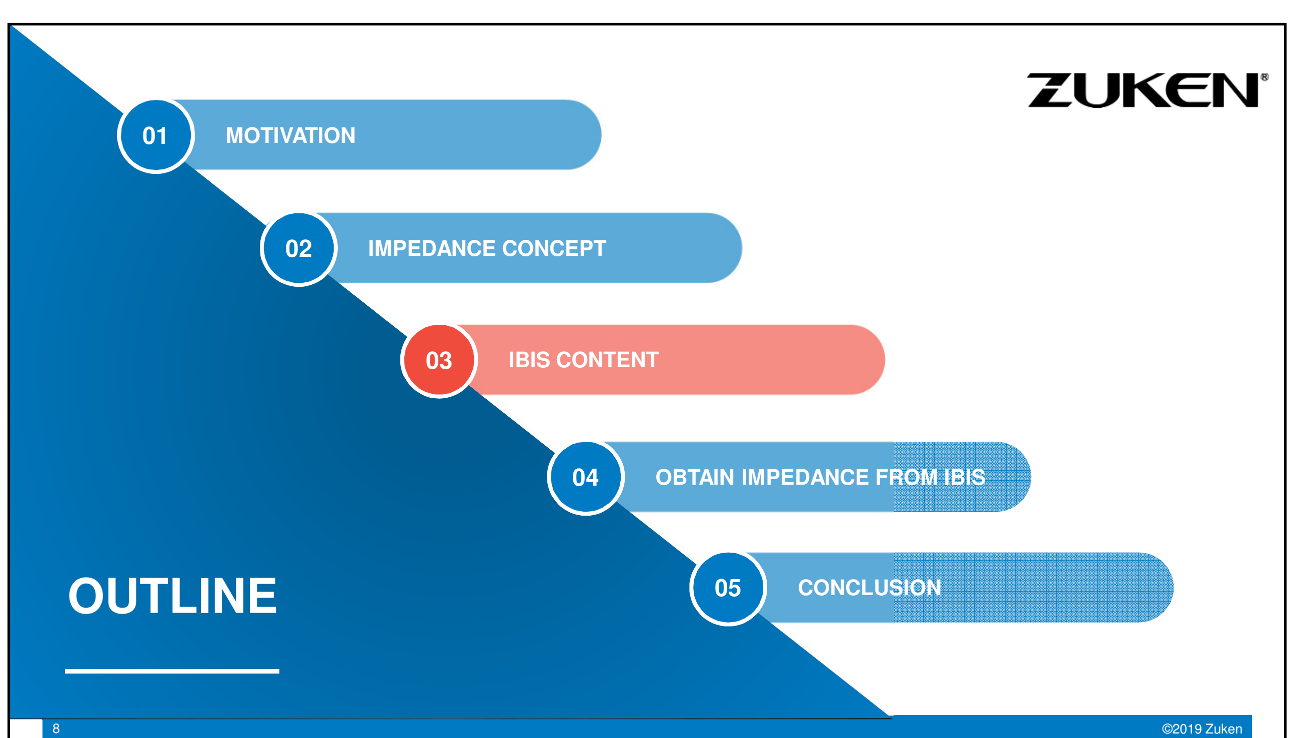
- Output impedance may also be determined using a similar technique. A fixed load resistor is used, and the output voltage is measured first with full load, then without the load.

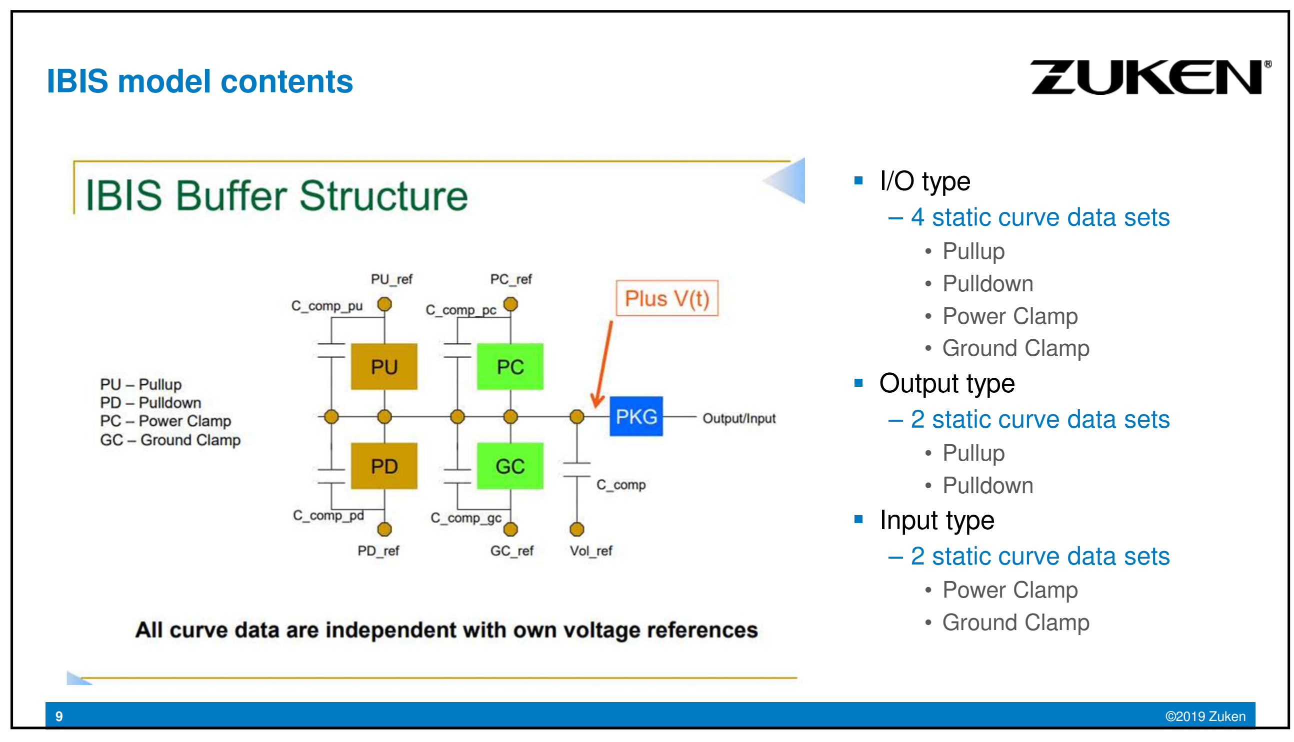


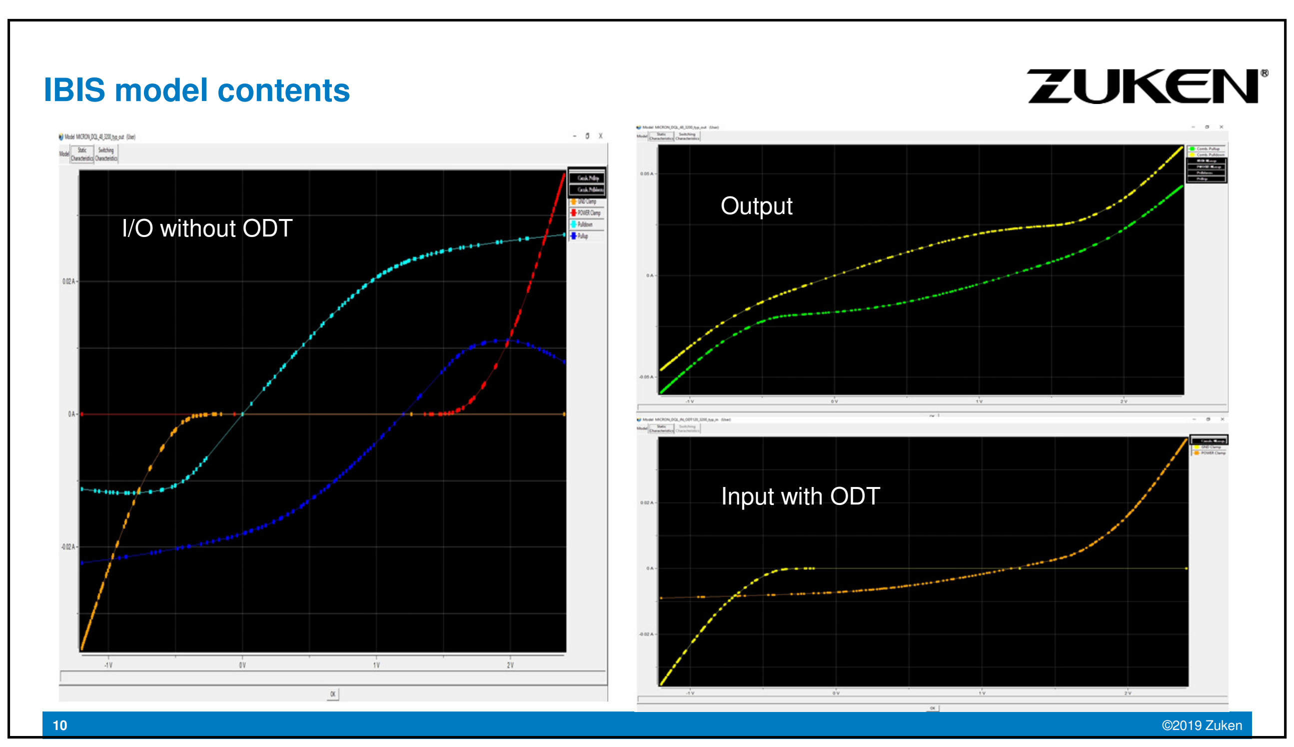
- Z_0 is the internal output impedance of the network to be measured.
- To find the output impedance the output voltage is measured first with no load resistor, then with a fixed load (purely resistive).
- First, the load resistor R_L is removed and output voltage (V) measured and recorded. Then R_L is placed back in circuit and the output voltage under load (V_L). The output impedance, Z_0 is now found by Ohm's Law for AC circuits. As the load is purely resistive $Z=V/I$, where *"V"* is voltage drop across the output impedance: (V - V_L), and *"I"* the output current, V_L/R_L. Thus:

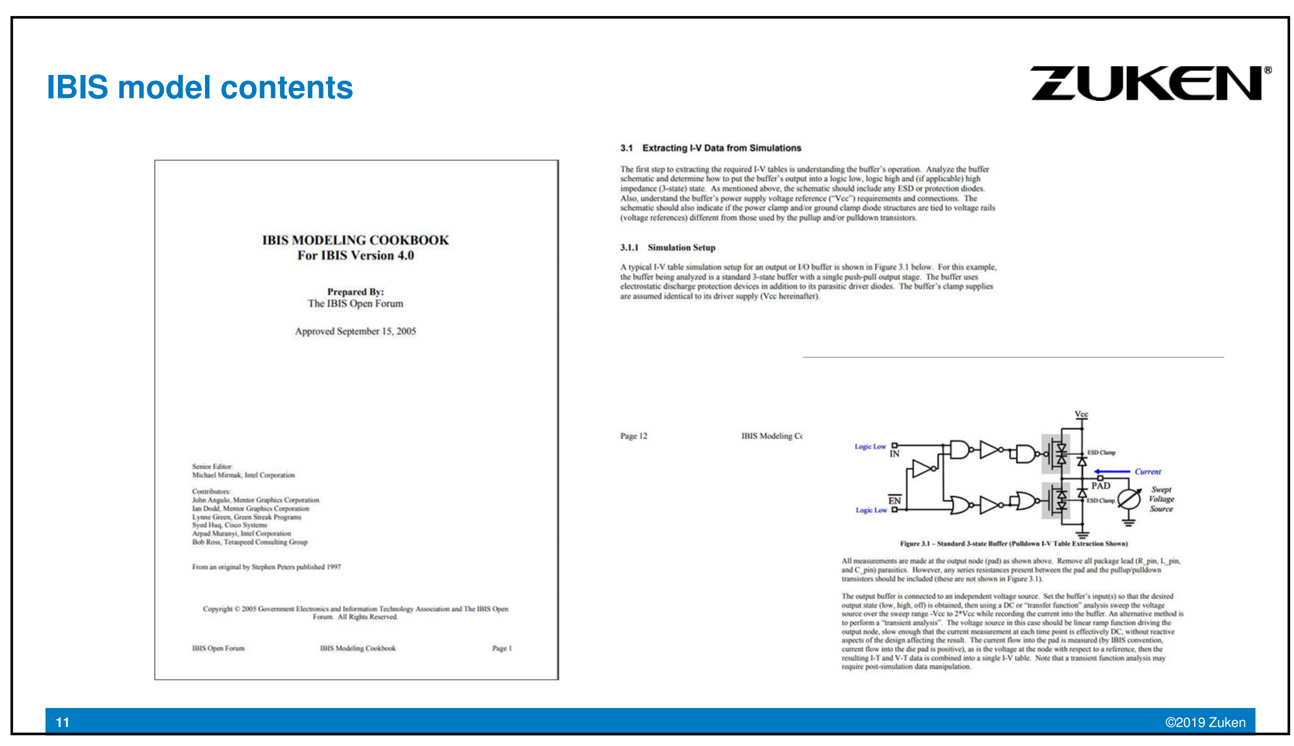
$$Z_0 = \frac{(V - V_L)}{V_L/R_L} = \frac{R_L(V - V_L)}{V_L}$$

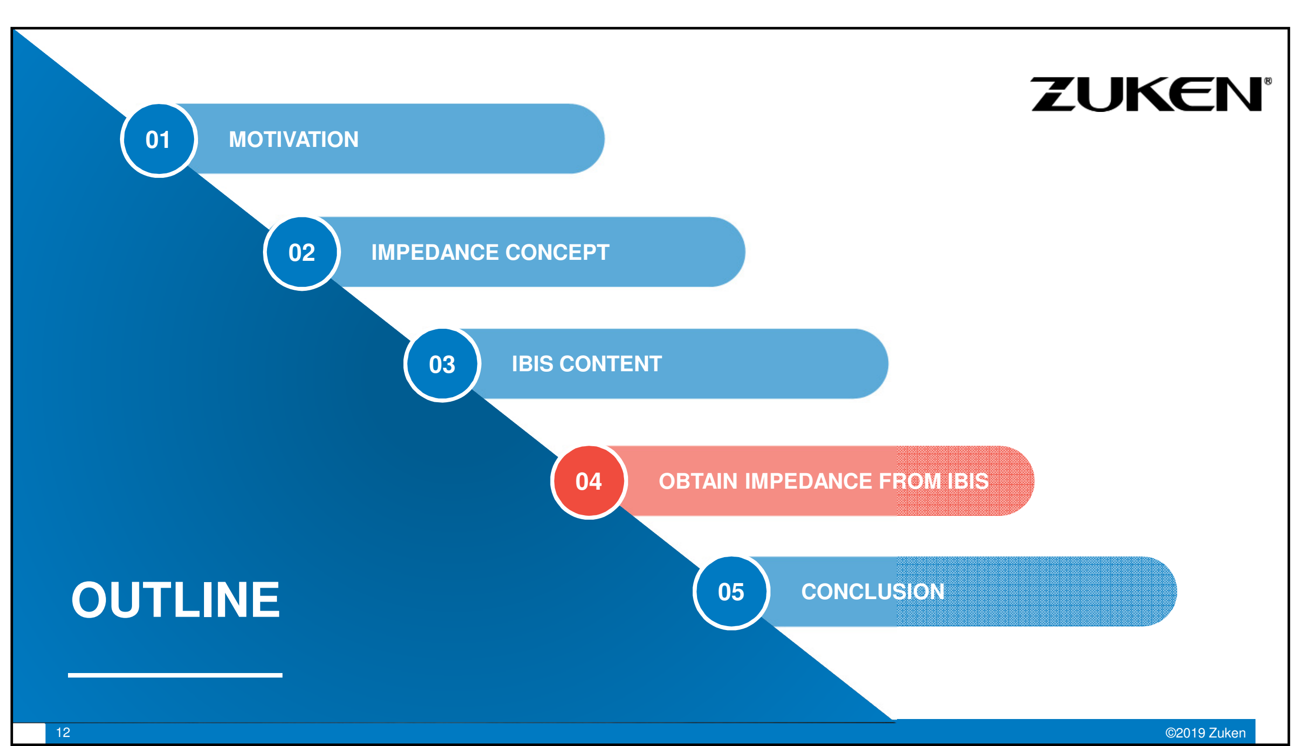
7 ©2019 Zuken

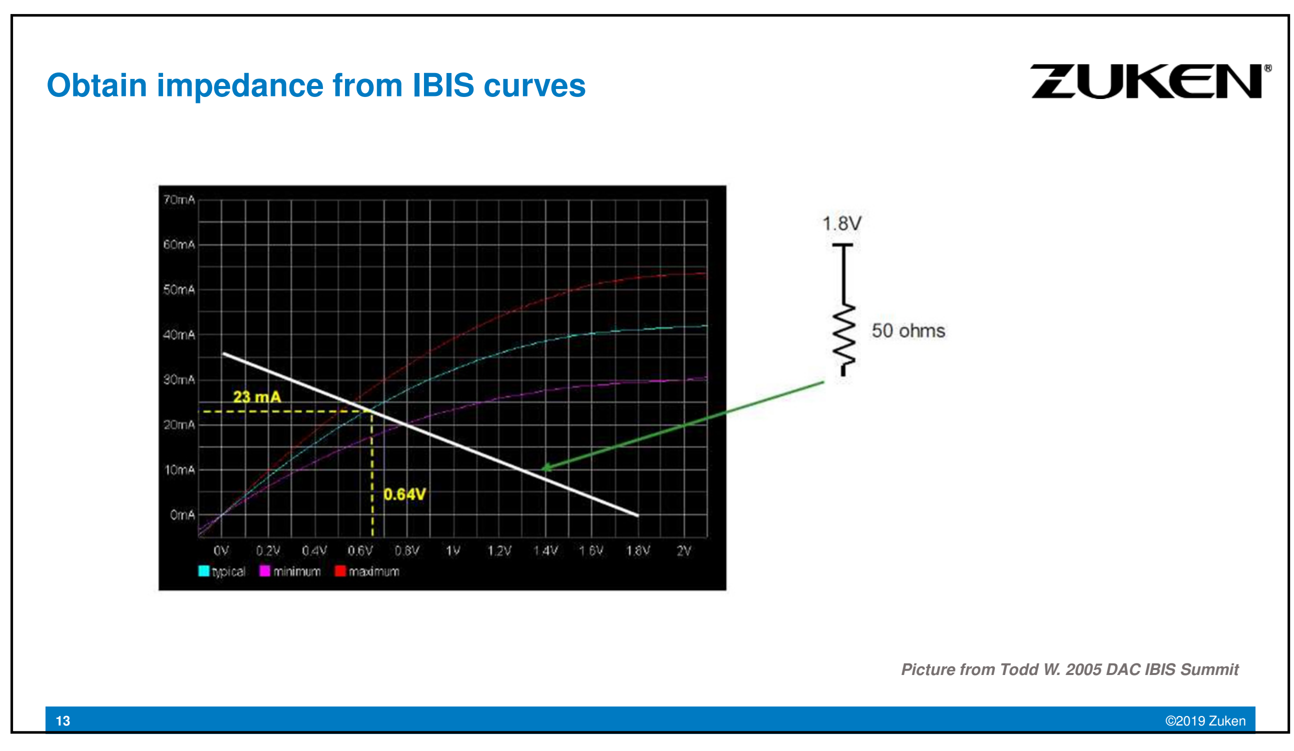


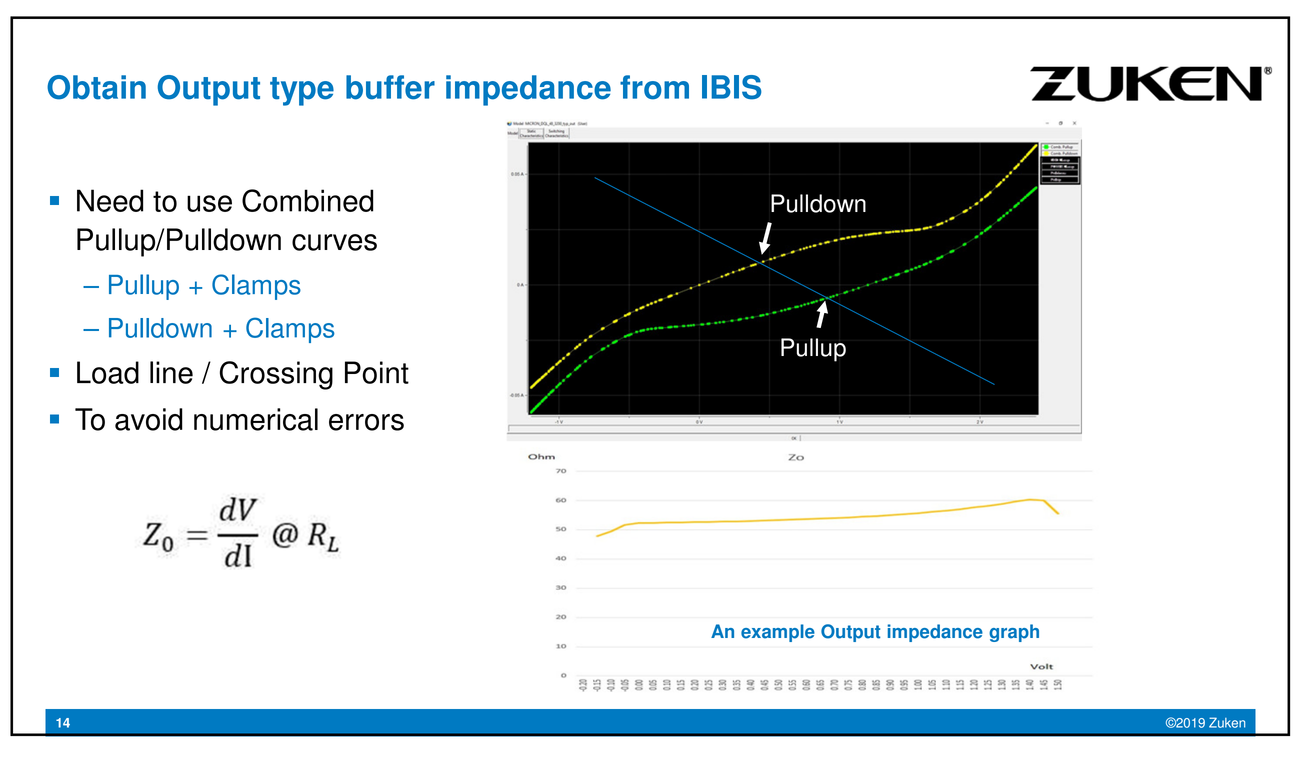

IBIS model contents
ZUKEN
IBIS Buffer Structure
PU_ref
PC_ref
C_comp_pu
C_comp_pc
Plus V(t)
PU
PC
PU – Pullup
PD – Pulldown
PC – Power Clamp
GC – Ground Clamp
PKG
Output/Input
PD
GC
C_comp
C_comp_pd
C_comp_gc
PD_ref
GC_ref
Vol_ref
All curve data are independent with own voltage references
I/O type
– 4 static curve data sets
Pullup
Pulldown
Power Clamp
Ground Clamp
Output type
– 2 static curve data sets
Pullup
Pulldown
Input type
– 2 static curve data sets
Power Clamp
Ground Clamp
9
©2019 Zuken

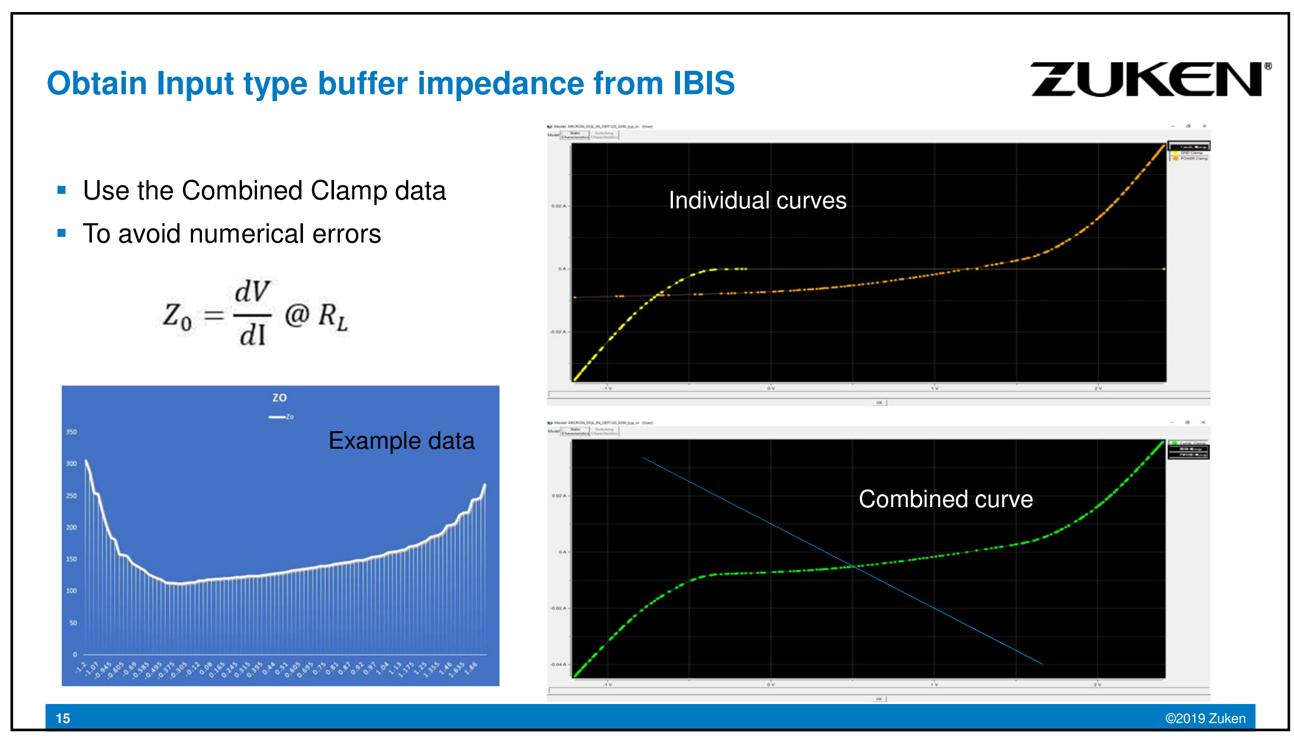

IBIS model contents
ZUKEN
I/O without ODT
Output
Input with ODT
10
©2019 Zuken

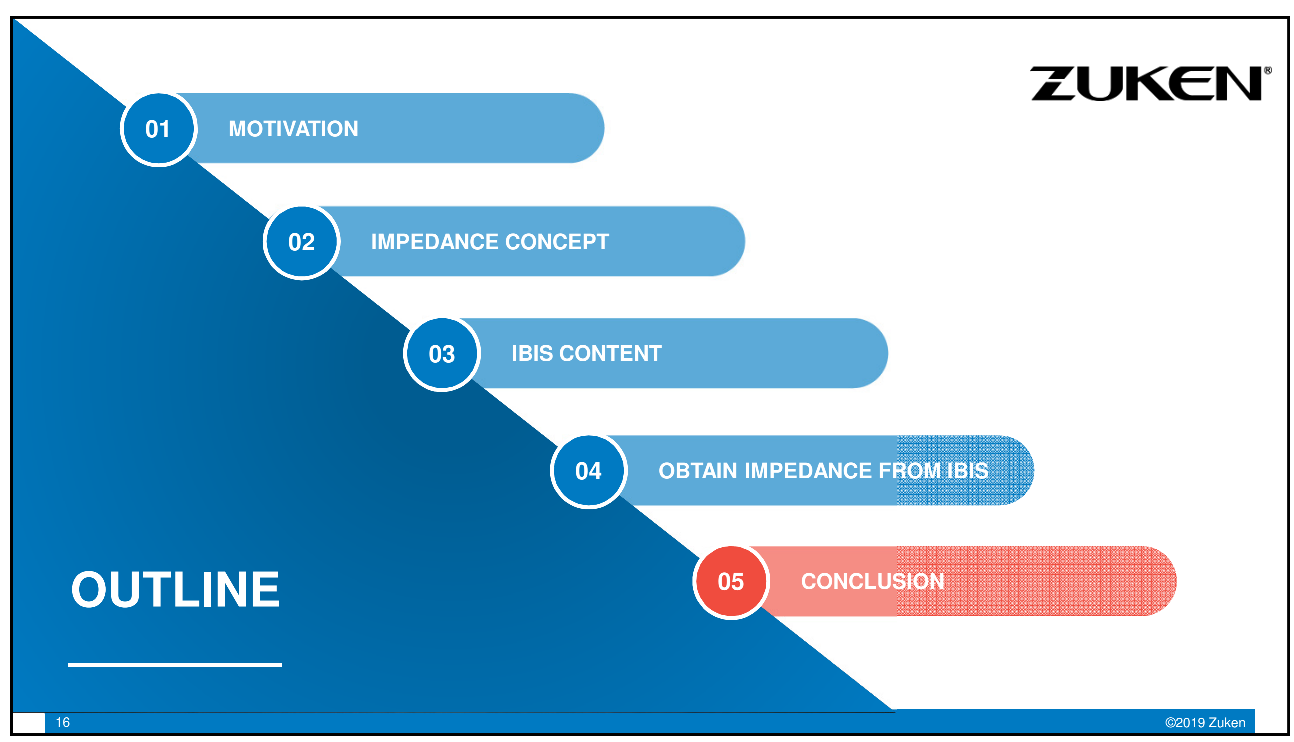

IBIS model contents
ZUKEN
IBIS MODELING COOKBOOK
For IBIS Version 4.0
Prepared By:
The IBIS Open Forum
Approved September 15, 2005
Senior Editor:
Michael Mirmak, Intel Corporation
Contributors:
John Angulo, Mentor Graphics Corporation
Ian Dodd, Mentor Graphics Corporation
Lynne Green, Green Streak Programs
Syed Huq, Cisco Systems
Arpad Muranyi, Intel Corporation
Bob Ross, Teraspeed Consulting Group
From an original by Stephen Peters published 1997
Copyright © 2005 Government Electronics and Information Technology Association and The IBIS Open Forum. All Rights Reserved.
IBIS Open Forum
IBIS Modeling Cookbook
Page 1
3.1 Extracting I-V Data from Simulations
The first step to extracting the required I-V tables is understanding the buffer's operation. Analyze the buffer schematic and determine how to put the buffer's output into a logic low, logic high and (if applicable) high impedance (3-state) state. As mentioned above, the schematic should include any ESD or protection diodes. Also, understand the buffer's power supply voltage reference ("Vcc") requirements and connections. The schematic should also indicate if the power clamp and/or ground clamp diode structures are tied to voltage rails (voltage references) different from those used by the pullup and/or pulldown transistors.
3.1.1 Simulation Setup
A typical I-V table simulation setup for an output or I/O buffer is shown in Figure 3.1 below. For this example, the buffer being analyzed is a standard 3-state buffer with a single push-pull output stage. The buffer uses electrostatic discharge protection devices in addition to its parasitic driver diodes. The buffer's clamp supplies are assumed identical to its driver supply (Vcc hereinafter).
Page 12
Vcc
Logic Low
IN
EN
Logic Low
ESD Clamp
Current
PAD
ESD Clamp
Swept
Voltage
Source
Figure 3.1 – Standard 3-state Buffer (Pulldown I-V Table Extraction Shown)
All measurements are made at the output node (pad) as shown above. Remove all package lead (R_pin, L_pin, and C_pin) parasitics. However, any series resistances present between the pad and the pullup/pulldown transistors should be included (these are not shown in Figure 3.1).
The output buffer is connected to an independent voltage source. Set the buffer's input(s) so that the desired output state (low, high, off) is obtained, then using a DC or "transfer function" analysis sweep the voltage source over the sweep range -Vcc to 2*Vcc while recording the current into the buffer. An alternative method is to perform a "transient analysis". The voltage source in this case should be linear ramp function driving the output node, slow enough that the current measurement at each time point is effectively DC, without reactive aspects of the design affecting the result. The current flow into the pad is measured (by IBIS convention, current flow into the die pad is positive), as is the voltage at the node with respect to a reference, then the resulting I-T and V-T data is combined into a single I-V table. Note that a transient function analysis may require post-simulation data manipulation.
11
©2019 Zuken


ZUKEN
01
MOTIVATION
02
IMPEDANCE CONCEPT
03
IBIS CONTENT
04
OBTAIN IMPEDANCE FROM IBIS
05
CONCLUSION
OUTLINE
12
©2019 Zuken


Obtain impedance from IBIS curves
ZUKEN
70mA
60mA
50mA
40mA
30mA
20mA
10mA
0mA
23 mA
0.64V
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
1.8V
2V
typical
minimum
maximum
1.8V
50 ohms
Picture from Todd W. 2005 DAC IBIS Summit
13
©2019 Zuken


Obtain Output type buffer impedance from IBIS
ZUKEN
Need to use Combined Pullup/Pulldown curves
– Pullup + Clamps
– Pulldown + Clamps
Load line / Crossing Point
To avoid numerical errors
$Z_0 = \frac{dV}{dI} @ R_L$
Pulldown
Pullup
Ohm
Zo
70
60
50
40
30
20
10
0
Volt
An example Output impedance graph
14
©2019 Zuken


Obtain Input type buffer impedance from IBIS
ZUKEN
Use the Combined Clamp data
To avoid numerical errors
$Z_0 = \frac{dV}{dI} @ R_L$
Example data
Individual curves
Combined curve
15
©2019 Zuken


ZUKEN
01 MOTIVATION
02 IMPEDANCE CONCEPT
03 IBIS CONTENT
04 OBTAIN IMPEDANCE FROM IBIS
05 CONCLUSION
OUTLINE
16
©2019 Zuken

Conclusion

ZUKEN

- Impedance matching is important for high-speed design
  - Not only for interconnect impedance, but also I/O buffer impedance should be counted in the big picture
- The I/O buffer impedance can be obtained from IBIS curve data
  - Obtain buffer driving impedance from IBIS combined Pullup/Pulldown curve data
  - Obtain buffer Input impedance from IBIS combined Power /Ground Clamps curve data
- I/O impedance maybe vary for different loads

17

©2019 Zuken

A potential application of IBIS to CISPR25 based EMI analysis of DCDC converter

Kazuyuki Sakata, Renesas Electronics Corp.
Koji Ichikawa, DENSO CORP.
Miyoko Goto, Ricoh Corp.
Toshiki Kanamoto, Hirosaki University

Copyright© JEITA SD-TC All Rights Reserved 2019

Agenda

- Motivation and objective
- Impedance modeling of DCDC converters
- Measurement settings and results
- Simulation results and comparison with measurement
- Discussion
- Summary

Copyright© JEITA SD-TC All Rights Reserved 2019

Agenda

- Motivation and objective
- Impedance modeling of DCDC converters
- Measurement settings and results
- Simulation results and comparison with measurement
- Discussion
- Summary

Copyright© JEITA SD-TC All Rights Reserved 2019

Motivation and objective

- EMI simulation of IBIS modeled DCDC converter
- ✓ Study on modeling to comply with CISPR25
- ✓ Initial trial with bare IBIS descriptions
- → Simulation results show discrepancies from measurements
- Make discussions on source of errors and solutions

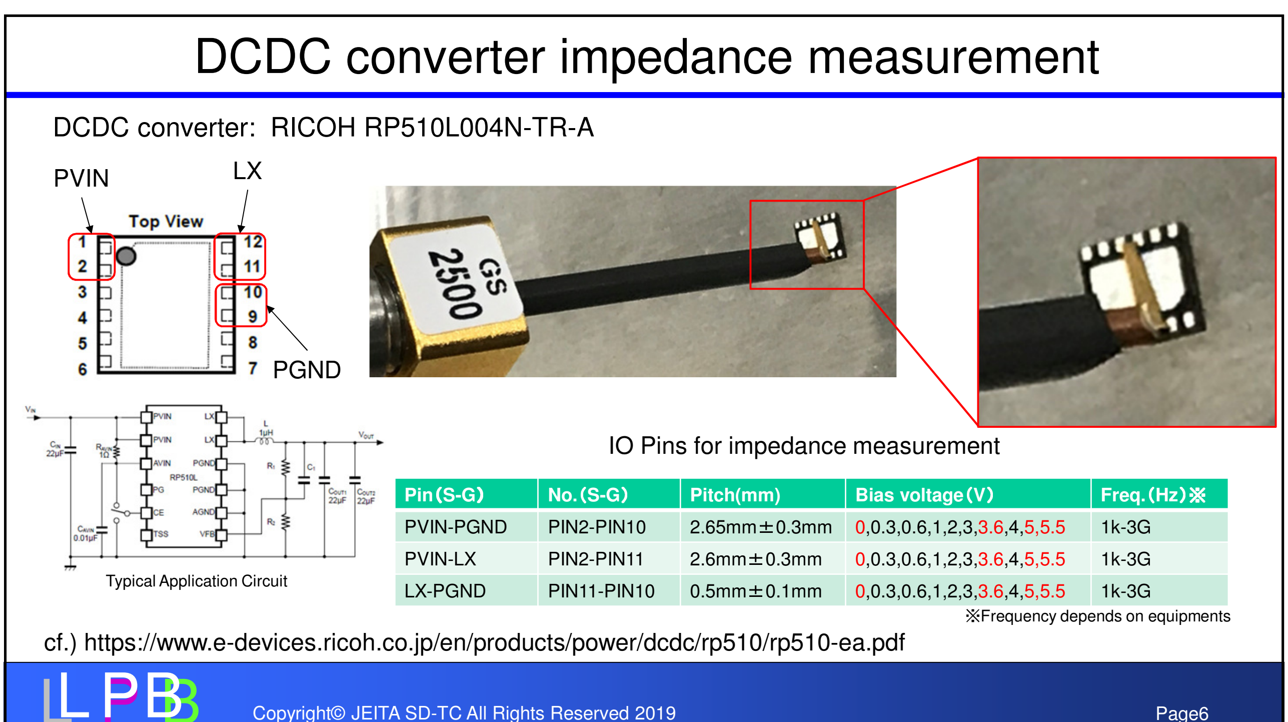
Copyright© JEITA SD-TC All Rights Reserved 2019

Agenda

- Motivation and objective
- Impedance modeling of DCDC converters
- Measurement settings and results
- Simulation results and comparison with measurement
- Discussion
- Summary

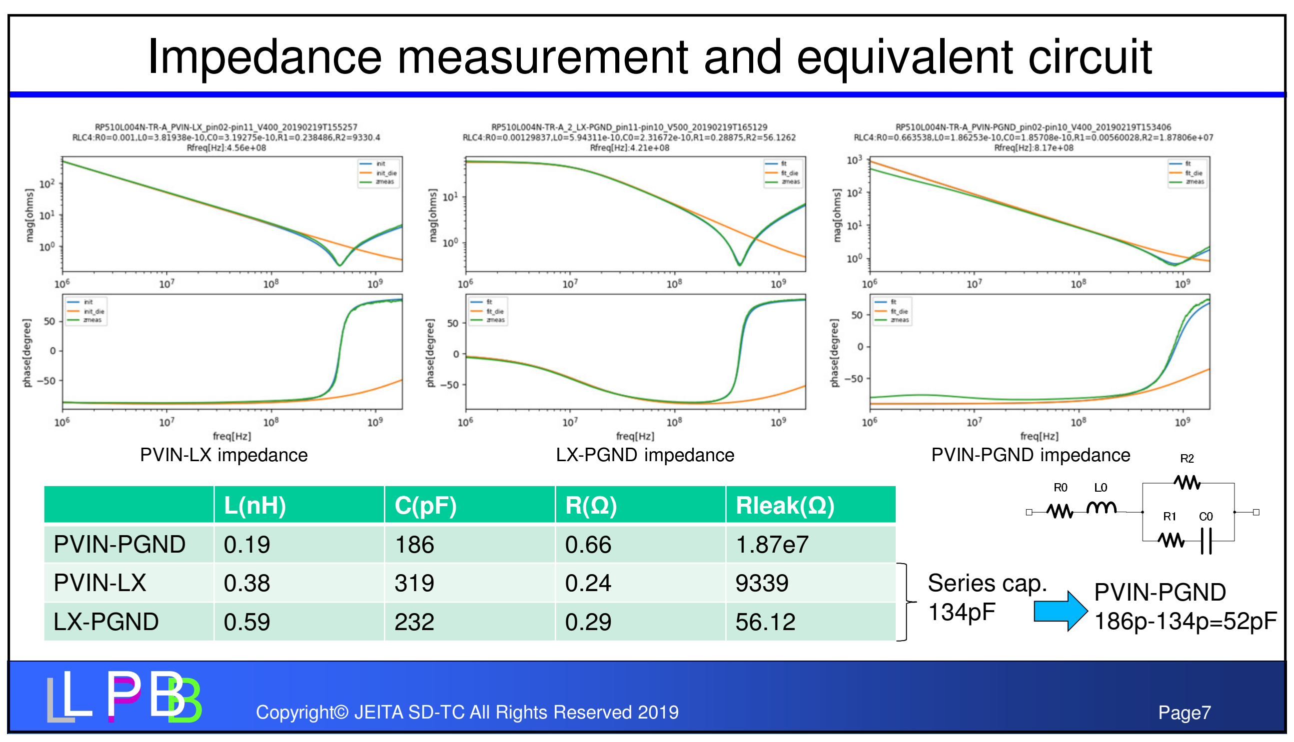
LPB

Copyright© JEITA SD-TC All Rights Reserved 2019



Pin (S-G)	No. (S-G)	Pitch(mm)	Bias voltage (V)	Freq. (Hz)※
PVIN-PGND	PIN2-PIN10	2.65mm±0.3mm	0,0.3,0.6,1,2,3,3.6,4,5,5.5	1k-3G
PVIN-LX	PIN2-PIN11	2.6mm±0.3mm	0,0.3,0.6,1,2,3,3.6,4,5,5.5	1k-3G
LX-PGND	PIN11-PIN10	0.5mm±0.1mm	0,0.3,0.6,1,2,3,3.6,4,5,5.5	1k-3G

※Frequency depends on equipments



	L(nH)	C(pF)	R(Ω)	Rleak(Ω)
PVIN-PGND	0.19	186	0.66	1.87e7
PVIN-LX	0.38	319	0.24	9339
LX-PGND	0.59	232	0.29	56.12

Capacitance description in IBIS format

Specify the measured caps as C_comp_pullup, C_comp_pulldown in the IBIS format.

```
[Model]    bbb
Model_type       I/O
Polarity         Non-Inverting
Vinl          = .72000000
Vinh           = 2.88000000
Vmeas          = 1.80000000
|C_comp          5.53197e-10 4.65065e-10 7.07186e-10 | CDL
C_comp_pullup     319e-12     NA          NA          | Measurement
C_comp_pulldown   232e-12     NA          NA          | Measurement
```

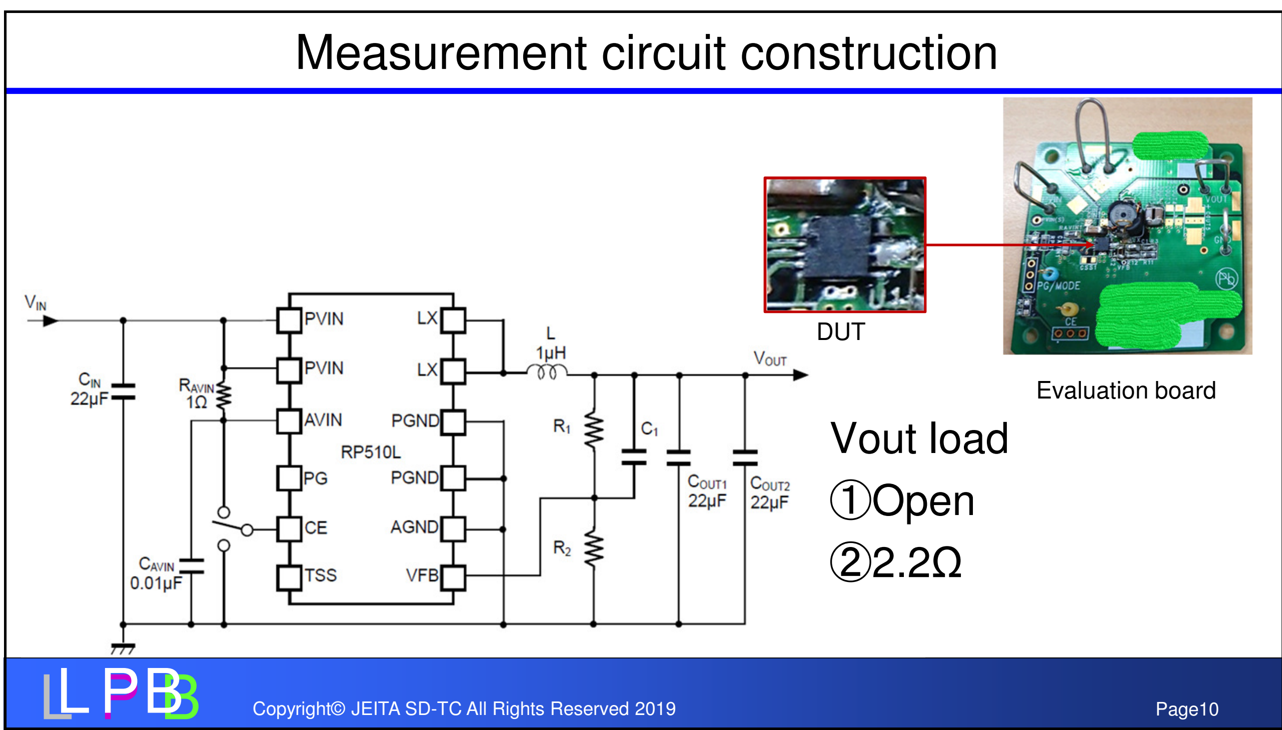
In case that large discrepancy appear in the total capacitance, need to regenerate IBIS model adding supplemental capacitance to the spice netlist.

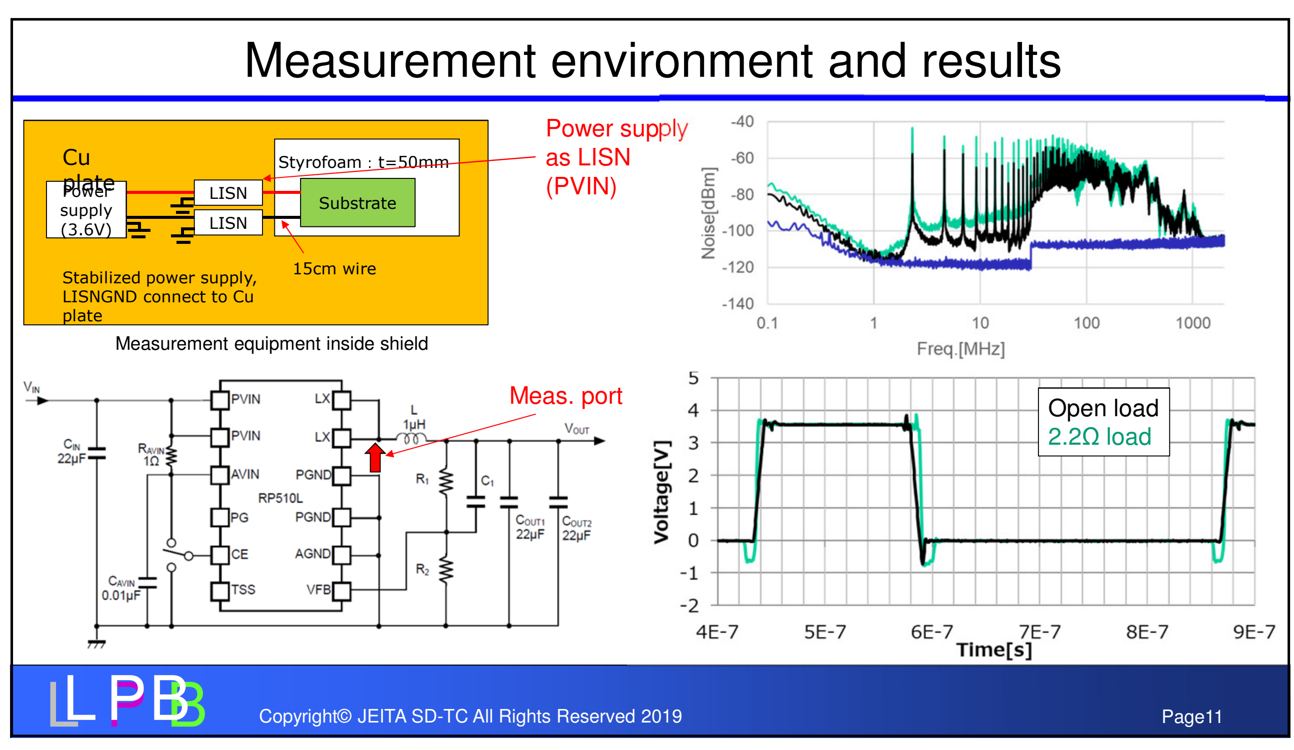
Copyright© JEITA SD-TC All Rights Reserved 2019

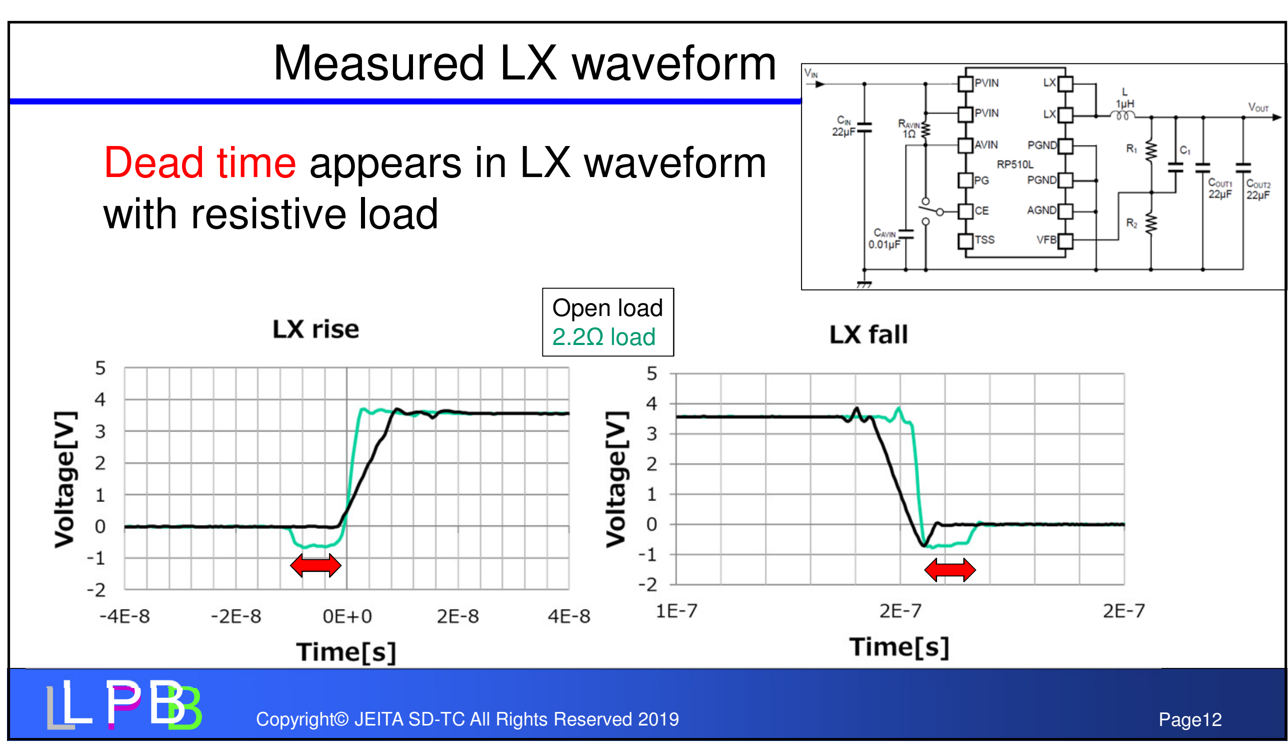
Agenda

- Motivation and objective
- Impedance modeling of DCDC converters
- Measurement settings and results
- Simulation results and comparison with measurement
- Discussion
- Summary

Copyright© JEITA SD-TC All Rights Reserved 2019




Measurement environment and results
Cu plate
Power supply (3.6V)
LISN
LISN
Styrofoam : t=50mm
Substrate
15cm wire
Stabilized power supply, LISNGND connect to Cu plate
Measurement equipment inside shield
Power supply as LISN (PVIN)
Noise[dBm]
Freq.[MHz]
Meas. port
RP510L
Open load
2.2Ω load
Voltage[V]
Time[s]
Copyright© JEITA SD-TC All Rights Reserved 2019
Page11

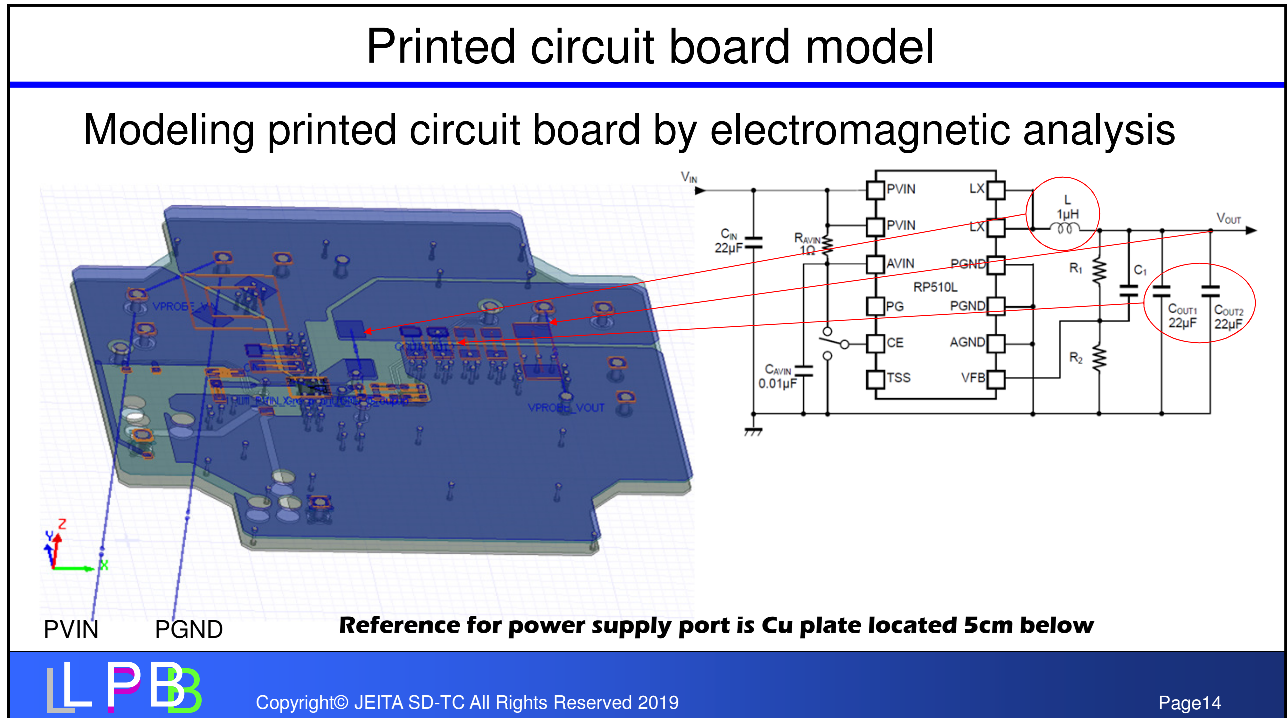

Measured LX waveform
Dead time appears in LX waveform with resistive load
LX rise
LX fall
Open load
2.2Ω load
Voltage[V]
Time[s]
RP510L
Copyright© JEITA SD-TC All Rights Reserved 2019
Page12

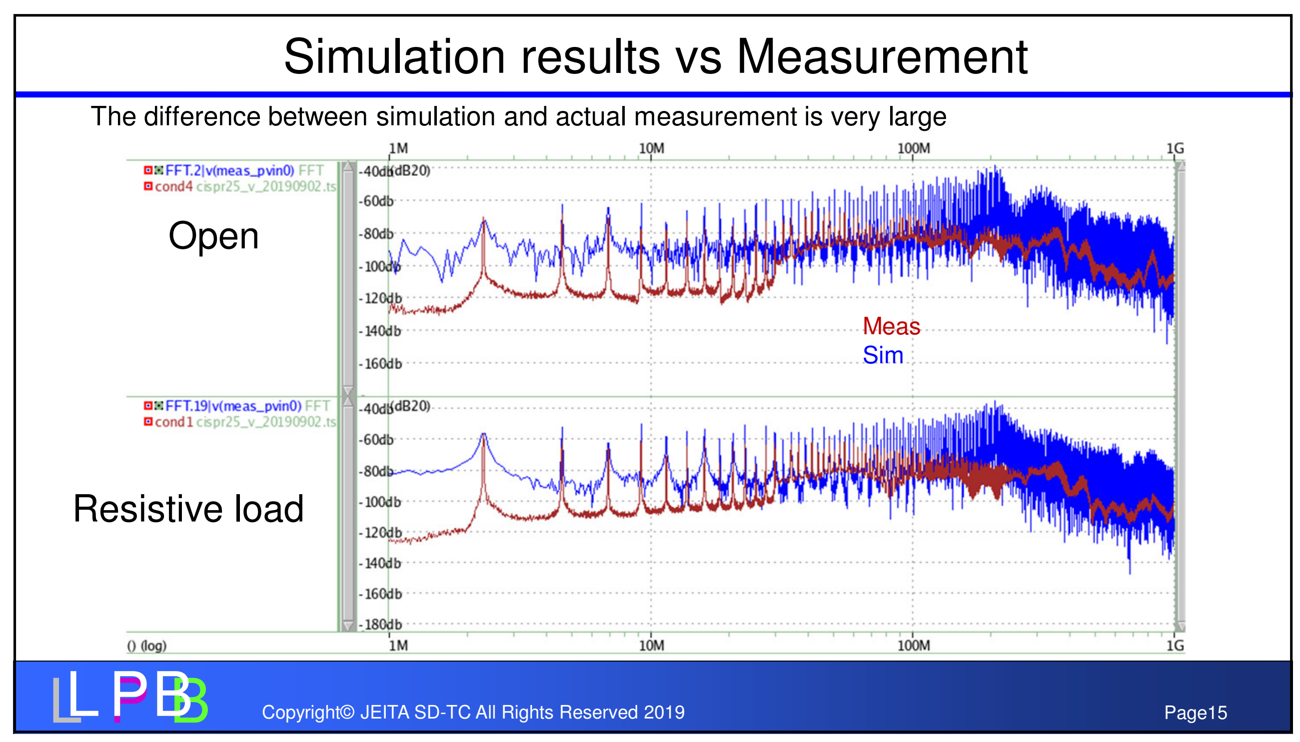
Agenda

- Motivation and objective
- Impedance modeling of DCDC converters
- Measurement settings and results
- Simulation results and comparison with measurement
- Discussion
- Summary

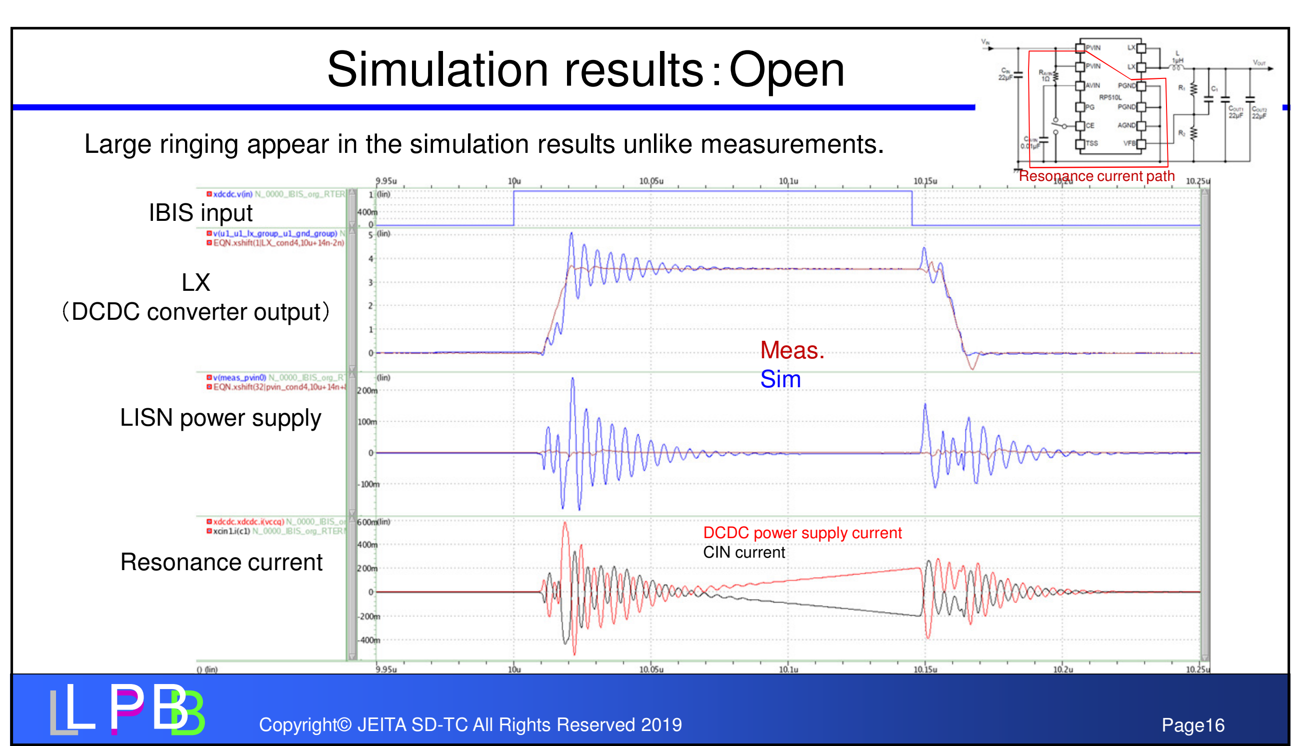
LPB

Copyright© JEITA SD-TC All Rights Reserved 2019

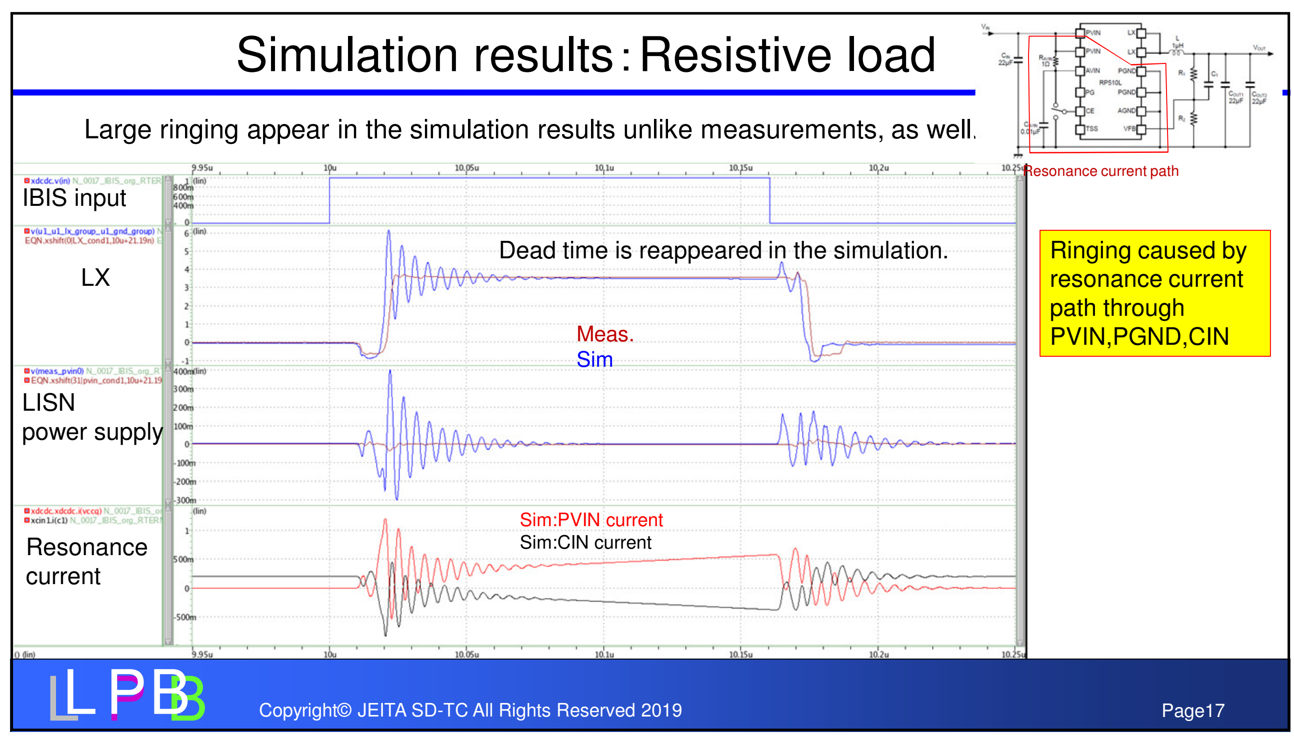




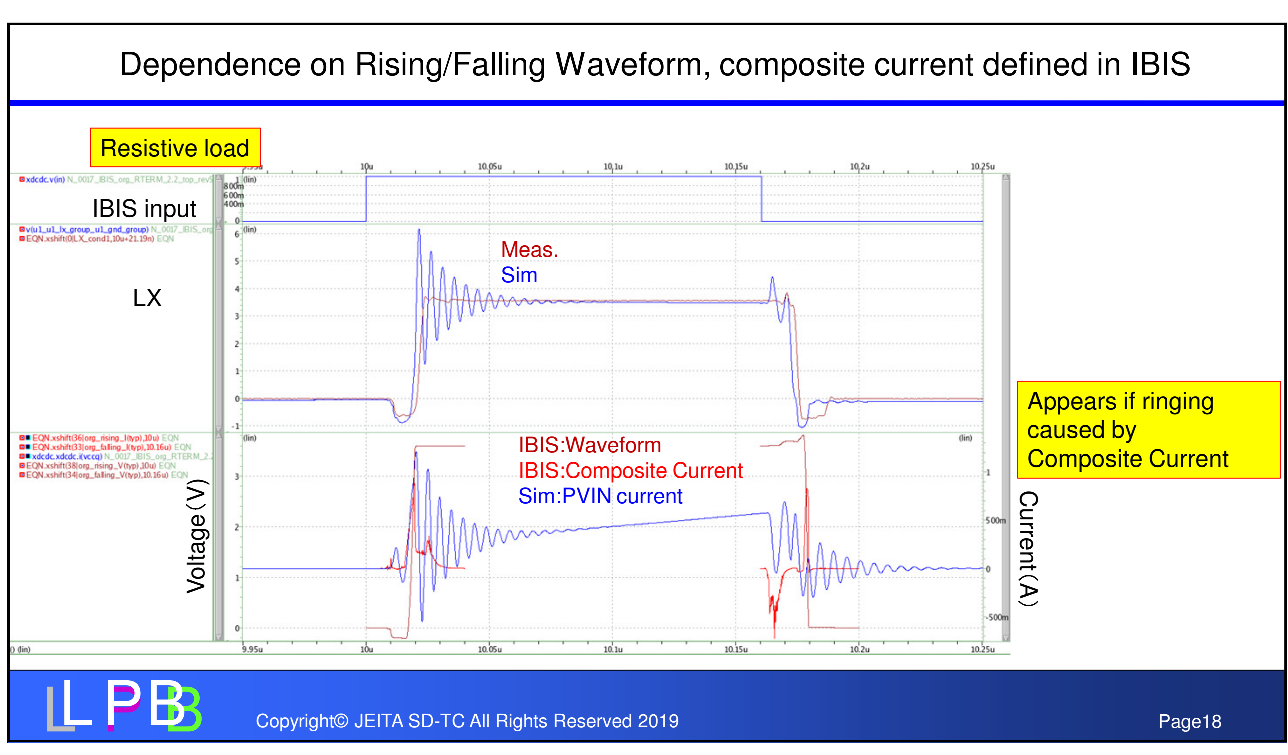
Simulation results vs Measurement
The difference between simulation and actual measurement is very large
Open
Resistive load
Meas
Sim
1M
10M
100M
1G
Copyright© JEITA SD-TC All Rights Reserved 2019
Page15



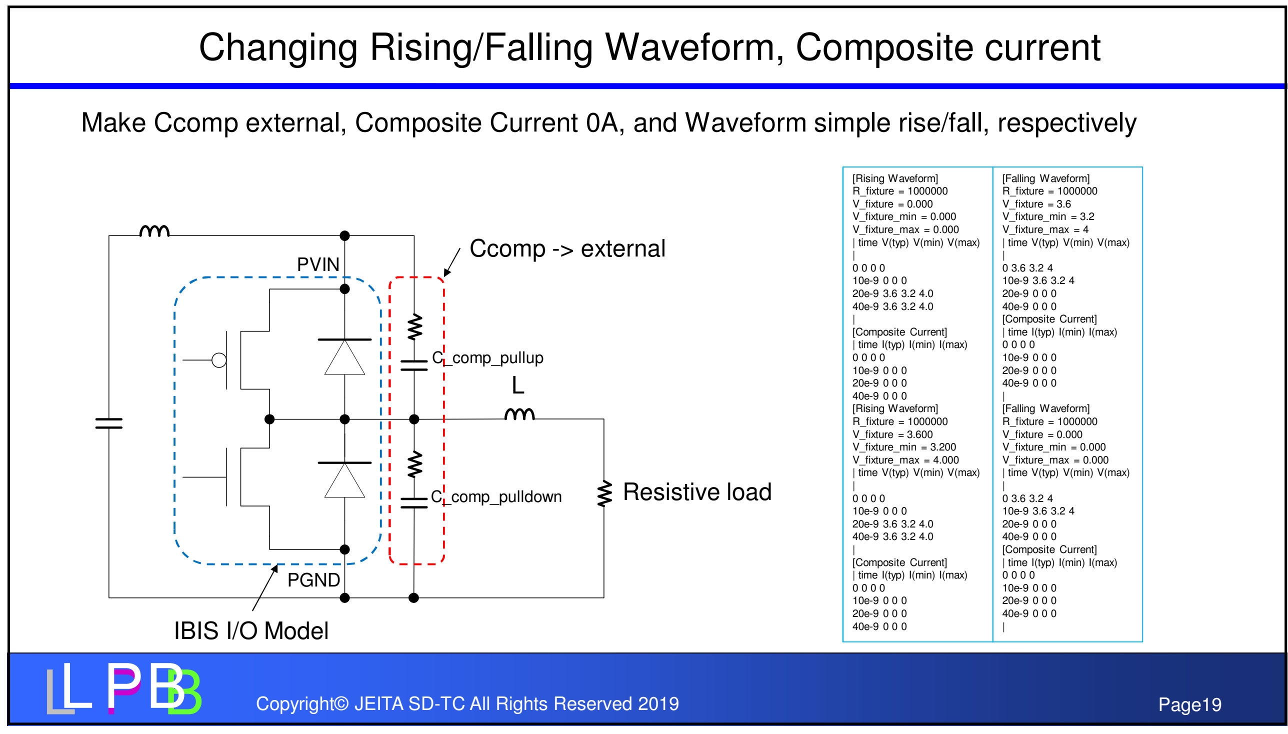
Simulation results：Open
Large ringing appear in the simulation results unlike measurements.
IBIS input
LX
（DCDC converter output）
LISN power supply
Resonance current
Meas.
Sim
DCDC power supply current
CIN current
Resonance current path
Copyright© JEITA SD-TC All Rights Reserved 2019
Page16

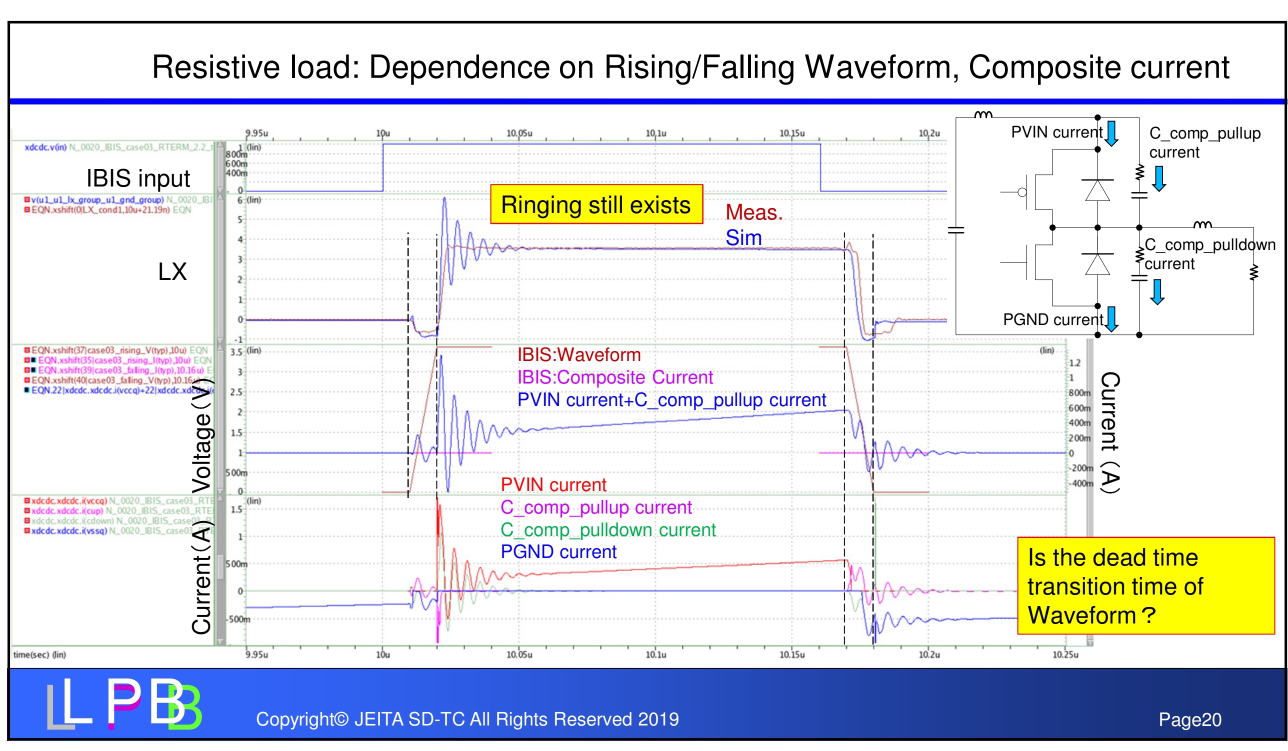


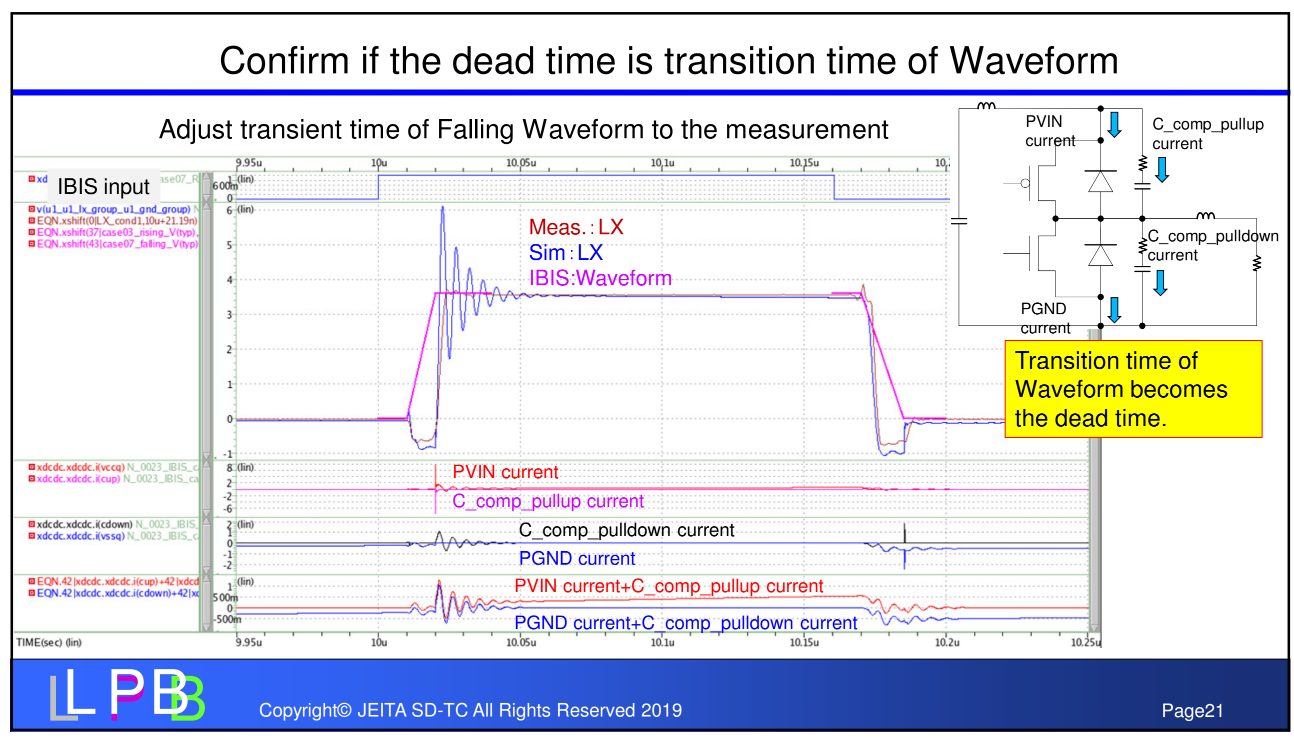
Simulation results：Resistive load
Large ringing appear in the simulation results unlike measurements, as well.
Resonance current path
IBIS input
LX
Dead time is reappeared in the simulation.
Meas.
Sim
LISN
power supply
Resonance
current
Sim:PVIN current
Sim:CIN current
Ringing caused by resonance current path through PVIN,PGND,CIN
LPB
Copyright© JEITA SD-TC All Rights Reserved 2019
Page17



Dependence on Rising/Falling Waveform, composite current defined in IBIS
Resistive load
IBIS input
LX
Meas.
Sim
IBIS:Waveform
IBIS:Composite Current
Sim:PVIN current
Voltage (V)
Current (A)
Appears if ringing caused by Composite Current
LPB
Copyright© JEITA SD-TC All Rights Reserved 2019
Page18


Changing Rising/Falling Waveform, Composite current
Make Ccomp external, Composite Current 0A, and Waveform simple rise/fall, respectively
Ccomp -> external
PVIN
C_comp_pullup
L
C_comp_pulldown
Resistive load
PGND
IBIS I/O Model
[Rising Waveform]
R_fixture = 1000000
V_fixture = 0.000
V_fixture_min = 0.000
V_fixture_max = 0.000
| time V(typ) V(min) V(max)
|
0 0 0 0
10e-9 0 0 0
20e-9 3.6 3.2 4.0
40e-9 3.6 3.2 4.0
|
[Composite Current]
| time I(typ) I(min) I(max)
0 0 0 0
10e-9 0 0 0
20e-9 0 0 0
40e-9 0 0 0
[Rising Waveform]
R_fixture = 1000000
V_fixture = 3.600
V_fixture_min = 3.200
V_fixture_max = 4.000
| time V(typ) V(min) V(max)
|
0 0 0 0
10e-9 0 0 0
20e-9 3.6 3.2 4.0
40e-9 3.6 3.2 4.0
|
[Composite Current]
| time I(typ) I(min) I(max)
0 0 0 0
10e-9 0 0 0
20e-9 0 0 0
40e-9 0 0 0
[Falling Waveform]
R_fixture = 1000000
V_fixture = 3.6
V_fixture_min = 3.2
V_fixture_max = 4
| time V(typ) V(min) V(max)
|
0 3.6 3.2 4
10e-9 3.6 3.2 4
20e-9 0 0 0
40e-9 0 0 0
[Composite Current]
| time I(typ) I(min) I(max)
0 0 0 0
10e-9 0 0 0
20e-9 0 0 0
40e-9 0 0 0
|
[Falling Waveform]
R_fixture = 1000000
V_fixture = 0.000
V_fixture_min = 0.000
V_fixture_max = 0.000
| time V(typ) V(min) V(max)
|
0 3.6 3.2 4
10e-9 3.6 3.2 4
20e-9 0 0 0
40e-9 0 0 0
[Composite Current]
| time I(typ) I(min) I(max)
0 0 0 0
10e-9 0 0 0
20e-9 0 0 0
40e-9 0 0 0
|
Copyright© JEITA SD-TC All Rights Reserved 2019
Page19

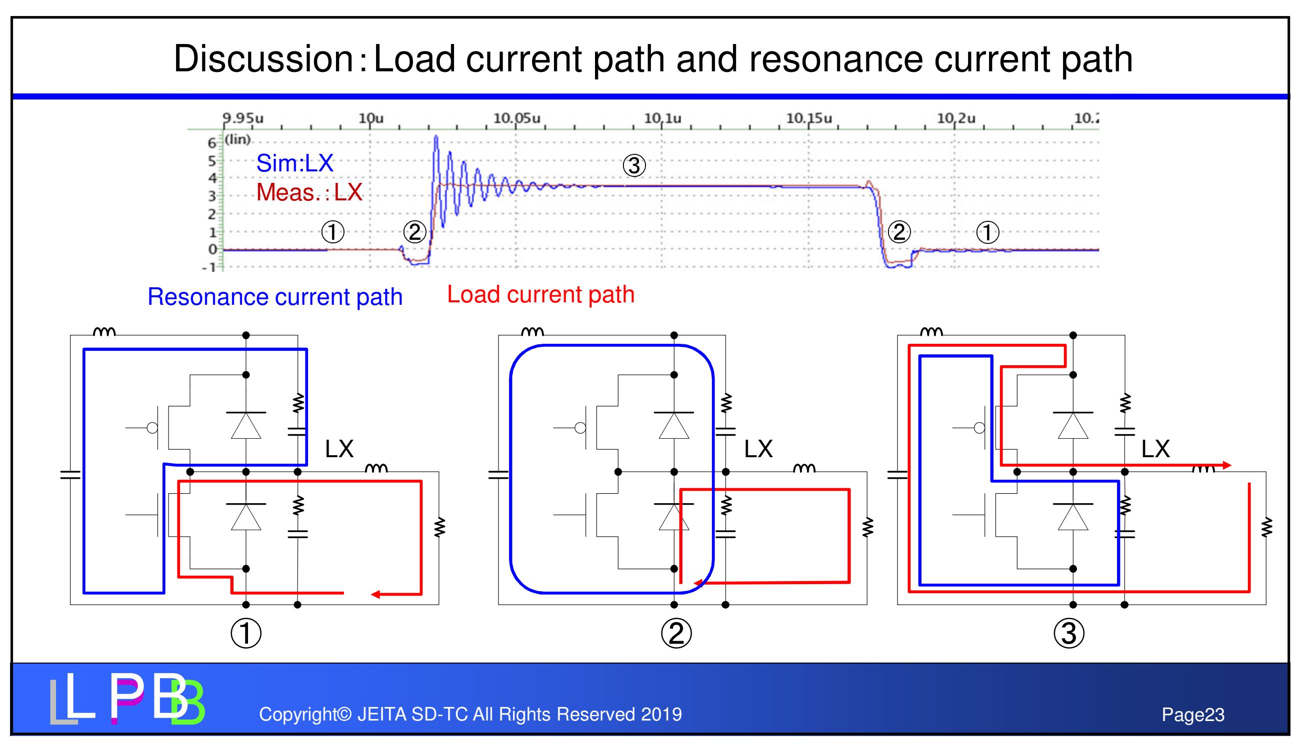

Resistive load: Dependence on Rising/Falling Waveform, Composite current
IBIS input
LX
Ringing still exists
Meas.
Sim
IBIS:Waveform
IBIS:Composite Current
PVIN current+C_comp_pullup current
Voltage (V)
Current (A)
PVIN current
C_comp_pullup current
C_comp_pulldown current
PGND current
PVIN current
C_comp_pullup current
C_comp_pulldown current
PGND current
Is the dead time transition time of Waveform ?
Copyright© JEITA SD-TC All Rights Reserved 2019
Page20

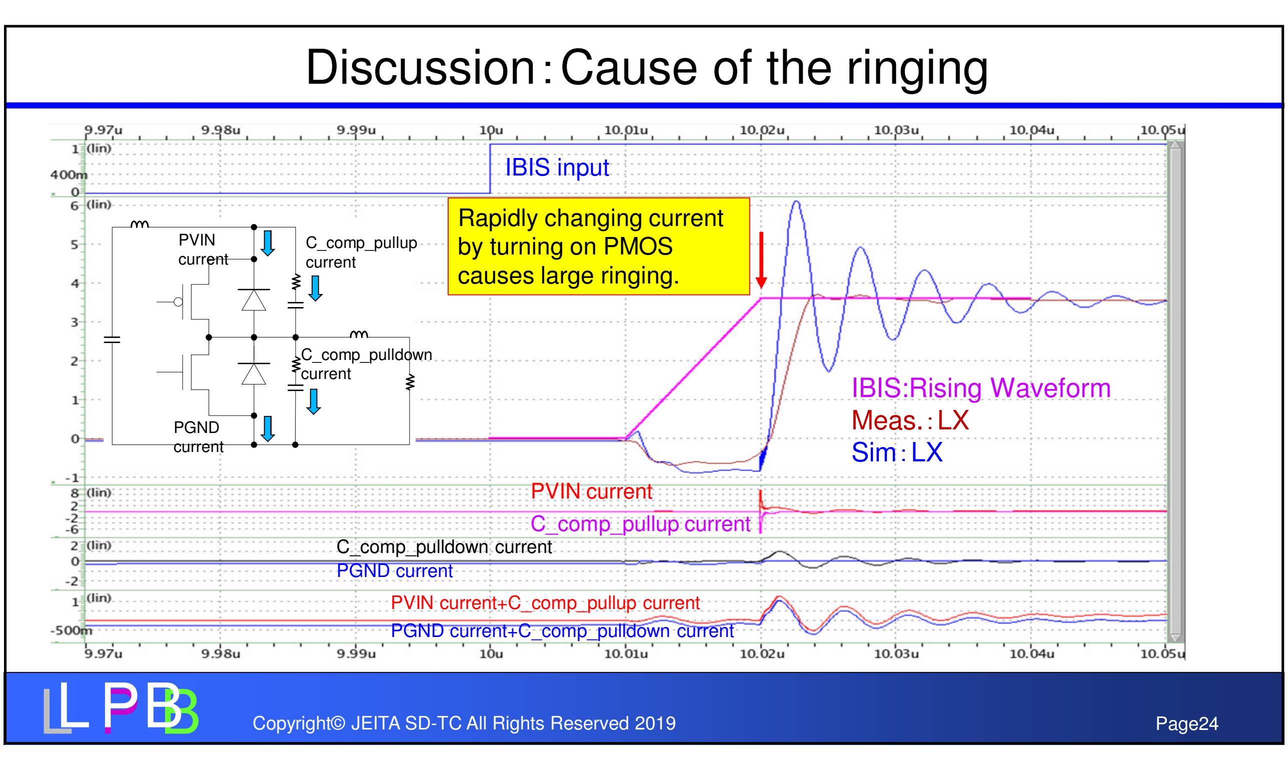


Agenda

- Motivation and objective
- Impedance modeling of DCDC converters
- Measurement settings and results
- Simulation results and comparison with measurement
- Discussion
- Summary

Copyright© JEITA SD-TC All Rights Reserved 2019


Discussion : Load current path and resonance current path
Sim:LX
Meas. : LX
Resonance current path
Load current path
LX
①
②
③
Copyright© JEITA SD-TC All Rights Reserved 2019
Page23


Discussion : Cause of the ringing
IBIS input
Rapidly changing current by turning on PMOS causes large ringing.
PVIN current
C_comp_pullup current
C_comp_pulldown current
PGND current
IBIS:Rising Waveform
Meas. : LX
Sim : LX
PVIN current
C_comp_pullup current
C_comp_pulldown current
PGND current
PVIN current+C_comp_pullup current
PGND current+C_comp_pulldown current
Copyright© JEITA SD-TC All Rights Reserved 2019
Page24

Agenda

- Motivation and objective
- Impedance modeling of DCDC converters
- Measurement settings and results
- Simulation results and comparison with measurement
- Discussion
- Summary

Copyright© JEITA SD-TC All Rights Reserved 2019

Summary

- Trial to simulate CISPR25 for IBIS described DCDC
- Discrepancies from measurements in high frequency range

✓ Possible source of error in the simulation:

Large ringing induced by instantly switching MOS transistors

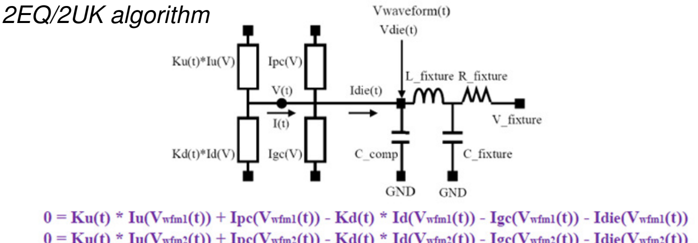
- Mitigating unrealistic transitions is considered to be a dominant solution.

Copyright© JEITA SD-TC All Rights Reserved 2019

Possible improvements

- Retrieve Waveform and Composite Current in IBIS by SPICE simulation adjusted the load conditions

cf.) https://ibis.org/summits/nov08a/chen.pdf



- Obtain Rising/Falling Waveform and Composite Current directly from measurement

Copyright© JEITA SD-TC All Rights Reserved 2019

IBIS-AMI & COM Co-design for 25G Serdes

Asian IBIS Summit
Tokyo, Japan
November 8, 2019

Nan Hou, Amy Zhang, Guohua Wang, David Zhang, Anders Ekholm

Page 1 (29)

AGENDA

- Traditional IBIS-AMI
- COM Overview
- IBIS-AMI Co-design with COM for 25G
- Two example channels
- Co-simulation Conclusion
- Next Steps

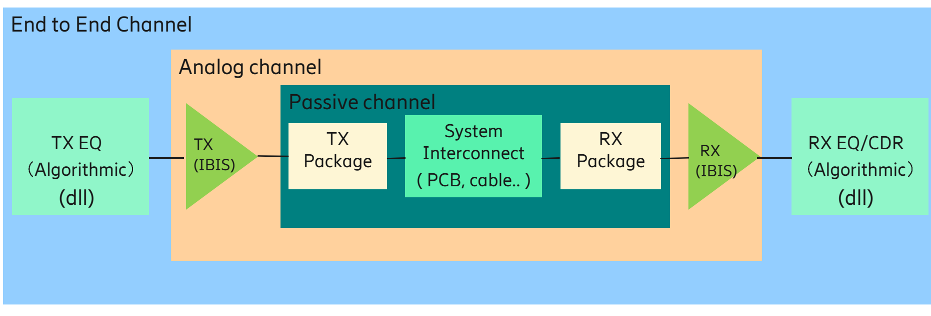
Page 2 (29)

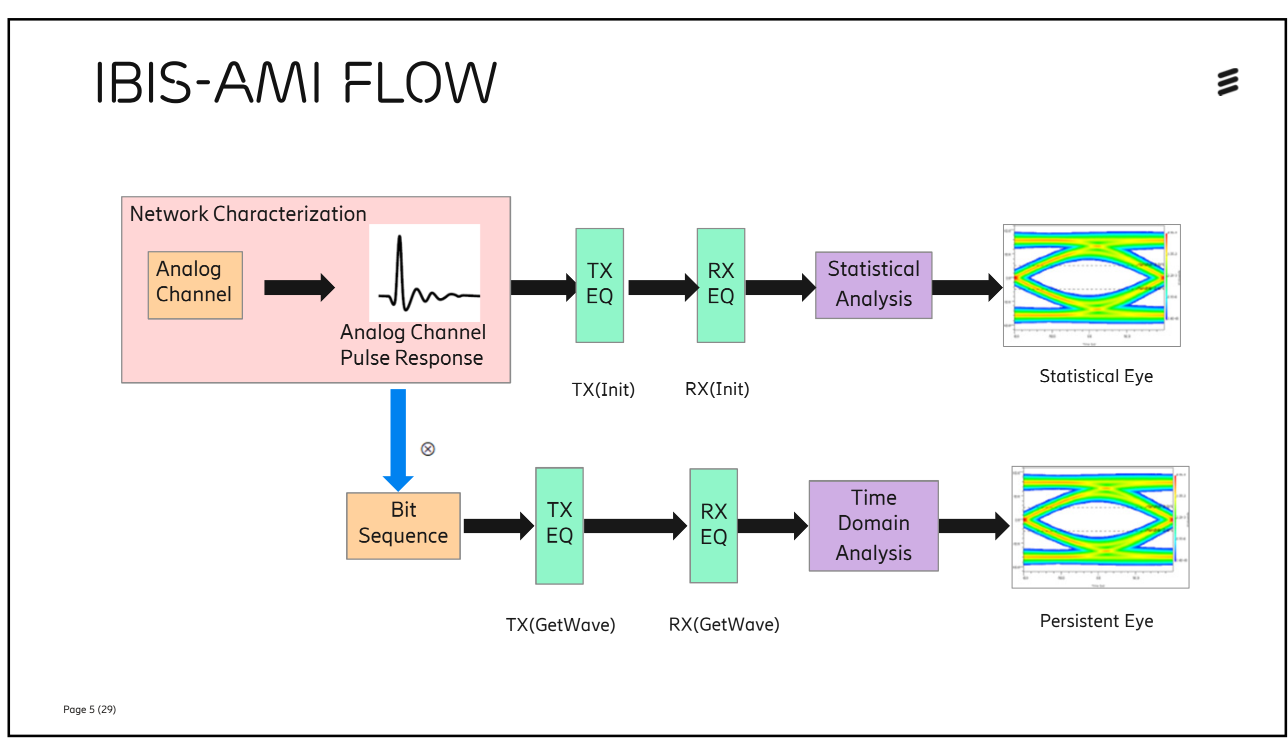
AGENDA

- Traditional IBIS-AMI
- COM Overview
- IBIS-AMI Co-design with COM for 25G
- Two example channels
- Co-simulation Conclusion
- Next Steps

IBIS-AMI OVERVIEW

- IBIS is Input/output Buffer Information Specification
- AMI stands for Algorithmic Modeling Interface
- Analog model: drive strength/amplitude, rise/fall time, impedance
- Algorithmic model: Equalizer (CTLE, FFE, DFE) , clock data recovery





AGENDA

- Traditional IBIS-AMI
- COM Overview
- IBIS-AMI Co-design with COM for 25G
- Two example channels
- Co-simulation Conclusion
- Next Steps

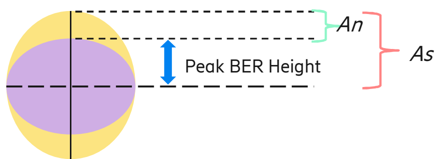
Page 6 (29)

COM OVERVIEW

The Channel Operating Margin (COM) is a figure of merit for a channel derived from a measurement of its scattering parameters

COM is related to the ratio of a calculated signal amplitude to a calculated noise amplitude as defined by Equation

$$COM = 20 \times \log 10(As/An)$$



Where *As* is the signal amplitude, *An* is the noise amplitude

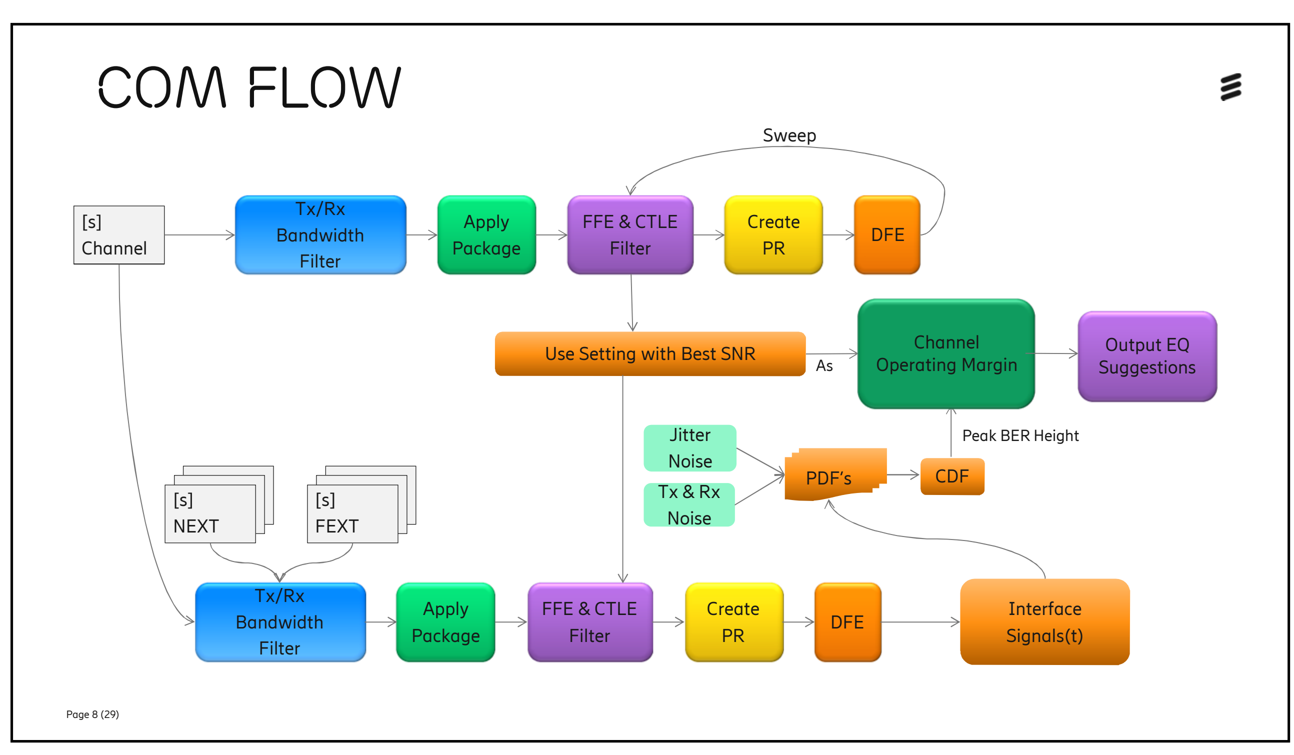
COM has been adapted by various standards:

- IEEE 802.3
- OIF CEI
- JEDEC 204C

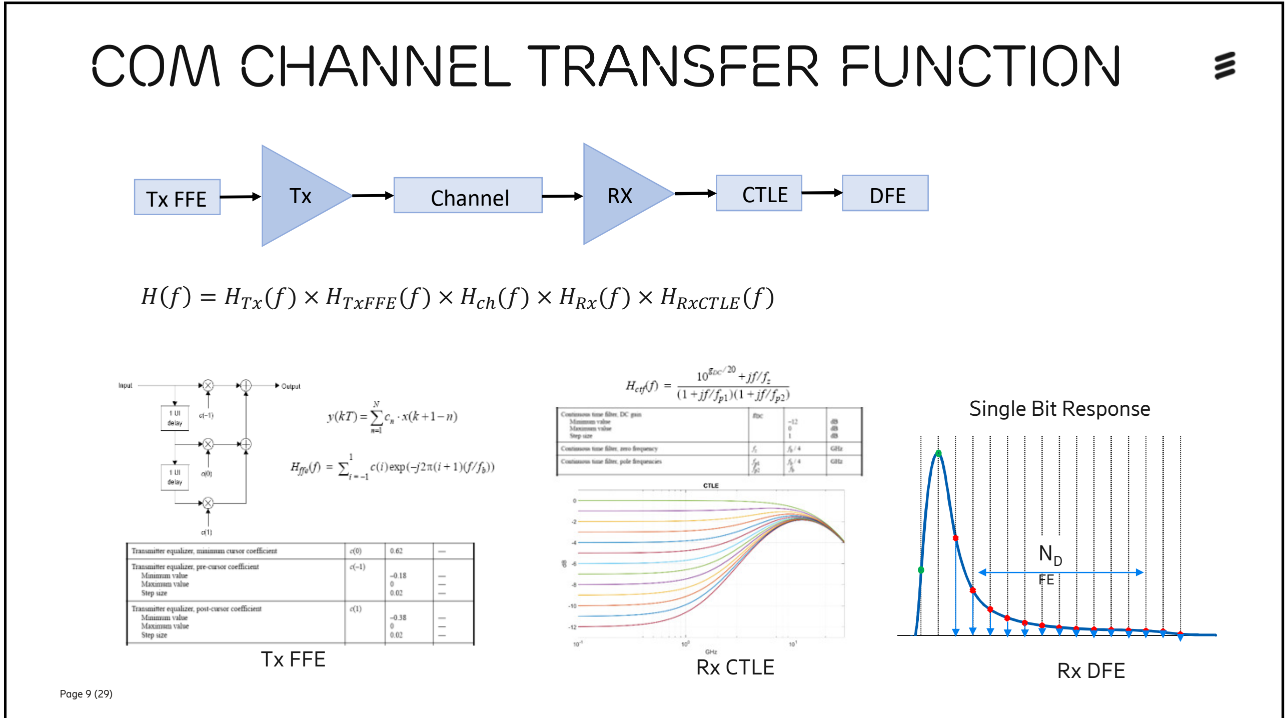
An (Peak BER Noise) = *As* - Peak BER Height

Page 7 (29)

COM FLOW



Page 8 (29)



COM OPTIMAL EQ SETTINGS

- COM is a figure of merit (FOM), which calculates the ratio of peak signal level to the peak noise level at the receiver sampling latch, comprehending device Tx characteristics (i.e., driver filter, FFE filter, package S-parameters), channel characteristics (i.e., S-parameters) and receiver characteristics (i.e., Rx filter, CTLE filter, package S-parameters and DFE)
- Determine optimal equalization settings
  - An exhaustive search for the best SNR used as a FOM for finding the best FFE and CTLE setting
  - FFE and CTLE are optimized jointly
  - The DFE is only used to gate the SBR

$$FOM = 10log_{10}\left(\frac{A_S^2}{\sigma_{TX}^2 + \sigma_{ISI}^2 + \sigma_J^2 + \sigma_{XT}^2 + \sigma_N^2}\right)$$

A_S – peak signal amplitude
σ_{TX} - transmitter noise
σ_{ISI} - residual ISI
σ_J – jitter contribution to amplitude noise
σ_{XT} – peak crosstalk
σ_N – spectral noise at the ouput of CTLE

Page 10 (29)

AGENDA

- Traditional IBIS-AMI
- COM Overview
- IBIS-AMI Co-design with COM for 25G
- Two example channels
- Co-simulation Conclusion
- Next Steps

IBIS-AMI COMBINE WITH COM

- Can we use COM to evaluate the channel margin in early design phase of a project?
- Are the COM recommended equalization parameters suitable for the Channel?
- How can we combine the advantages of COM with IBIS-AMI?

25G CO-SIMULATION PROCESS

- Extraction of passive S parameter model of the simulation channel
- Use S parameter to do COM simulation
- IBIS simulation using COM recommended EQ parameter
- IBIS simulation to sweep EQ parameter
- Comparing the eye diagram in time domain

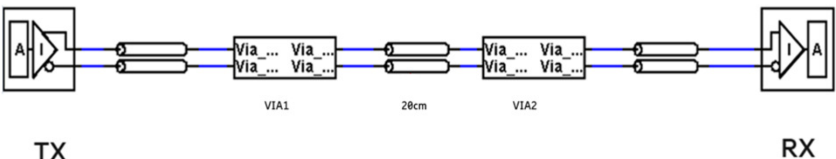
AGENDA

- Traditional IBIS-AMI
- COM Overview
- IBIS-AMI Co-design with COM for 25G
- **Two example channels**
- Co-simulation Conclusion
- Next Steps

CASE1-SIMULATION TOPOLOGY

Simulation Topology Configuration

- Signal Rate: 25Gbps
- PCB Material: Mid-loss FR4
- PCB Channel Length: 20 cm



COM SIMULATION CONFIGURATION

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	24.576	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[2.5e-4 2.5e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 30]	mm	[test cases]
z_p (NEXT)	[12 12]	mm	[test cases]
z_p (FEXT)	[12 30]	mm	[test cases]
z_p (RX)	[12 30]	mm	[test cases]
C_p	[1.8e-4 1.8e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[55 55]	Ohm	[TX RX]
f_r	0.75	*fb	
c(0)	0.62		min
c(-1)	[-0.18:0.02:0]		[min:step:max]
c(1)	[-0.38:0.02:0]		[min:step:max]
g_DC	[-12:1:0]	dB	[min:step:max]
f_z	6.144	GHz	
f_p1	6.144	GHz	
f_p2	24.576	GHz	
A_v	0.4	V	
A_fe	0.4	V	
A_ne	0.6	V	
L	2		
M	32		
N_b	0	UI	
b_max(1)	1		
b_max(2..N_b)	1		
sigma_RJ	0.01	UI	
A_DD	0.05	UI	
eta_0	5.20E-08	V^2/GHz	
SNR_TX	27	dB	
R_LM	1		
DER_0	1.00E-12		
Operational control			
COM Pass threshold	3	dB	
Include PCB	0	logical	

Table 93A¨C2 parameter		
Parameter	Setting	Units
package_tl_tau	6.141E-03	ns
package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
package_Z_c	78.2	Ohm

Table 92¨C12 parameter		
Parameter	Setting	
board_tl_tau	6.191E-03	ns
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
board_Z_c	109.8	Ohm
z_bp (TX)	151	mm
z_bp (NEXT)	72	mm
z_bp (FEXT)	72	mm
z_bp (RX)	151	mm

All parameter come from IEEE 802.3bj

COM SIMULATION RESULT

Channel Compliance Checker Rev1.1 - [Single Mode]

Single Batch Help Exit

Compliance Check

S-parameter Selection: C:\25G_20cm.s4p [Browse]

Standard Selection: CEI-25G-LR

☑ Run COM

☑ Generate Report [Run Check]

Result Viewer

Check Item [Plot]

COM: 10.9926 dB

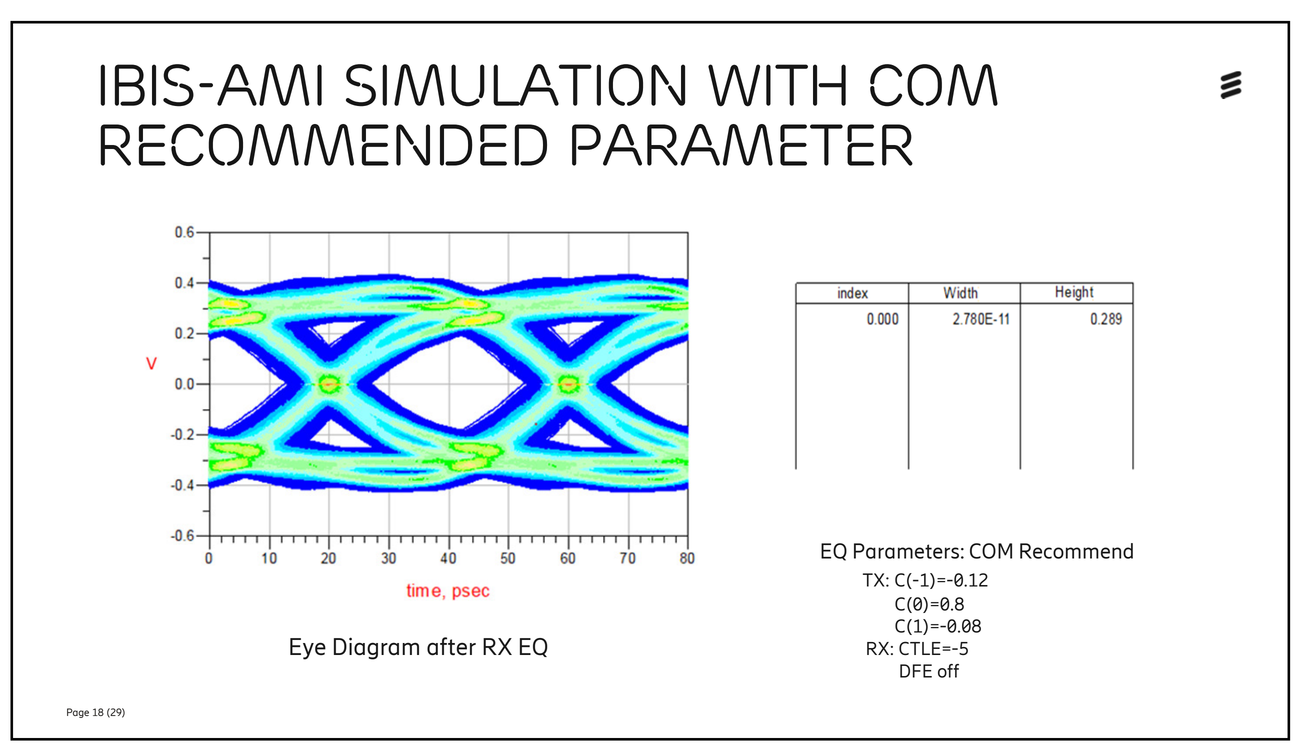
EQ Tap:
TXLE_taps: "[-0.12 0.8 -0.08]"
CTLE_DC_gain_dB: -5
DFE Taps: "zeros(0

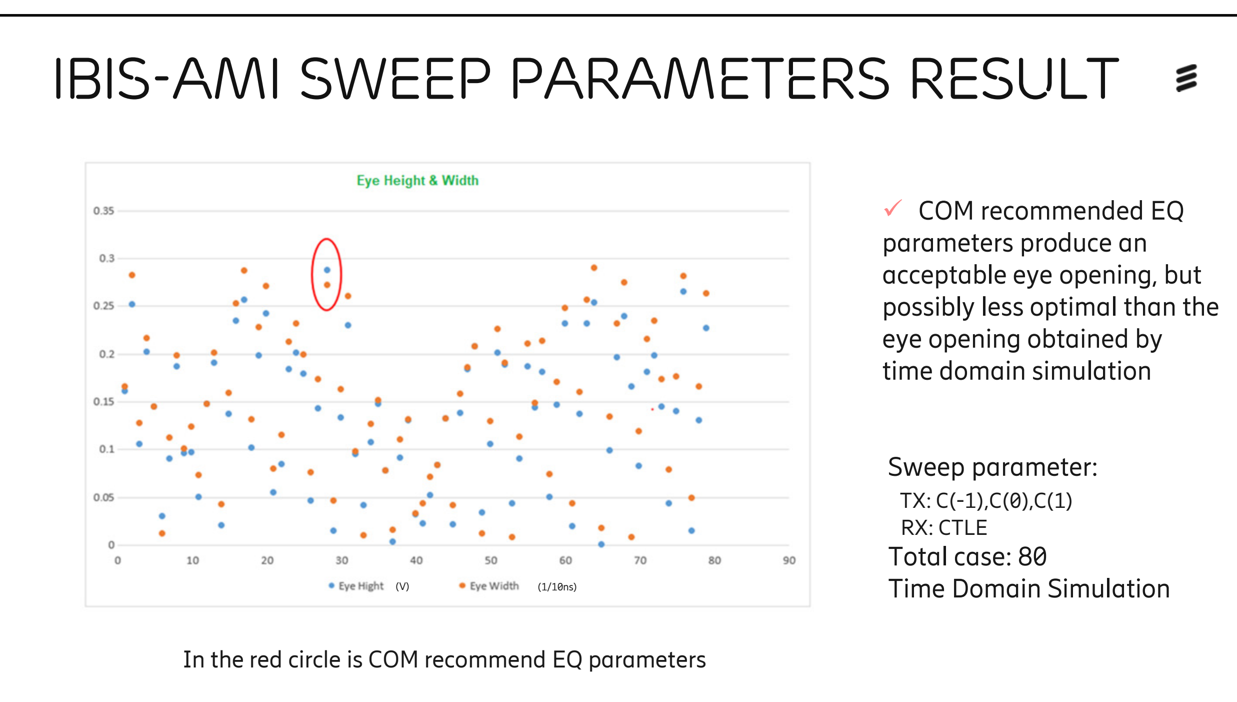
Compliance Check for Single

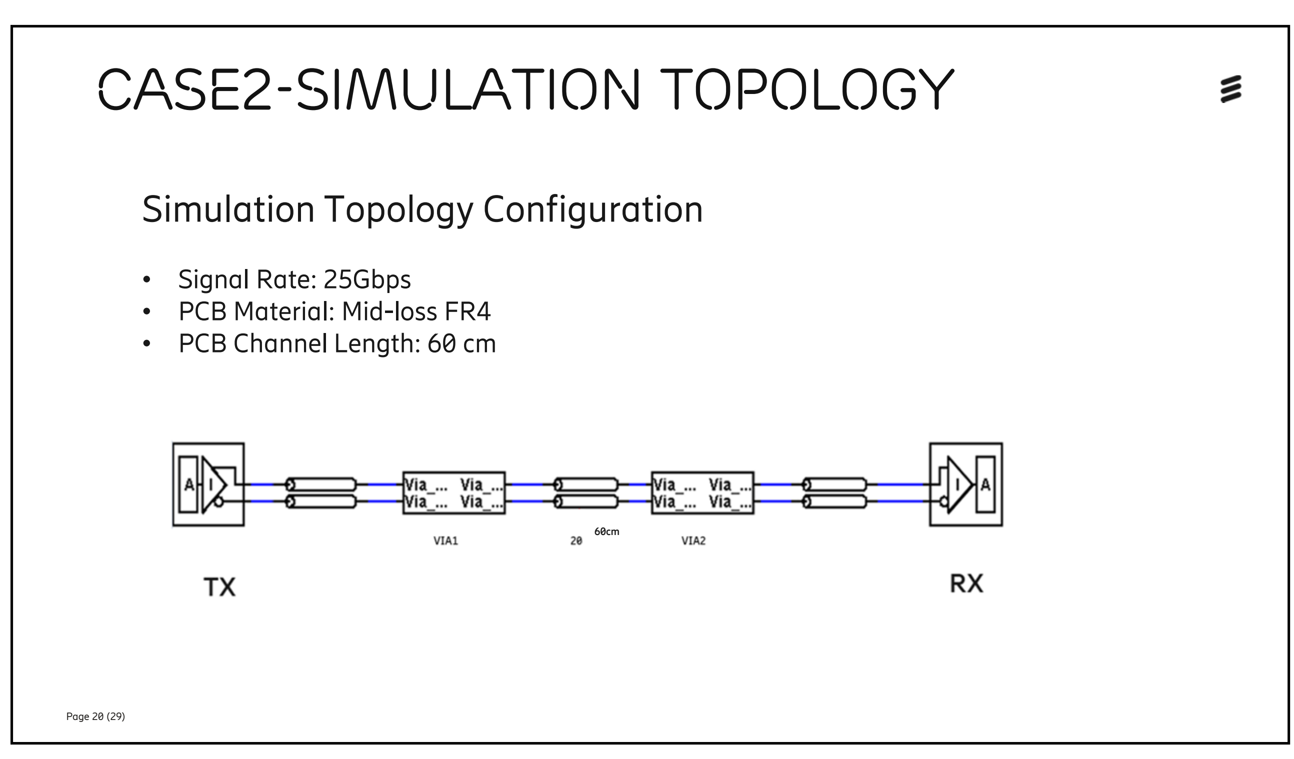
Insertion Loss — SDD21 (dB) vs. Frequency (GHz); legend: IL, Spec., Spec.

Return Loss — SDD11, SDD22(dB) vs. Frequency (GHz); legend: SDD11, SDD22, Spec.

Page 17 (29)




IBIS-AMI SWEEP PARAMETERS RESULT
Eye Height & Width
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0
10
20
30
40
50
60
70
80
90
Eye Hight (V)
Eye Width (1/10ns)
COM recommended EQ parameters produce an acceptable eye opening, but possibly less optimal than the eye opening obtained by time domain simulation
Sweep parameter:
TX: C(-1),C(0),C(1)
RX: CTLE
Total case: 80
Time Domain Simulation
In the red circle is COM recommend EQ parameters
Page 19 (29)


CASE2-SIMULATION TOPOLOGY
Simulation Topology Configuration
Signal Rate: 25Gbps
PCB Material: Mid-loss FR4
PCB Channel Length: 60 cm
VIA1
20
60cm
VIA2
TX
RX
Page 20 (29)

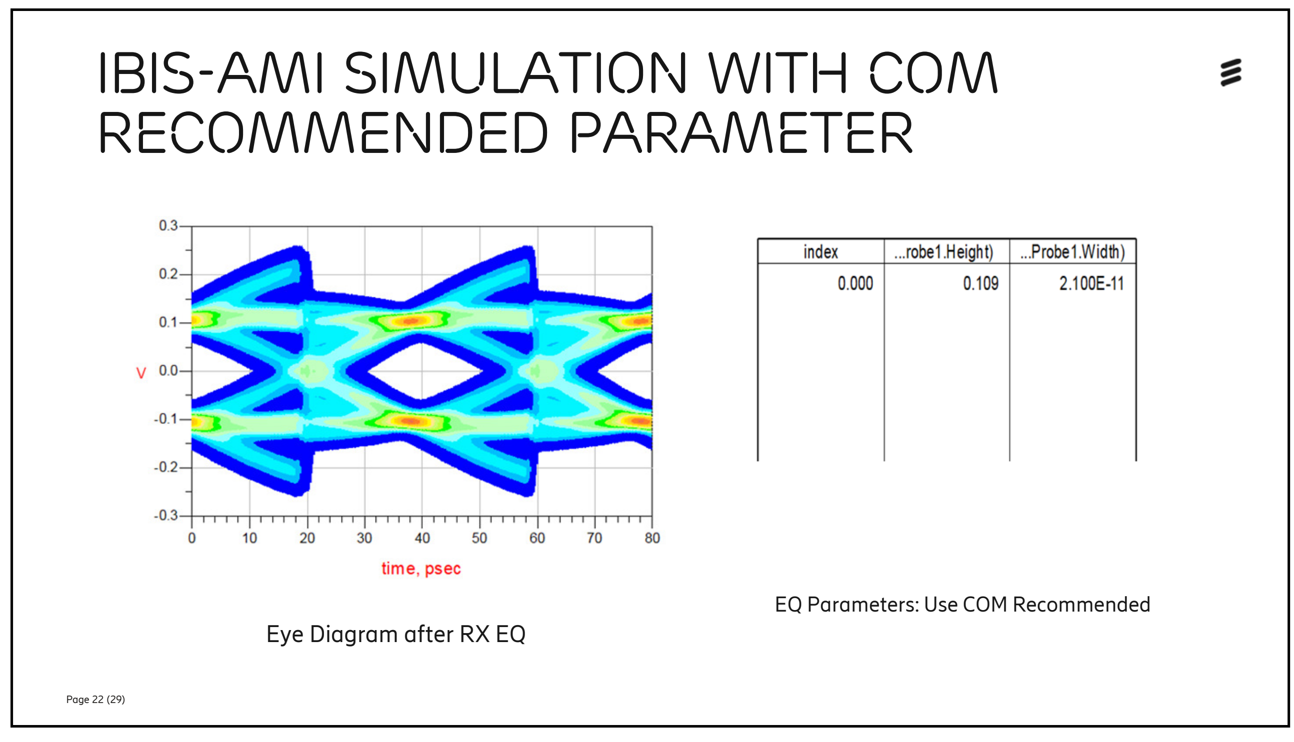
COM SIMULATION RESULT

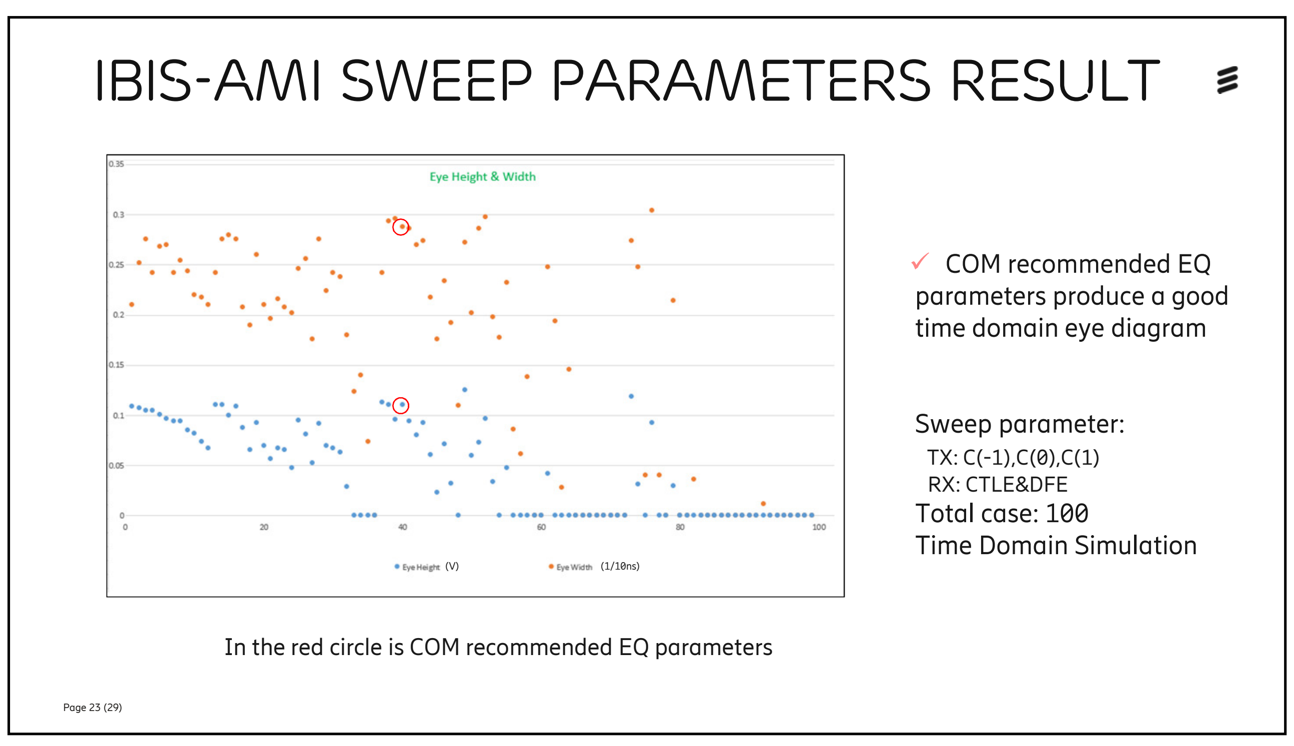
Compliance Check
S-parameter Selection
C:\s .s4p
Standard Selection
CEI-25G-LR
Run COM
Generate Report
Result Viewer
Check Item
Plot
COM
2.0448 dB
EQ Tap
TXLE_taps: "[-0.18 0.74 -0.08]"
CTLE_DC_gain_dB: -12
DFE Taps:
"[0.50272418380154;0.0414188816361097;-0.014323633127473 4;-0.000398495104593833;0.00737370694471256;0.0112097846969935;0.0169933215752706;0.0146572838013608;0.0147587713052646;0.012691147788 9632;0.0110415975235017;0.0112299536603352;0.00849681996649246;0.00854543

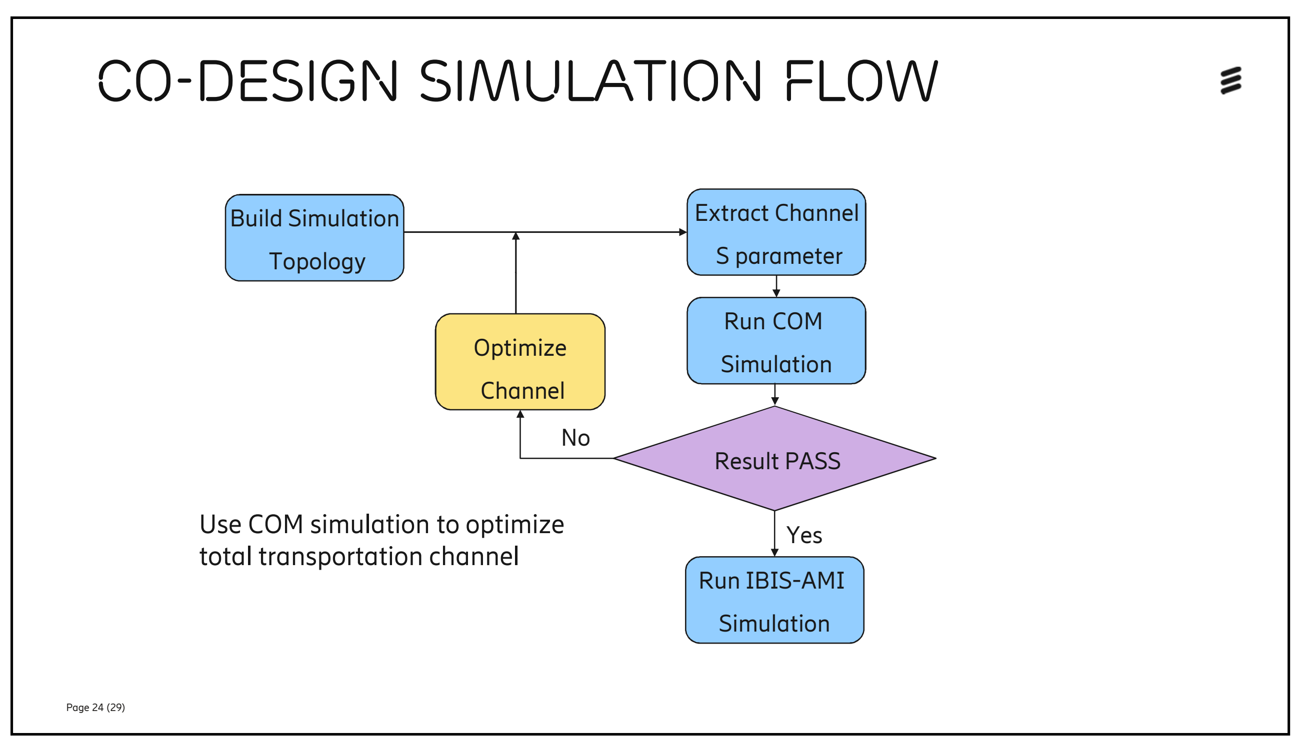
Insertion Loss
SDD21 (dB)
Frequency (GHz)
IL
Spec.
Spec.

Return Loss
SDD11, SDD22(dB)
Frequency (GHz)
SDD11
SDD22
Spec.

Page 21 (29)




IBIS-AMI SWEEP PARAMETERS RESULT
Eye Height & Width
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0
20
40
60
80
100
Eye Height (V)
Eye Width (1/10ns)
✓ COM recommended EQ parameters produce a good time domain eye diagram
Sweep parameter:
TX: C(-1),C(0),C(1)
RX: CTLE&DFE
Total case: 100
Time Domain Simulation
In the red circle is COM recommended EQ parameters
Page 23 (29)


CO-DESIGN SIMULATION FLOW
Build Simulation Topology
Extract Channel S parameter
Run COM Simulation
Optimize Channel
No
Result PASS
Yes
Run IBIS-AMI Simulation
Use COM simulation to optimize total transportation channel
Page 24 (29)

AGENDA

- Traditional IBIS-AMI
- COM Overview
- IBIS-AMI Co-design with COM for 25G
- Two example channels
- Co-simulation Conclusion
- Next Steps

Page 25 (29)

CO-SIMULATION CONCLUSION

- COM enables passive channel evaluation of high-speed signals at early design phase
- COM recommended EQ parameters are suitable for same channel in time domain simulation
- COM simulation is faster, making them more suitable for the post-layout phase of large designs to sweep EQ parameters

Page 26 (29)

AGENDA

- Traditional IBIS-AMI
- COM Overview
- IBIS-AMI Co-design with COM for 25G
- Two example channels
- Co-simulation Conclusion
- Next Steps

NEXT STEPS

- Model crosstalk in actual link
- Co-simulation for 56G PAM-4
- Accuracy of IBIS-AMI model
- Correlation of Co-simulation with measurement