**AGENDA - Asian IBIS Summit (Tokyo)**

**Monday, November 12, 2018**

Akihabara UDX

Tokyo, Japan

Room: **4F NEXT1**

Sponsors: **Japan Electronics and Information Technology Industries Association (JEITA)**

**IBIS Open Forum**

**ANSYS, Inc.**

**Apollo**

**Cadence Design Systems**

**Cybernet Systems**

**Keysight Technologies**

**Ricoh**

**Toshiba Corporation**

**Zuken, Inc.**

*(Order and times subject to change)*

13:00 **SIGN IN**

13:05 **MEETING** **WELCOMES**

* Mike LaBONTE (SiSoft, USA)  
   Chair, IBIS Open Forum
* Miyo KAWATA (ANSYS Japan K.K., Japan)  
   Chair, JEITA EDA Model Subcommittee

13:10 **JEITA EDA Model Specialty Committee Report**

Miyo KAWATA (ANSYS Japan K.K., Japan)

13:15 **IBIS Update**

Mike LaBONTE (SiSoft, USA)

13:25 **Package Models for Critical Timing Validation with IBIS**

Yukio MASUKO (Japan Electronics Packaging and Circuits Association  
(JPCA), Japan)

13:50 **Best Case Analysis**

Shinichi MAEDA (KEI Systems, Japan)

14:15 **A Practical Methodology for SerDes Design**

Amy ZHANG\*, Guohua WANG\*, David ZHANG\*, Zilwan MAHMOD\*, Anders EKHOLM\*\*

(Ericsson, \*China, \*\*Sweden)

*[Presented by Anders EKHOLM (Ericsson, Sweden)]*

14:45 **Model Correlation for IBIS-AMI**

Wenyan XIE\*, Guohua WANG\*, David ZHANG\* Anders EKHOLM\*\*

(Ericsson, \*China, \*\*Sweden)

*[Presented by Anders EKHOLM (Ericsson, Sweden)]*

15:20 **BREAK**

* Reconvene at 15:40

15:40 **Concerns when Applying Channel Simulation to DDR Interface**

Masaki KIRINAKA, Akiko TSUKADA (Fujitsu Interconnect Technologies Limited, Japan)

*[Presented by Masaki KIRINAKA (Fujitsu Interconnect Technologies Limited, Japan)]*

16:05 **Simulation Technology for Memory Designers in DDR4/5**

Satoshi NAKAMIZO (Keysight Technologies, Japan)

16:30 **Study of DDR Asymmetric Rt/Ft in Existing IBIS-AMI Flow**

Wei-kai SHIH\*, Wei-hsing HUANG\*\*; SPISim (\*Japan, \*\*USA)

*[Presented by Wei-kai SHIH (SPISim, Japan)*

16:55 **Study on Potential Feature Additions for Bit-by-bit Simulation Technique to  
Address the DDR5 Requirements**

Ted MIDO (Synopsys, Japan)

17:25 **CONCLUDING ITEMS**

17:35 **END OF IBIS SUMMIT MEETING**

* ****Thank you for your participation