EIAJ-IMIC

I/0 Interface Model for Integrated Circuits

I/0 Interface Model Project Group
Technical standardization on Semiconductor Devices
Electronic Industries Association of Japan (EIAJ)
http://tsc.eiaj.or.jp

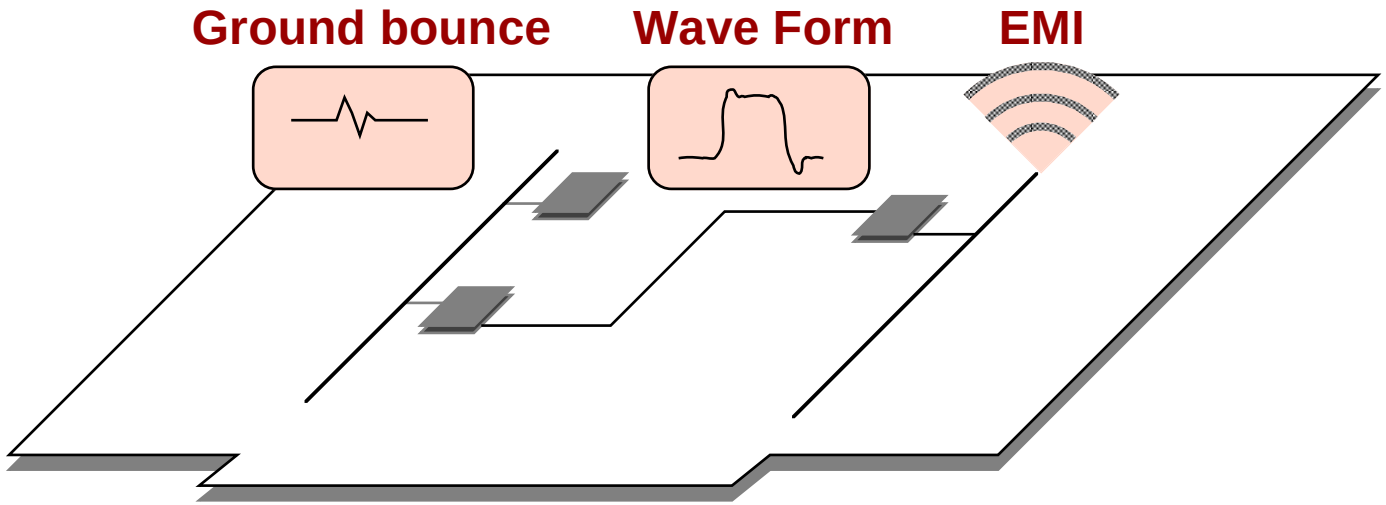
Content

1. Background and issues
2. Overview of EIAJ-IMIC
3. Application of the model and simulation results
4. Future work
5. Conclusion

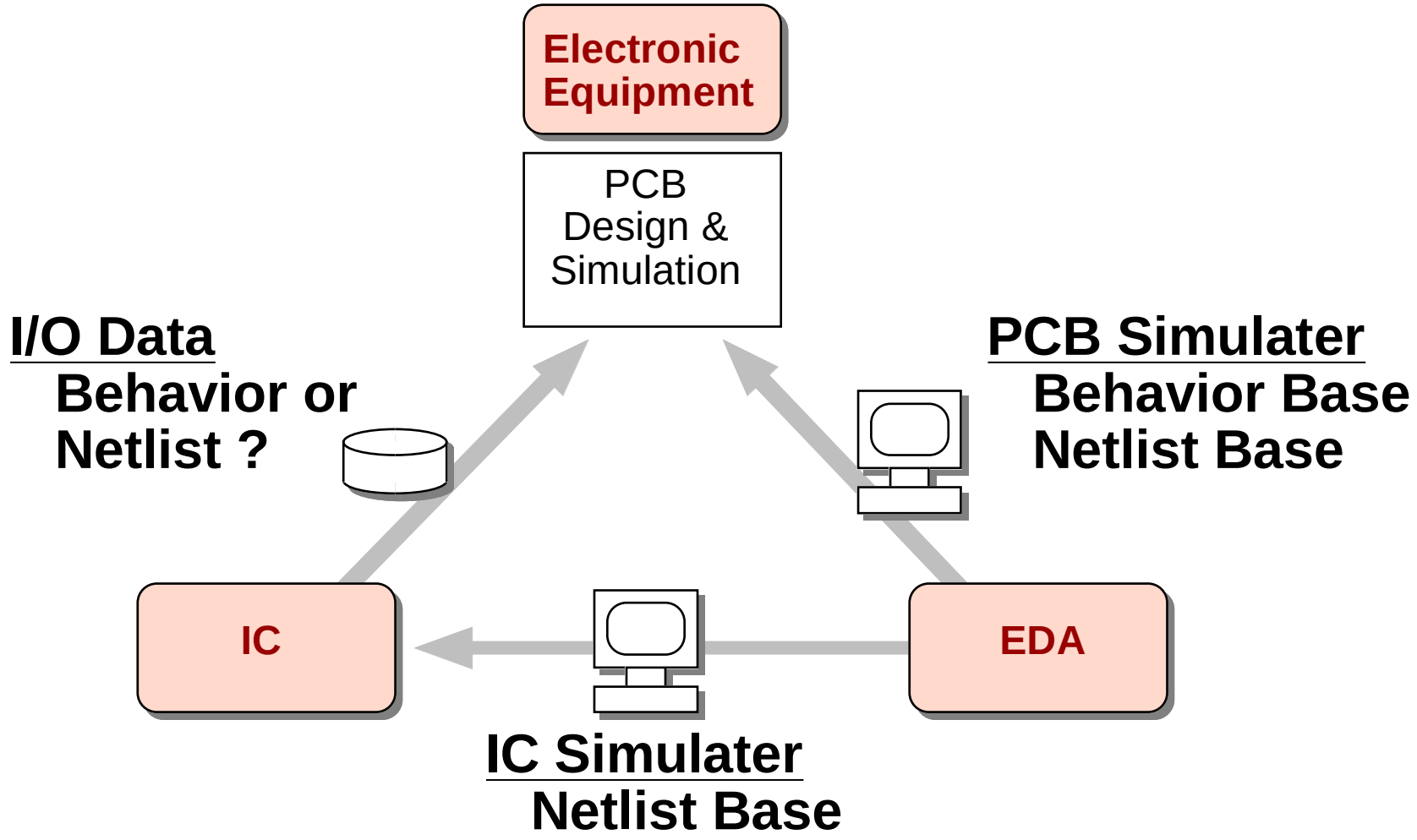
Background

- **Higher speed in system interface**
- **Simulation in printed circuit board design**
- **Increased requirements for electrical data of components**

--> Pioneering standardization activity : *"IBIS"*



Environment of PCB Simulation



Issues

- There are two types of PCB simulator ;
  Behavior base and Netlist base.
  Which type of I/O data should be supplied by IC vendors?

- IBIS approaches from behavior type.
  Are IC vendors supplying it easily?
  Are users satisfied with it?

- EIAJ-IMIC approaches from netlist type.
  How and by whom is it converted for behavior base PCB simulator?

Requirement to IMIC

- To keep description capability of circuits and accuracy of simulation results comparing with SPICE.
- To protect process and circuits information of ICs.
- To improve simulation speed.

Content

Scope

To standardize electrical model of input and output signals, power supply and ground terminals of integrated circuits in order to provide for analysis of electrical characteristic of equipment using them.

In the work, the following items shall be considered.

(1) To standardize in order to solve current problems and in order to extend capabilities of analysis, on the basis of results of the past standardization activities

(2) To make description rules for electrical circuits more flexible to solve the problems

(3) To introduce the concept of modelling levels to exchange relevant data for each application

(4) To enhance electrical modelling for packages and modules

Organization

Electronic Industries Association of Japan (EIAJ)

Technical Standardization Center

- **Committee on Semiconductor Devices**
  - ***I/O Interface Model Project Group***
  - ***Package Electrical Characterization Project Group***
- **Committee on Semiconductor Packages**

Members

Hideki Fukuda / Hitachi, Leader

Takeshi Watanabe / NEC, Sub-leader

Shinji Tanabe / Oki

Yuki Hashimoto / Oki

Toshiya Takahashi / Kawasaki Steel

Koichi Abe / Kawasaki Steel

Hidetoshi Mizutani / Sanyo

Nobuhiro Okano / Sharp

Tsuyoshi Horigome / Shindengen

Fumito Ikeda / Seiko Epson

Kimio Terada / Toshiba

Yuichiro Yoshida / Toshiba

Saburo Hojo / Hitachi

Masanori Shimasue / HP Japan

Noriaki Ogushi / Fujitsu

Takashi Hirata / Matsushita

Tomoo Ishida / Mitsubishi

Nobuaki Tsuji / Yamaha

Norio Matsui / Applied Simulation Tech.

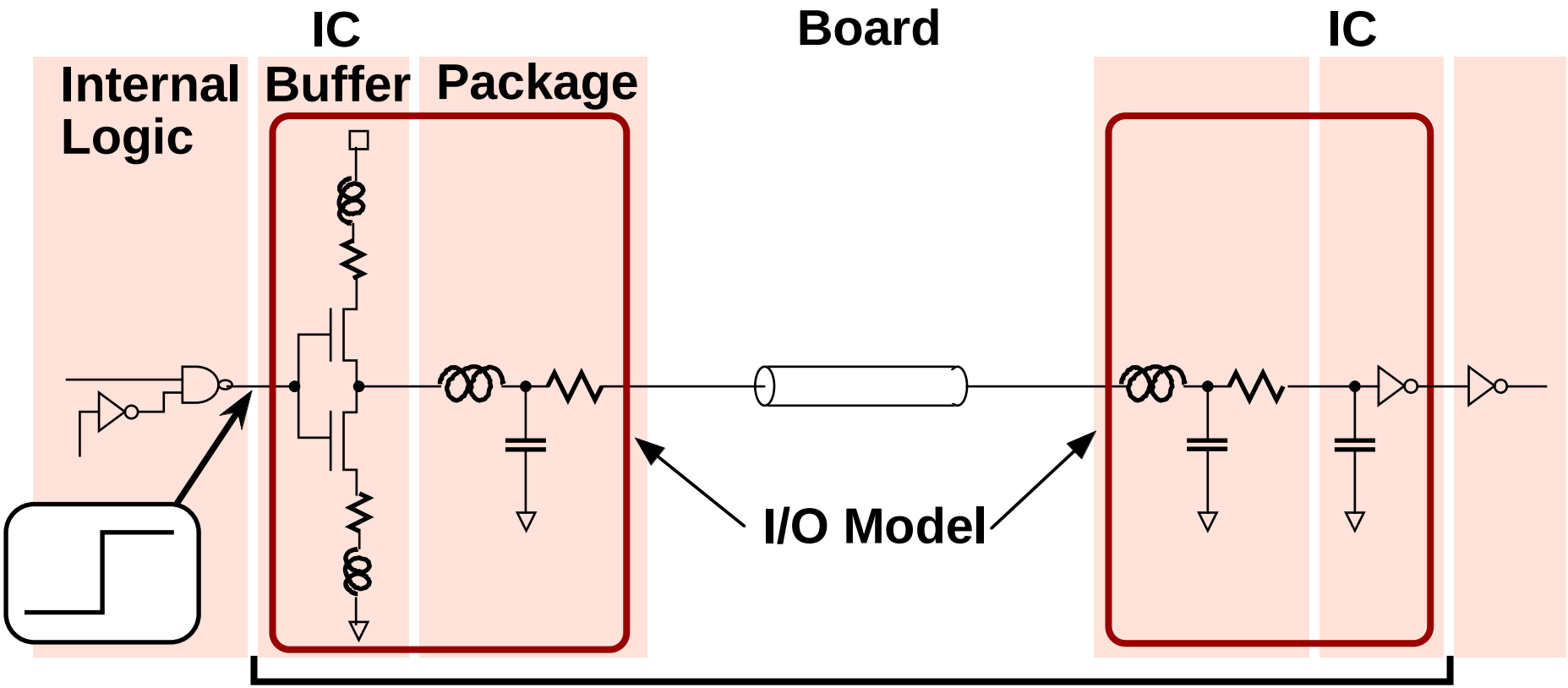
Akira Ohta / Inotech

Kenji Mori / Zuken

History

8 / '96	Start
12 / '96	Fix Draft v0.0 (Overview)
2 / '97	Release Draft v0.0
3 / '97	Introduce at IBIS Meeting
6 / '97	Update at IBIS Meeting
12 / '97	Fix Draft v1.0
1 / '98	Update at IBIS Meeting
3 / '98	Release Draft v1.1
5 / '98	Open Home Page
6 / '98	Update at IBIS Meeting
10 / '98	Have Meeting with IBIS Members
5 / '99	Have Meeting with IBIS Members
6 / '99	Release Draft v1.2

Model Overview

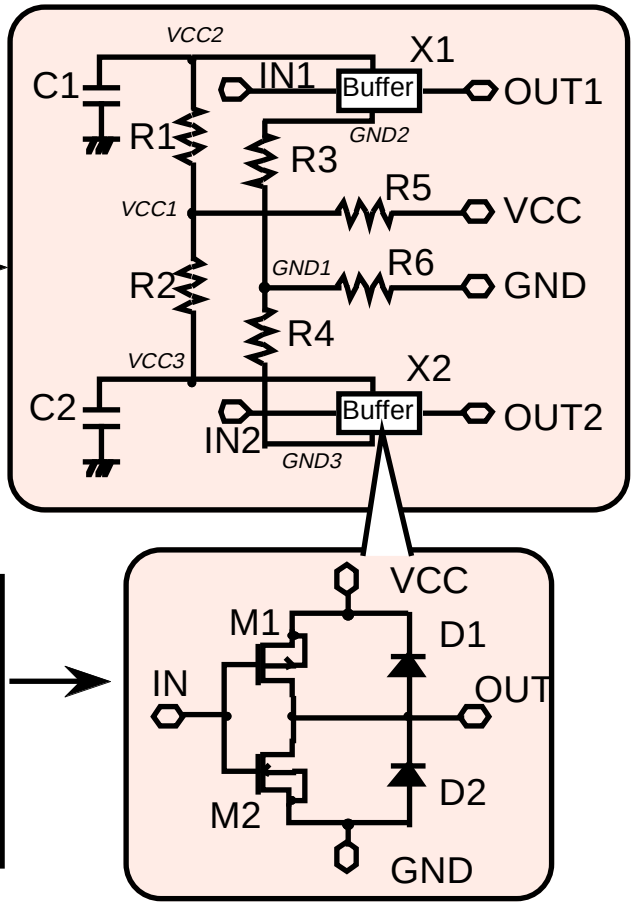


- A part or all of I/O buffer circuits are described as netlist.
- Netlists of buffer, package and board are merged for simulation.
- Description of power/ground circuit allows bounce analysis.

Model Description

Elements and interconnections are described in *SPICE format*
i.e.) power/ground lines, packages, memory modules

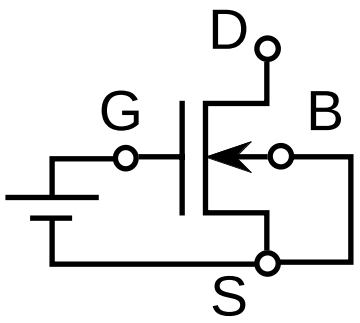
```
[Circuit Connection]
R1 VCC1 VCC2 1.0
R2 VCC1 VCC3 1.2
R3 GND1 GND2 1.1
R4 GND1 GND3 0.9
R5 VCC1 VCC  0.5
R6 GND1 GND  0.5
C1 VCC2  0   1P
C2 VCC3  0   1P
X1 IN1 OUT1 VCC2 GND2 BUFFER
X2 IN2 OUT2 VCC3 GND3 BUFFER
.SUBCKT BUFFER IN OUT VCC GND
M1 IN OUT VCC VCC PMOS L=1U W=10U
M2 IN OUT GND GND NMOS L=1U W=10U
D1 OUT VCC D AREA=2
D2 GND OUT D
.ENDS BUFFER
```



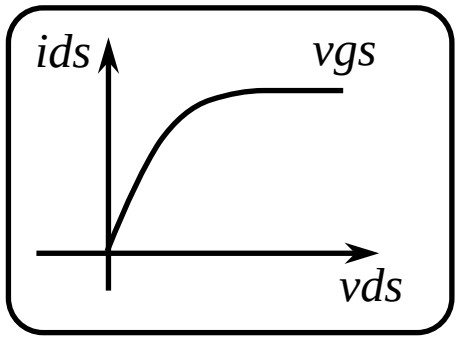
MOS Device Model (1)

1-dimensional table model

for such as switch MOS transistor



Vds = variable
Vgs = const.
Vbs = const.



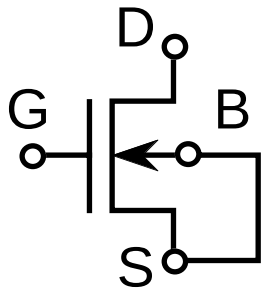

```
.MODEL MODEL2 NMOS MODEL=TABLE
+ L=0.8U W=10U AD=100P AS=100P
+ DATA=CHANNEL
+ VBS=0 VGS=3.3
+  0.0   2.0m   0.5n   0.5n   3.5n
+  0.2   3.0m   0.5n   0.5n   3.5n
+  0.5   4.0m   0.5n   0.5n   3.5n
+   .     .      .      .      .
+   .     .      .      .      .
```

Vds Ids Cgs Cgd Cgb

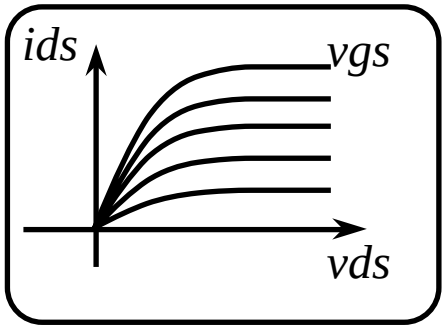
MOS Device Model (2)

2-dimensional table model

for such as slew rate control MOS transistor



Vds = variable
Vgs = variable
Vbs = const.



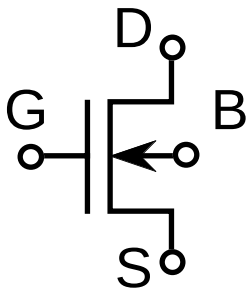

```
.MODEL MODEL2 NMOS MODEL=TABLE
+ L=0.8U W=10U AD=100P AS=100P
+ DATA=CHANNEL
+ VBS=0
+ 0.05   0.0   2.0m   0.5n   0.5n   3.5n
+ 0.05   0.2   3.0m   0.5n   0.5n   3.5n
+ 0.05   0.5   4.0m   0.5n   0.5n   3.5n
+   .      .     .      .      .
+   .      .     .      .      .
```

Vgs Vds Ids Cgs Cgd Cgb

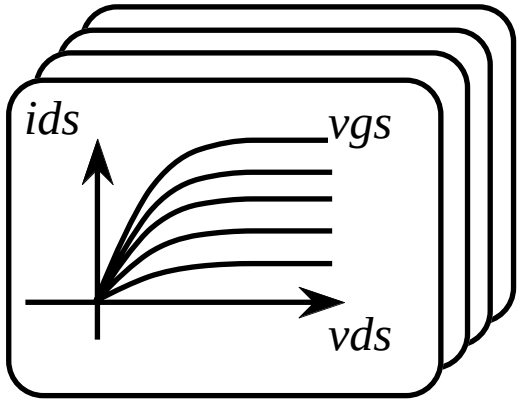
MOS Device Model (3)

3-dimensional table model

for such as transfer gate MOS transistor



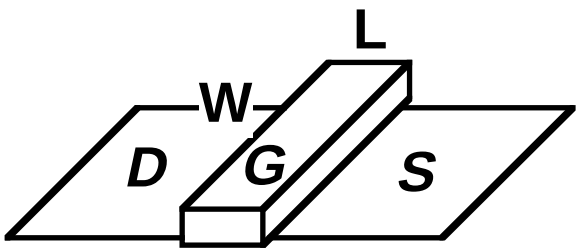
Vds = variable
Vgs = variable
Vbs = variable

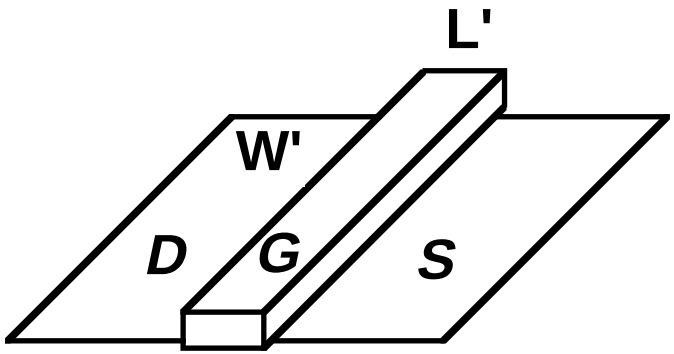


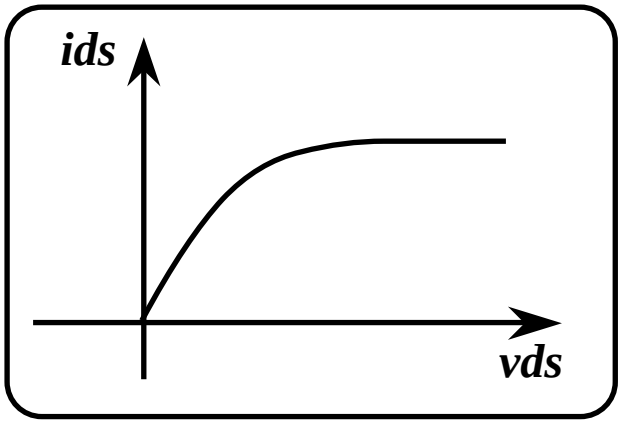

```
.MODEL MODEL2 NMOS MODEL=TABLE
+ L=0.8U W=10U AD=100P AS=100P
+ DATA=CHANNEL
+ 0.05   0.0   0.0   2.0m   0.5n   0.5n   3.5n
+ 0.05   0.2   0.1   3.0m   0.5n   0.5n   3.5n
+ 0.05   0.5   0.2   4.0m   0.5n   0.5n   3.5n
+   .     .     .      .      .
+   .     .     .      .      .
```

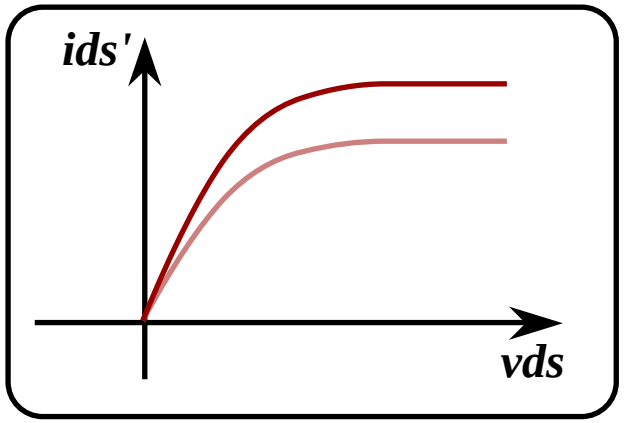
Vgs Vds Vbs Ids Cgs Cgd Cgb

MOS Geometric Dependence









MOS characteristics

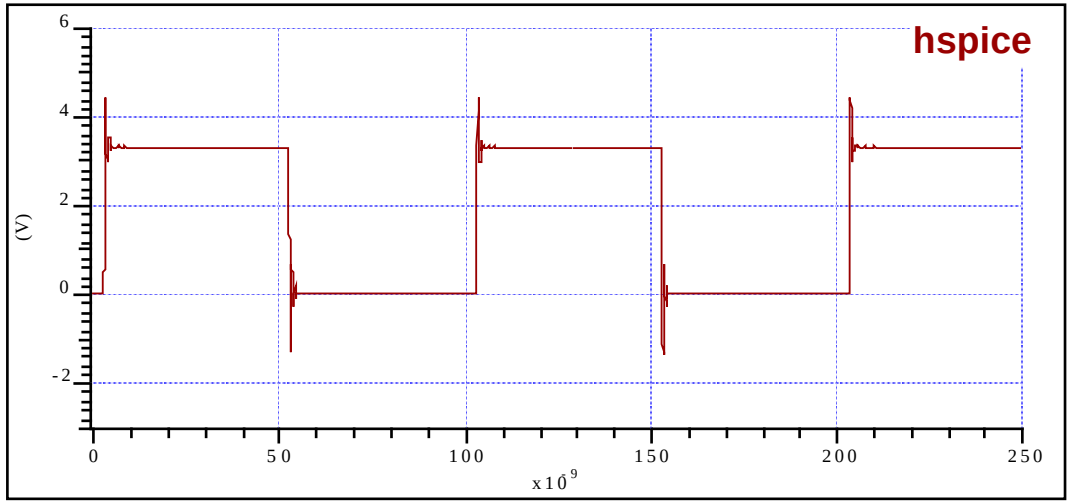
$$Ids' = Ids\left(\frac{L}{L'}\right)\left(\frac{W'}{W}\right)$$

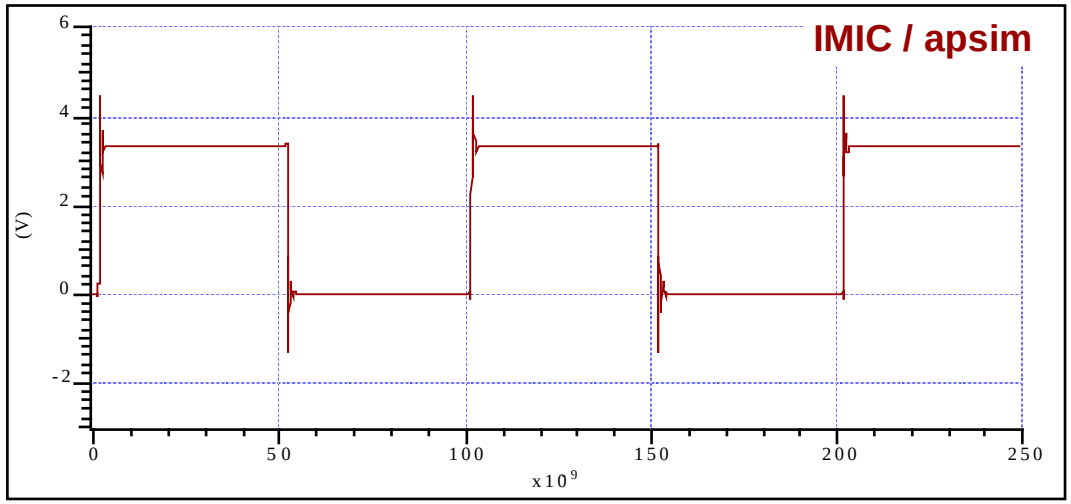
Model Level

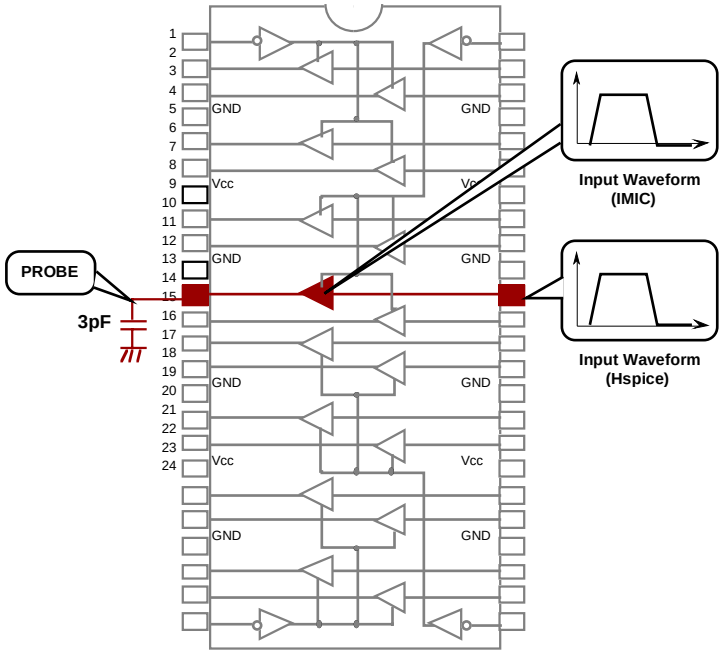
Level	Object	Simulation
1	Signal Integrity (SI)	To analyze signal waveform. - Light load to simulator
2	Power Integrity (PI)	To analyze power/ground bounce and EM emmision from boards. - Large size of circuits containing many parasitic LCRs - Heavy load to simulator
3	EMI	To analyze EM emission from package itself. (Future Problem)

Content

Simulation Result (1) - Signal Integrity - Cl = 3pF

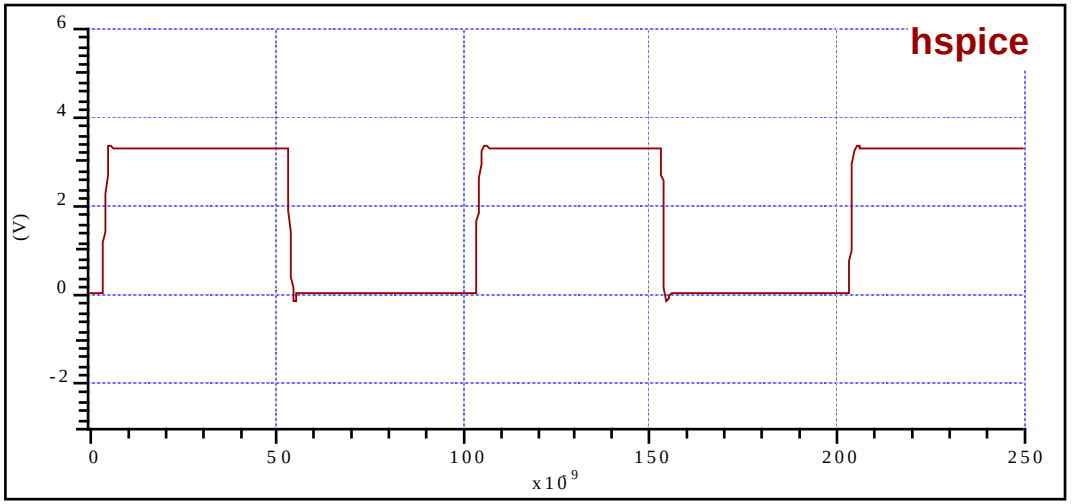


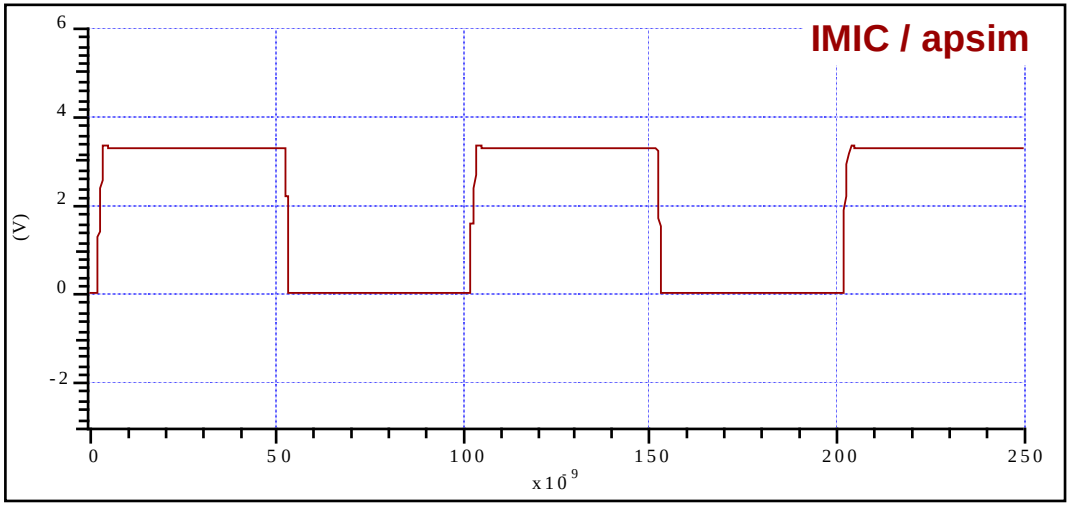


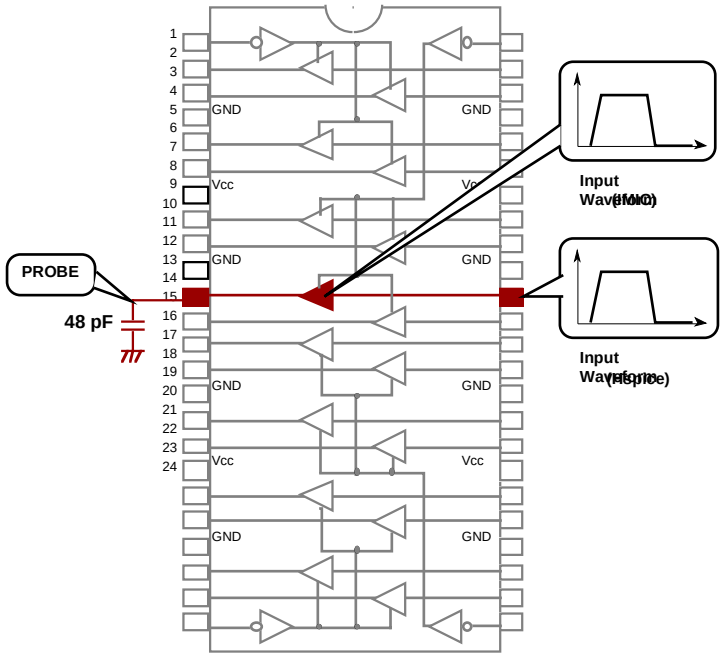


Computing TIme : 4.9 sec (IMIC)

Simulation Result (2) - Signal Integrity - Cl = 48pF

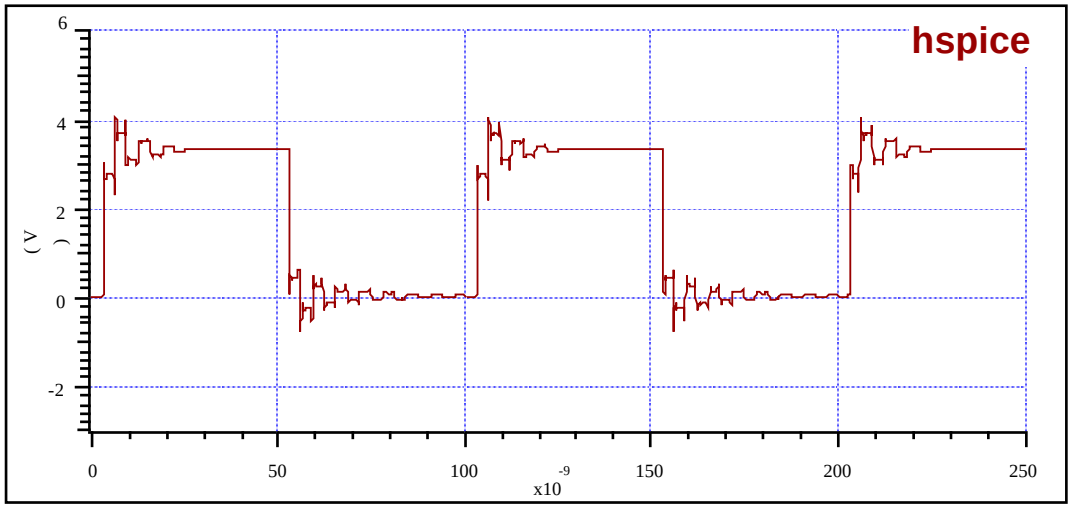


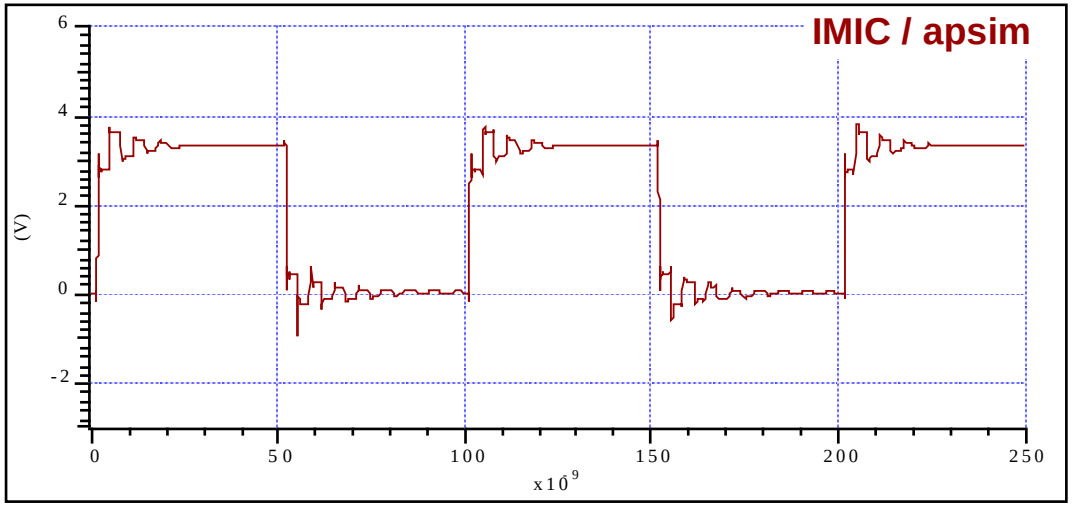


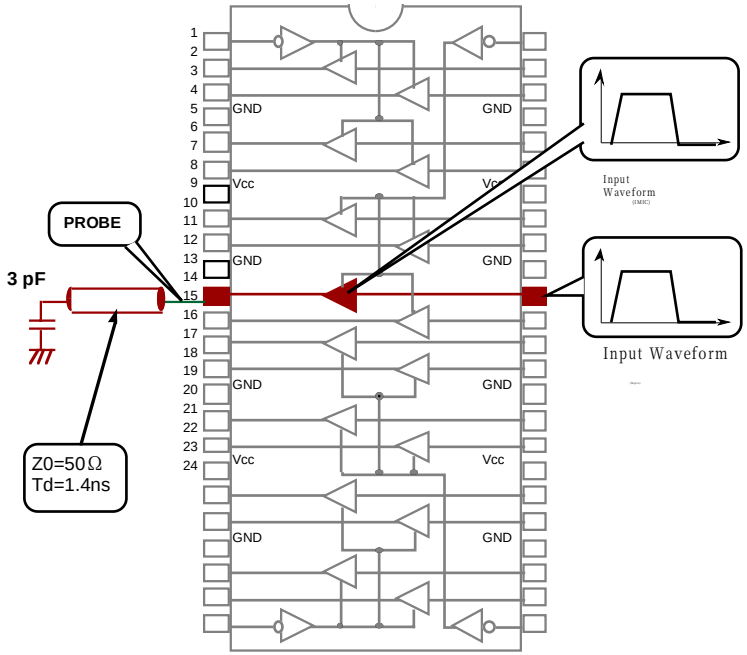


Computing TIme : 4.9 sec (IMIC)

Simulation Result (3) - Signal Integrity - Cl : Transmission Line



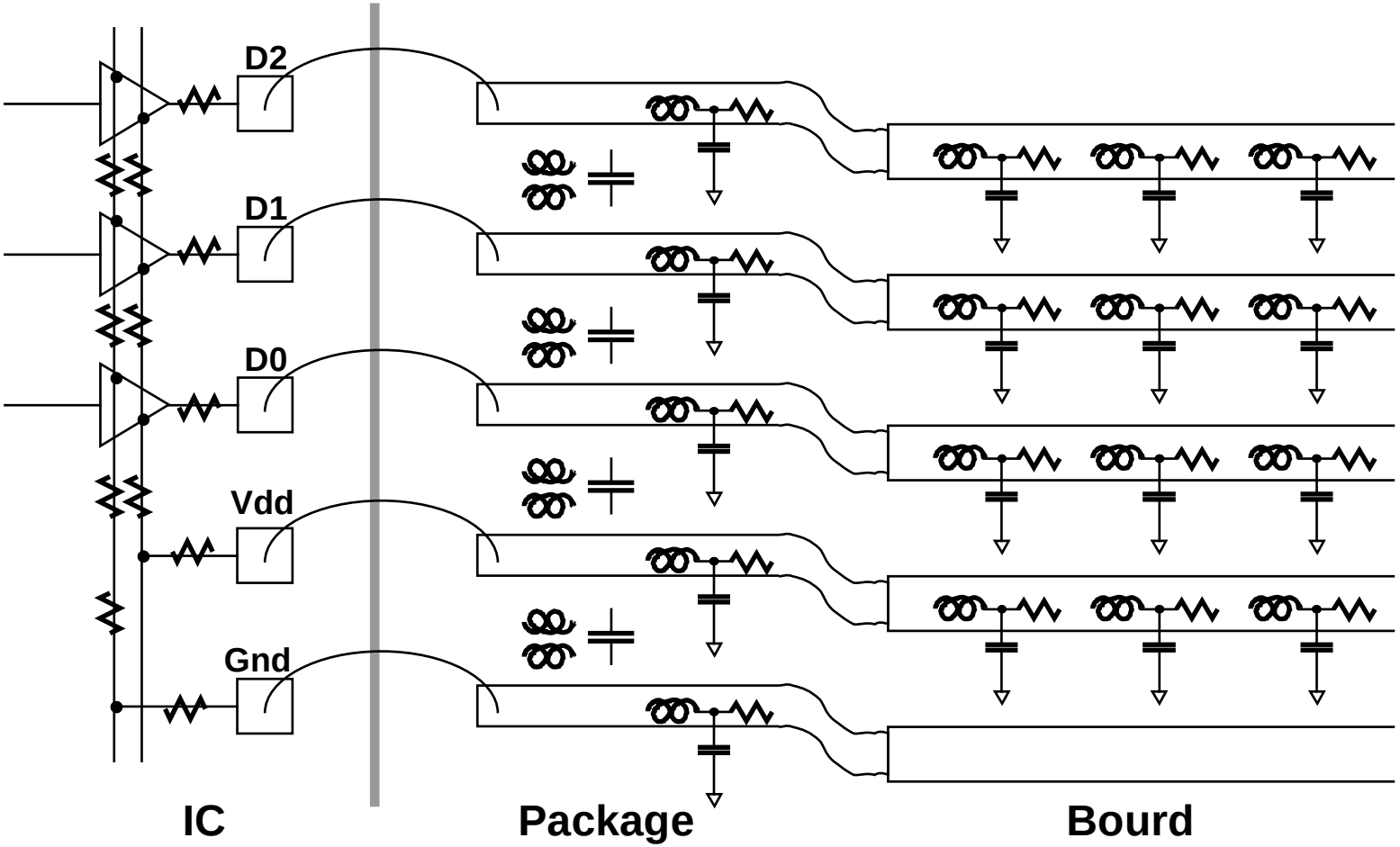




Computing TIme : 6.8 sec (IMIC)

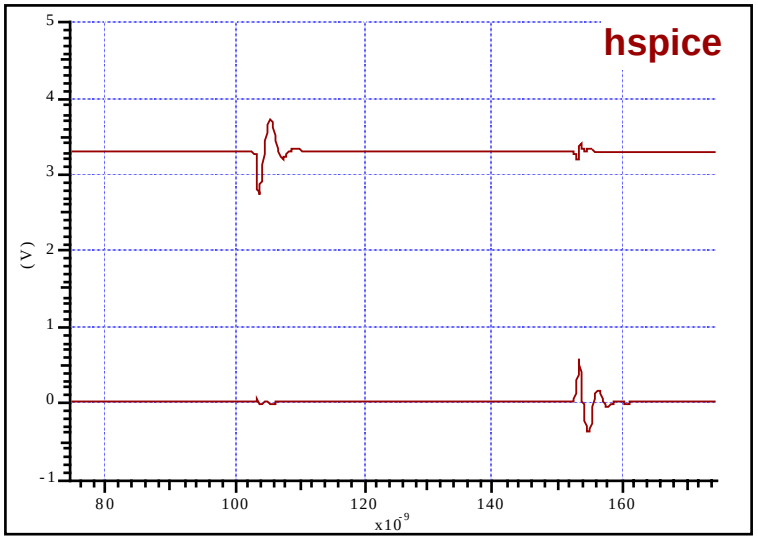
Power/Ground Noise

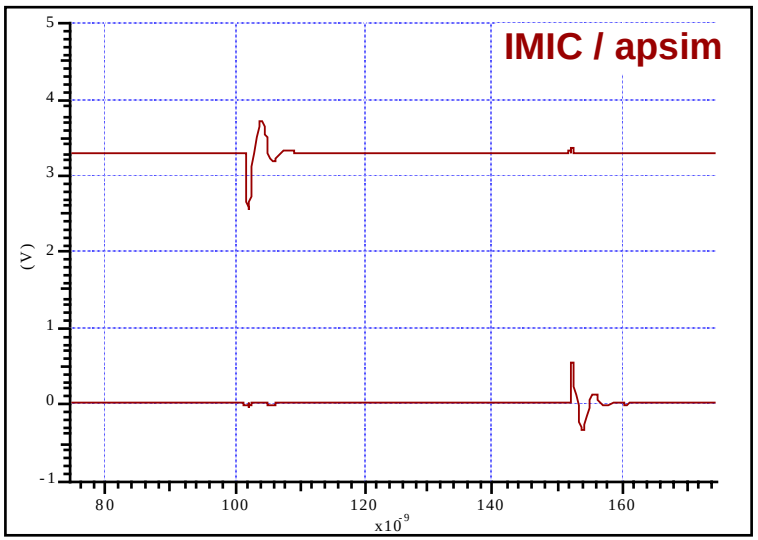
Simultaneous switching of bus line generates noise through power/ground line.

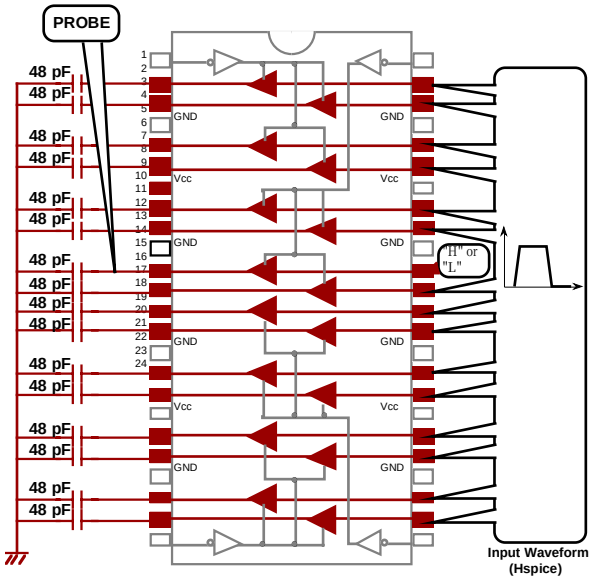


Simulation Result (4) - Power Integrity -

15 Buffers Switched, Package Model without Mutual Inductance

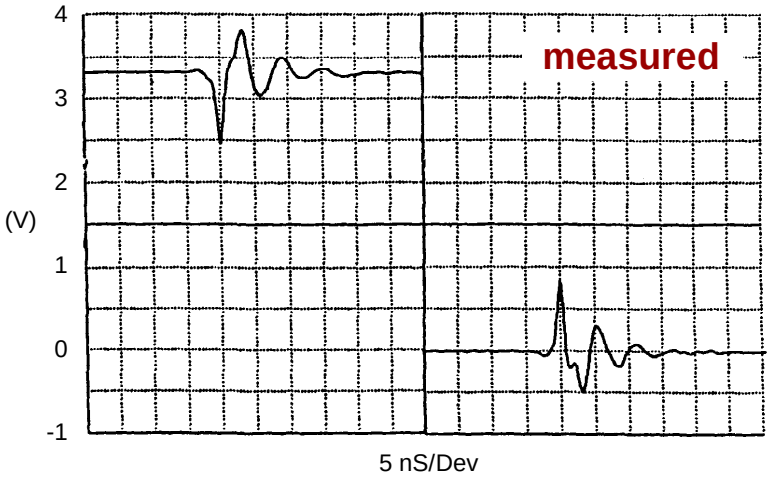






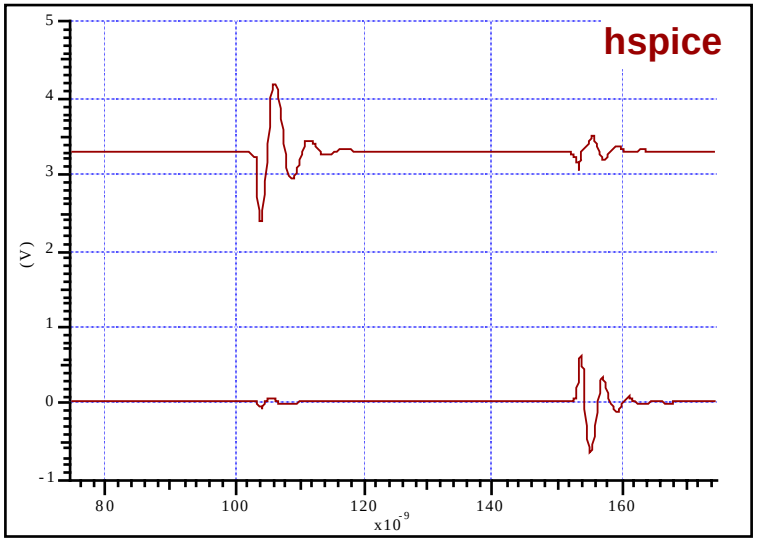
Computing TIme ("Hi" Side)

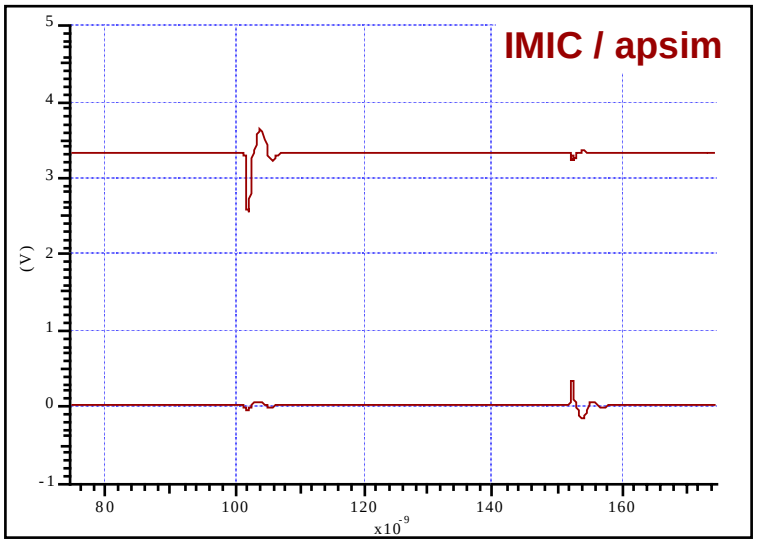
4.3 min (hspice)
1.4 min (IMIC)

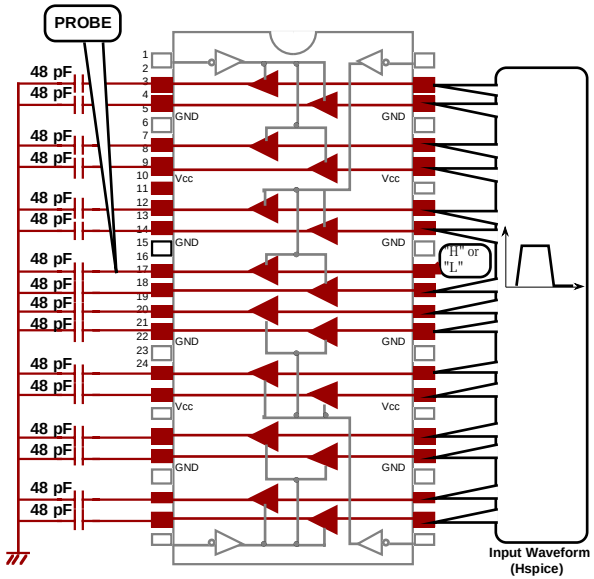


Simulation Result (5) - Power Integrity -

15 Buffers Switched, 1/4 Package Model

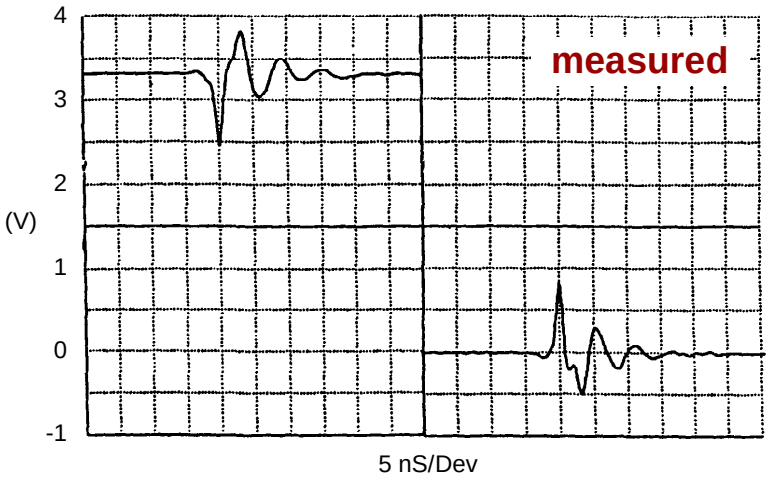






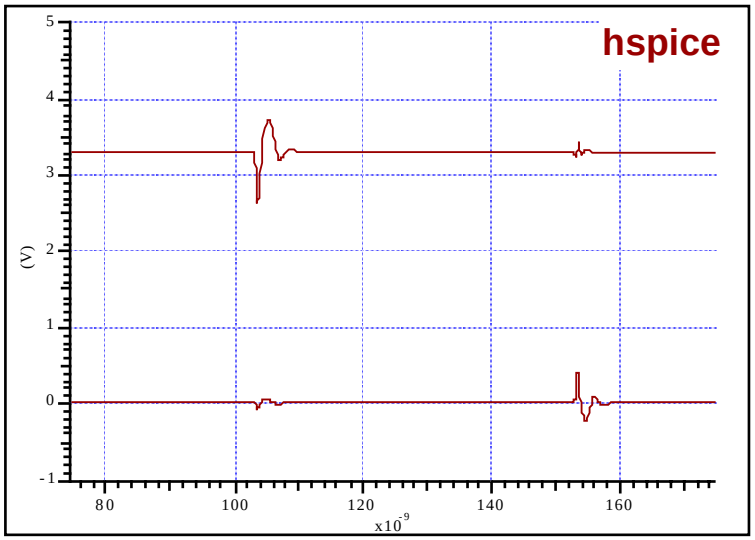
Computing TIme ("Hi" Side)

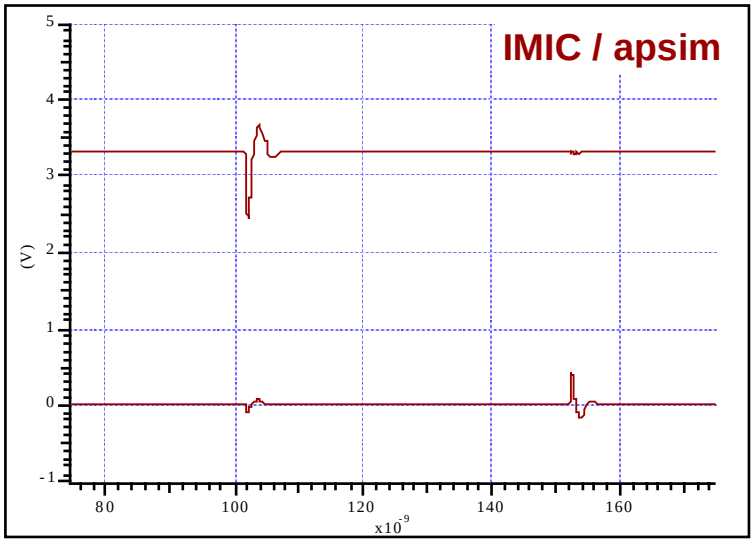
9.8 min (IMIC)

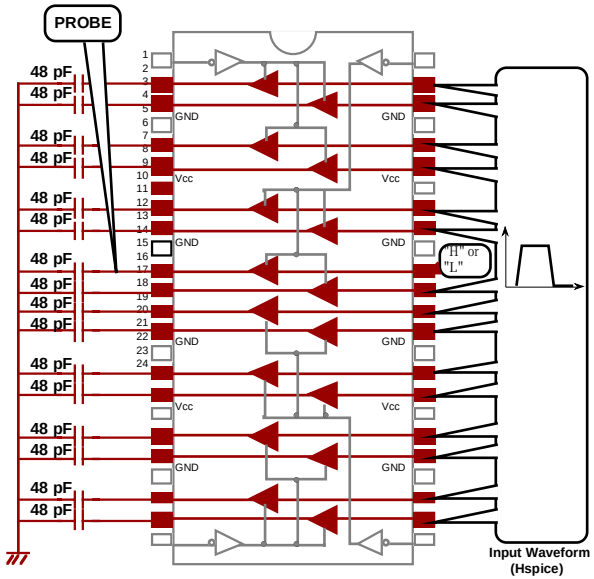


Simulation Result (6) - Power Integrity -

15 Buffers Switched, Full Package Model

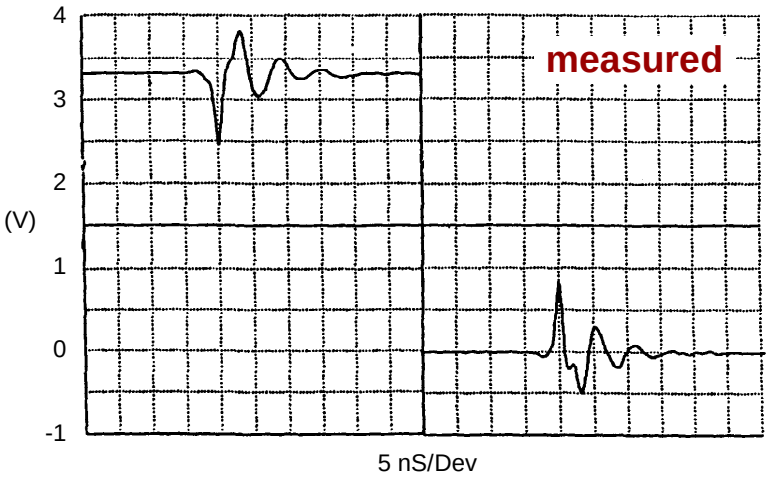






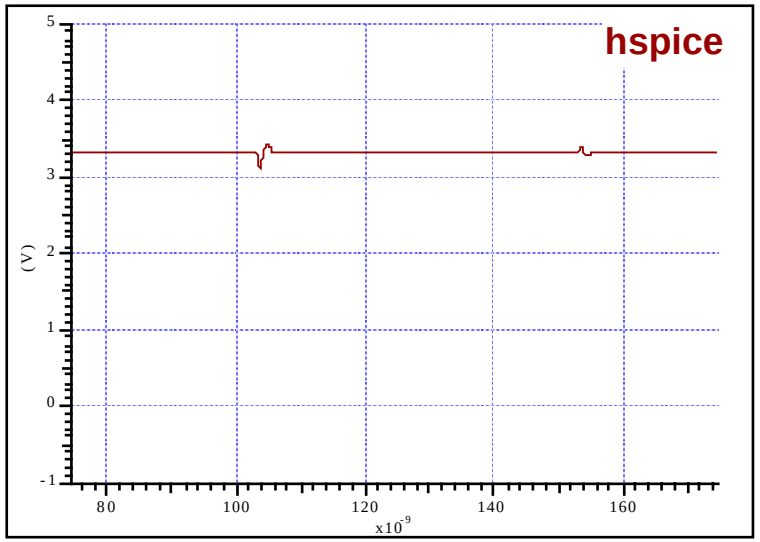
Computing TIme ("Hi" Side)

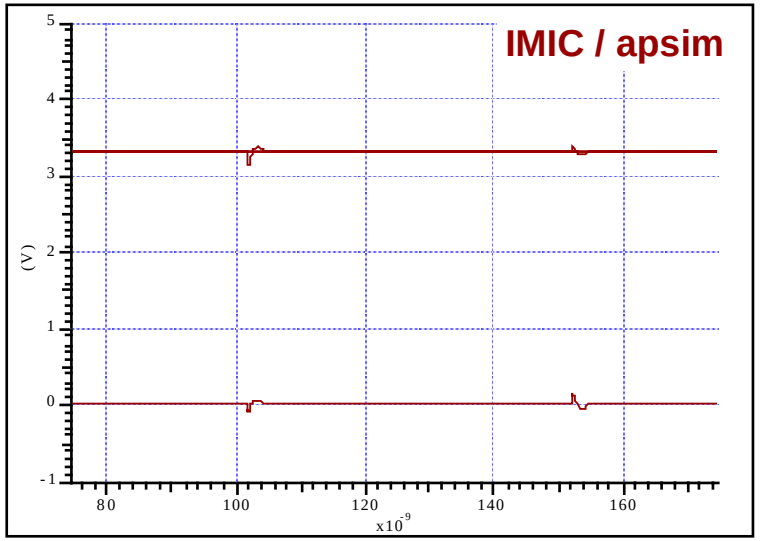
7.2 hr (hspice)
24.8 min (IMIC)

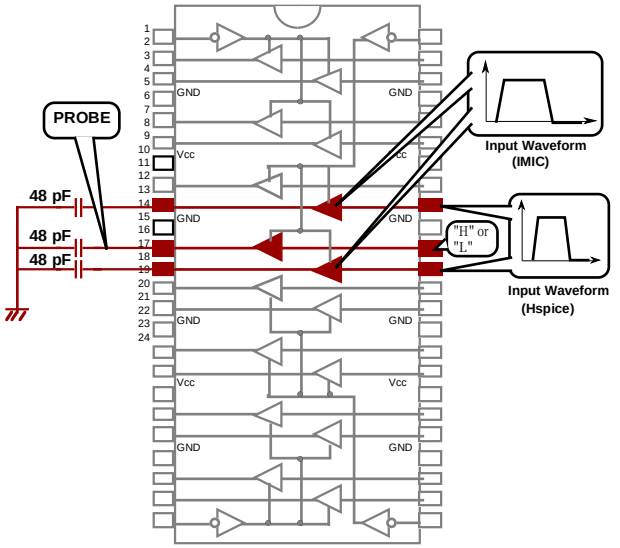


Simulation Result (7) - Power Integrity -

2 Buffers Switched, Full Package Model

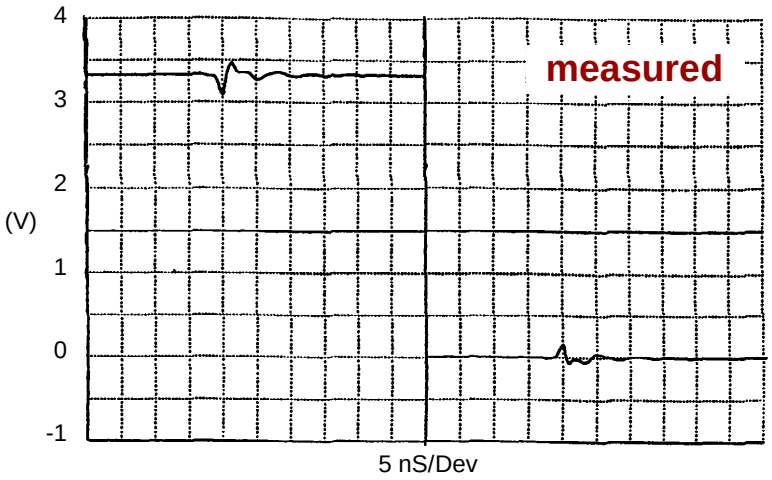






Computing TIme ("Hi" Side)

24.5 min (IMIC)



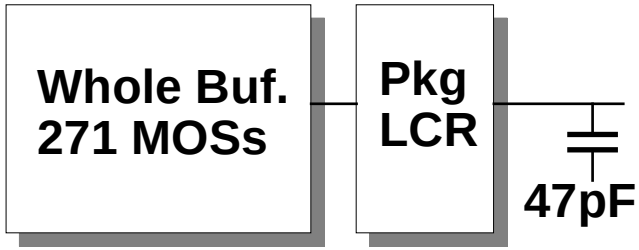
Experiment

PCI buffer TEG

- array of 14 PCI (5volts) buffers
- 160 QFP package
- 47pF load

Netlist

- circuits on silicon; extracted by LVS
- package LCR ; measured

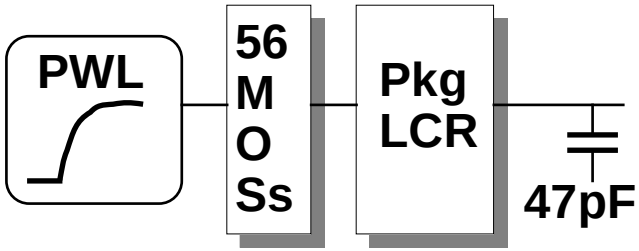


Experiment cases

- 1, 5, 10 buffer(s) switched simultaneously
- rise, fall

Signal / noise observation

- measurement
- HSPICE whole buffer circuits
- HSPICE a part protected
- IMIC / Apsim

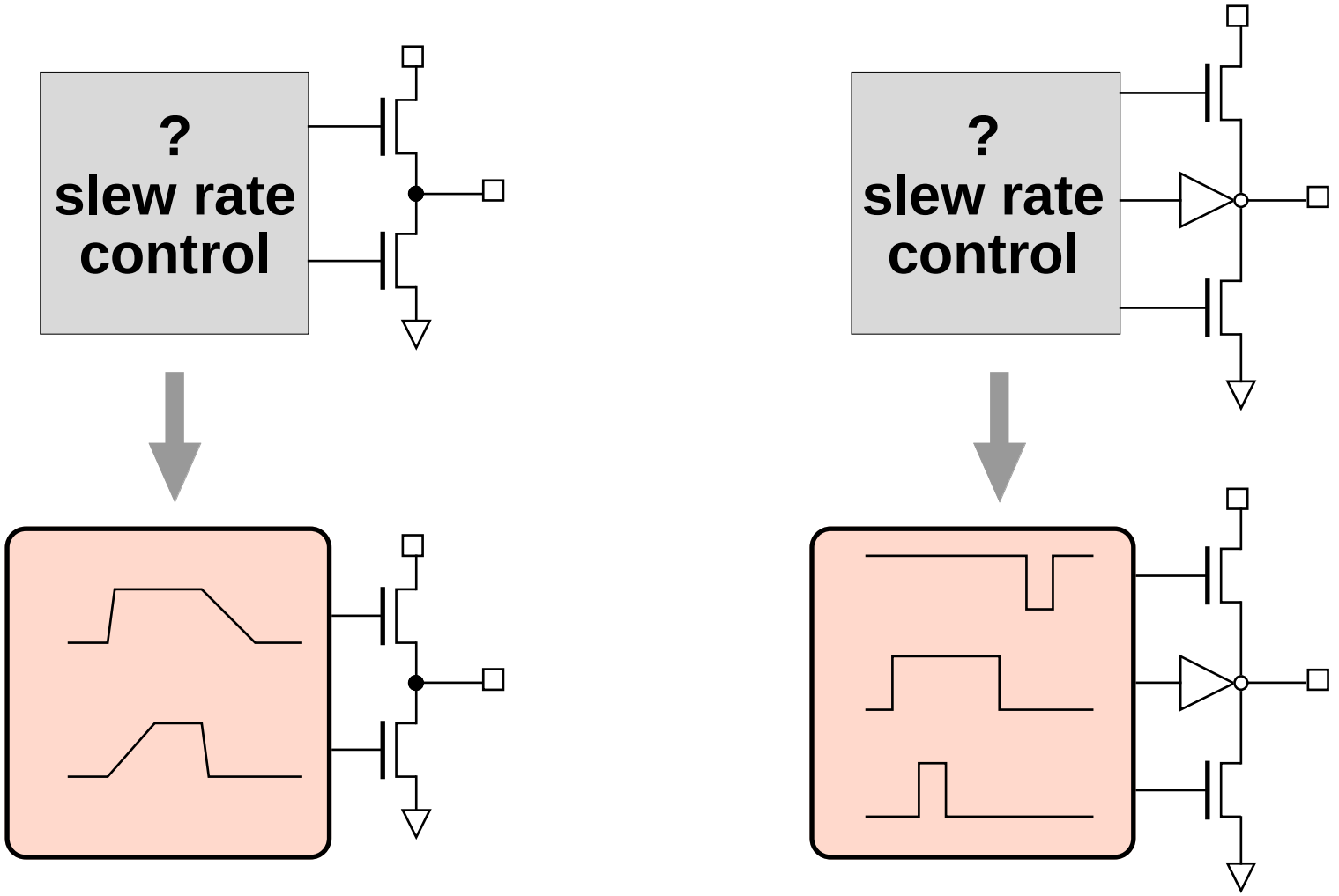


Monitoring points

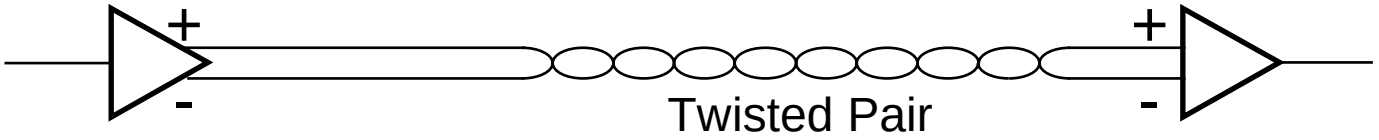
- output of a buffer switched
- output of a buffer holded at high and low

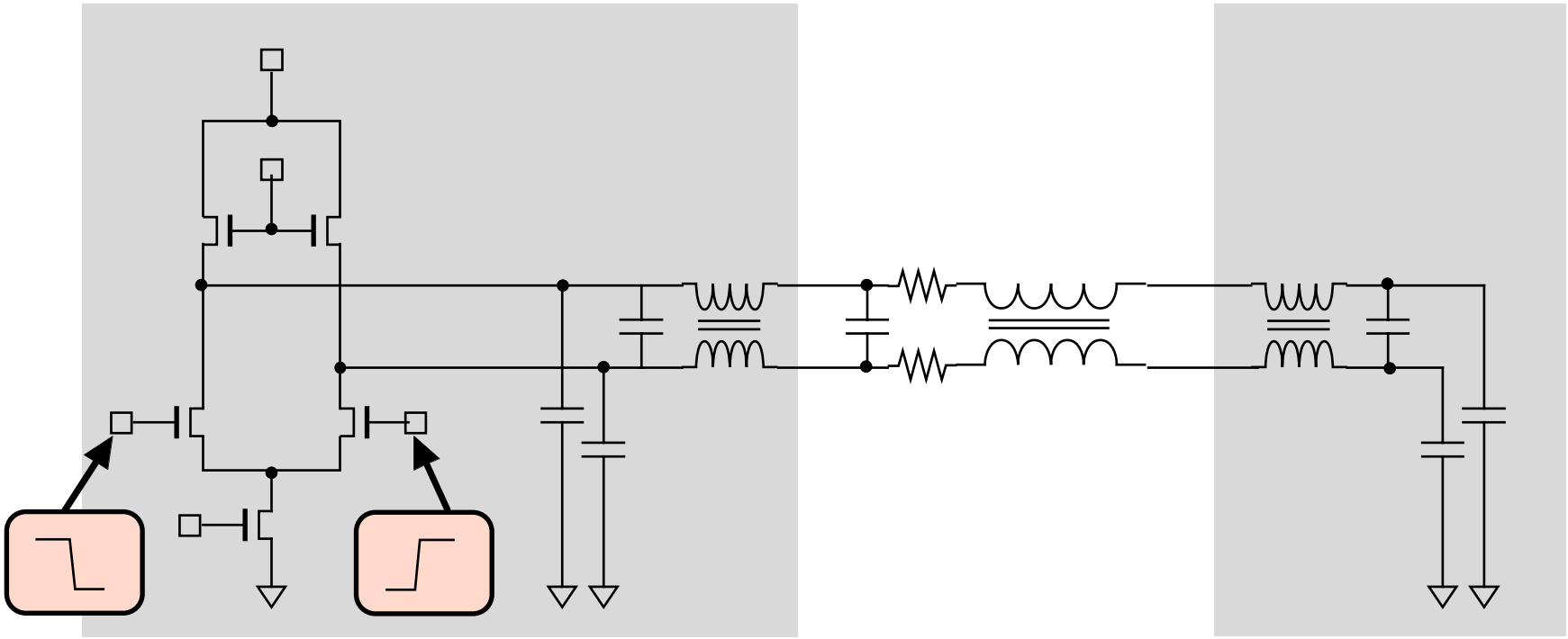
Data source: YAMAHA

Slew Rate Control Buffer



Differential Transmitter





Content

Future Work

1. Filing of application notes

- Signal integrity of complex buffers
  PCI buffers, Slew rate control buffers, LVDS, - - -
- Power/ground bounce
- Package electrical characterization
  Too detailed data bring long simulation time.

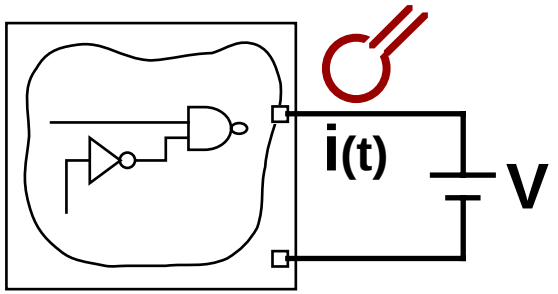
2. Challenge to new technologies

- Release of EMI model
- Characterization of new types of package
  BGA, CSP, - - -
- Modeling of DRAM module

EM Emission from Board

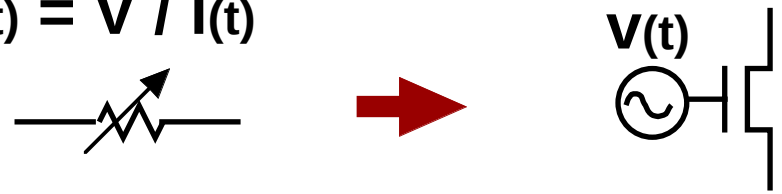
(1) Measure terminal current

- **Magnetic field prove method**
- **Simulation of whole circuits of IC**

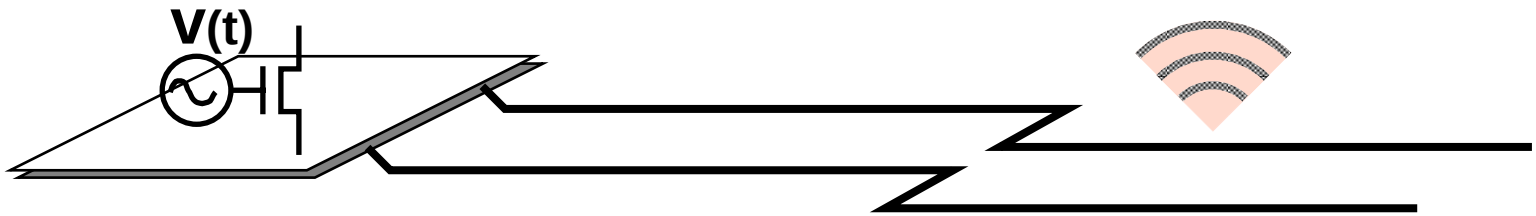


(2) Model terminal current

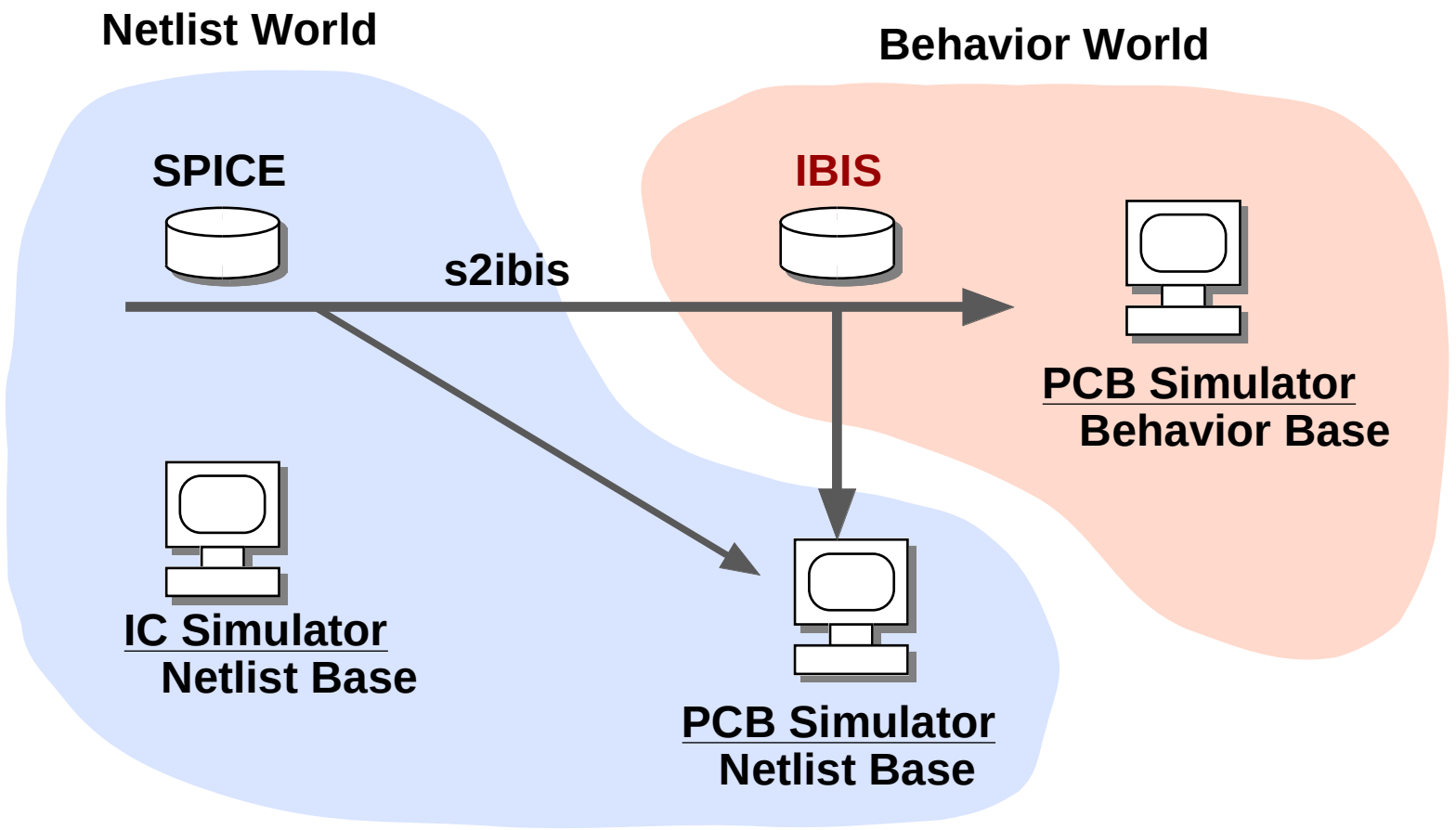
$$r_{(t)} = V / i_{(t)}$$



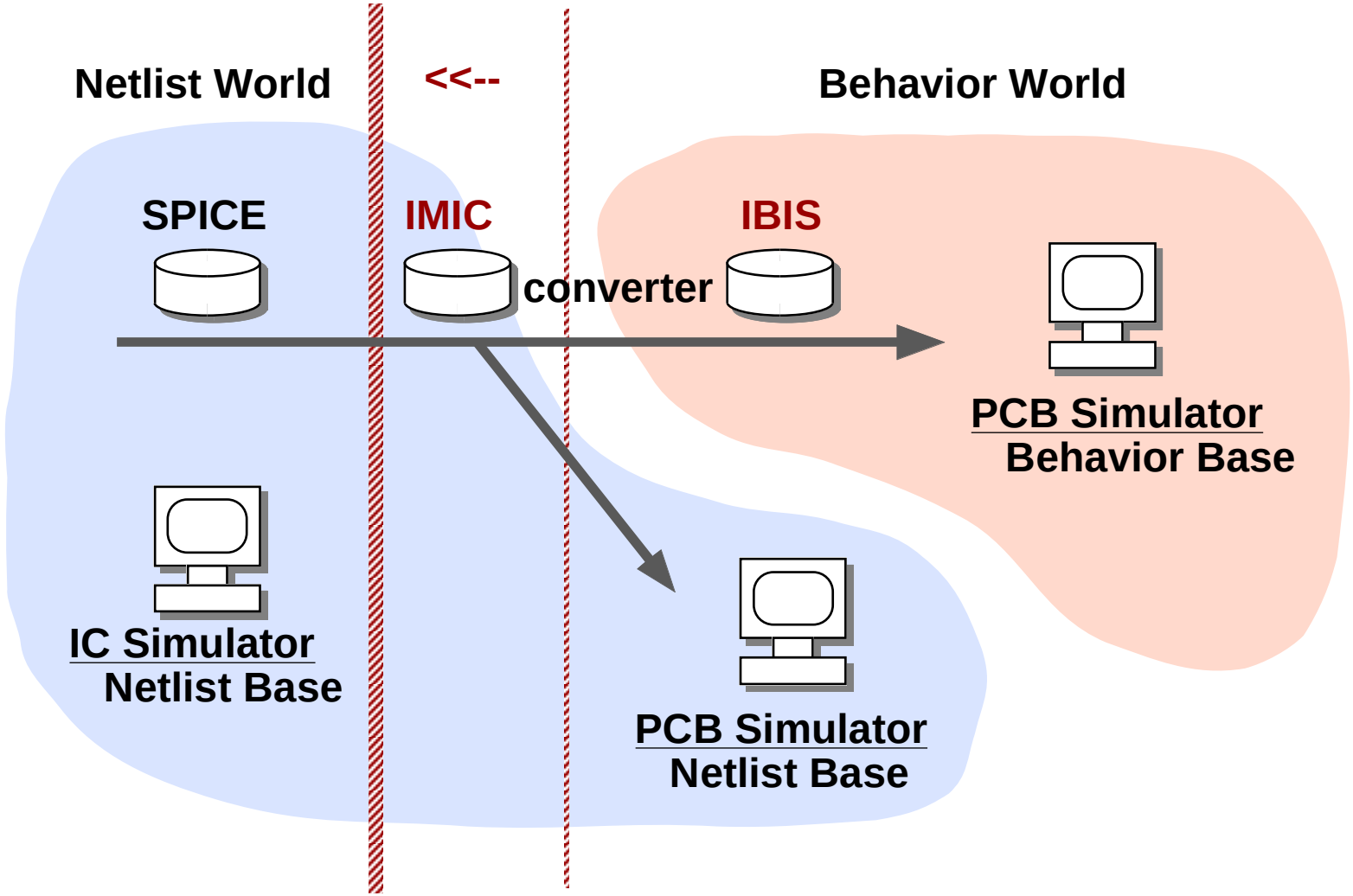
(3) Simulate EM emmision from board



Flow of I/O Data



Expansion of IBIS



Content

Benefits

Electronic equipment industry

- can get I/O data more easily without negotiation or NDA with IC companies.
- can analyze PCB at various levels, from only I/O data.

EDA industry

- can develop more advanced EDA using I/O data.
- can get more customers in the broader market.

IC industry

- can reduce inconvenience of supplying I/O data.
- can protect information of semiconductor process and circuits.

Conclusion

1. IMIC is an I/O interface model whose features are;
   - flexiblity in circuits description
   - protection of semiconductor process and circuits information
   - faster simulation than SPICE.

2. IMIC shows good accuracy in experiments

3. Joint work by IBIS and IMIC could improve silicon interface in PCB simulation