Improved C_comp Model Case Study

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Outline

Improving the C_comp model

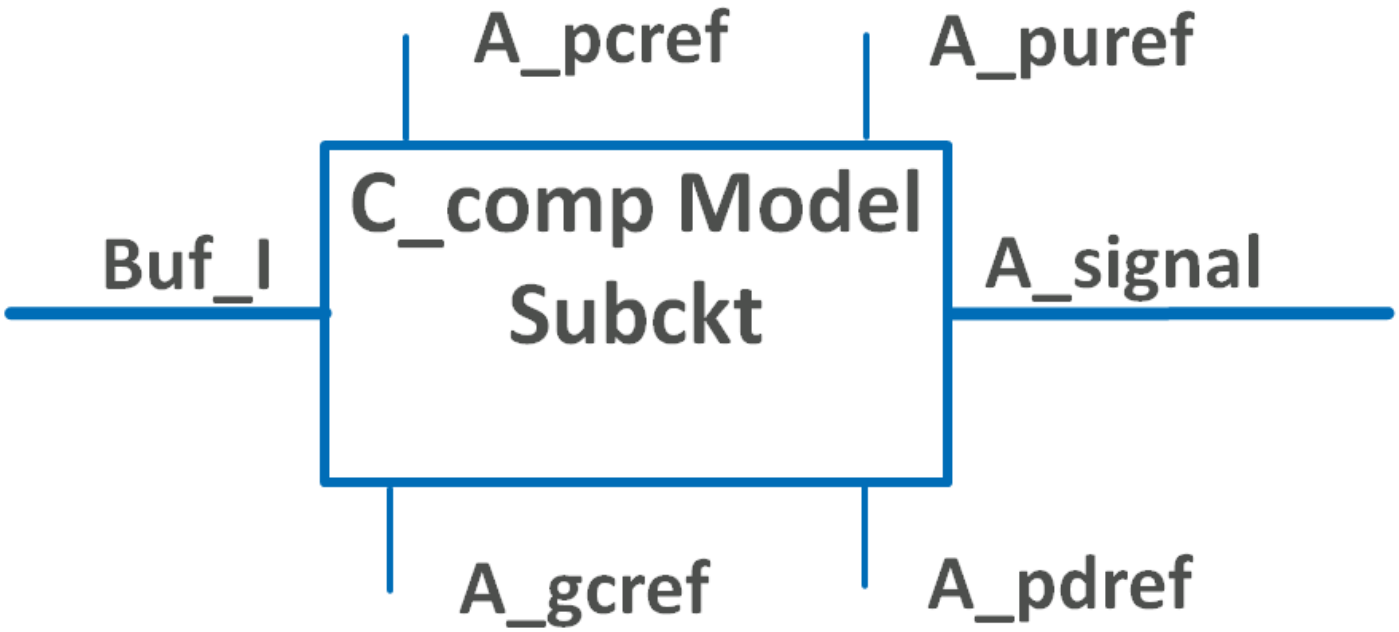
Case Study for a Lossy C_comp model

- Creating a Measurement Based Model
- Test Case Simulation with two C_comp Models

Conclusion

Improving the C_comp Model

IBIS-ISS based C_comp subcircuit model in development by the ATM and Interconnect task groups



Model could represent a frequency dependent C_comp behavior

Creating a Measurement Based C_comp model

8Gb DDR4 x8

- 25nm process
- 78-ball single layer FBGA

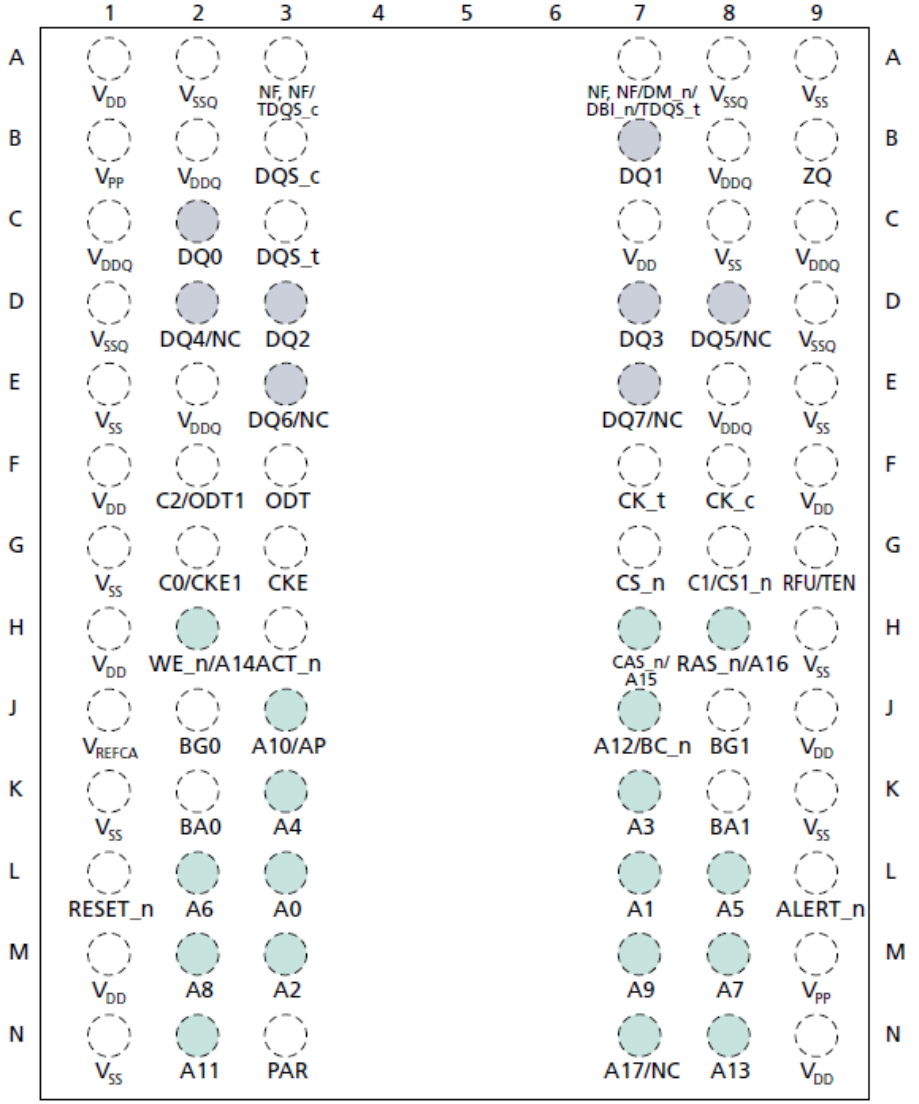
3-DUTs

- C_pkg (no die)
- L_pkg (shorted die)
- C_pkg, L_pkg, C_die (live die)

VNA Measurement:

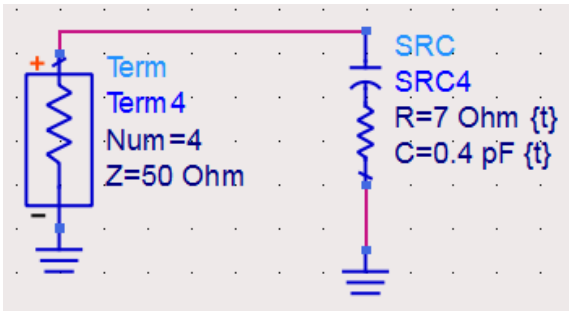
- S11
- 50MHz – 8.5GHz
- 5.28125MHz steps

Modeled several Address inputs

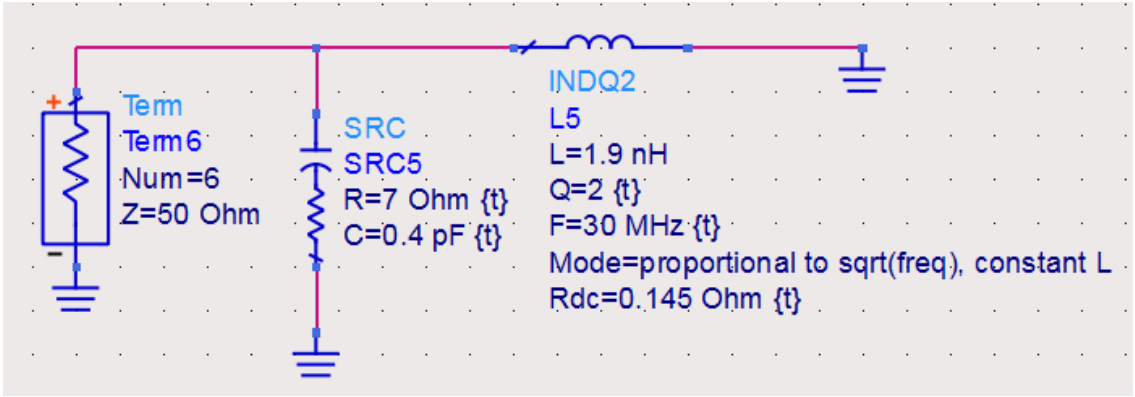


Model Schematics – Address Inputs

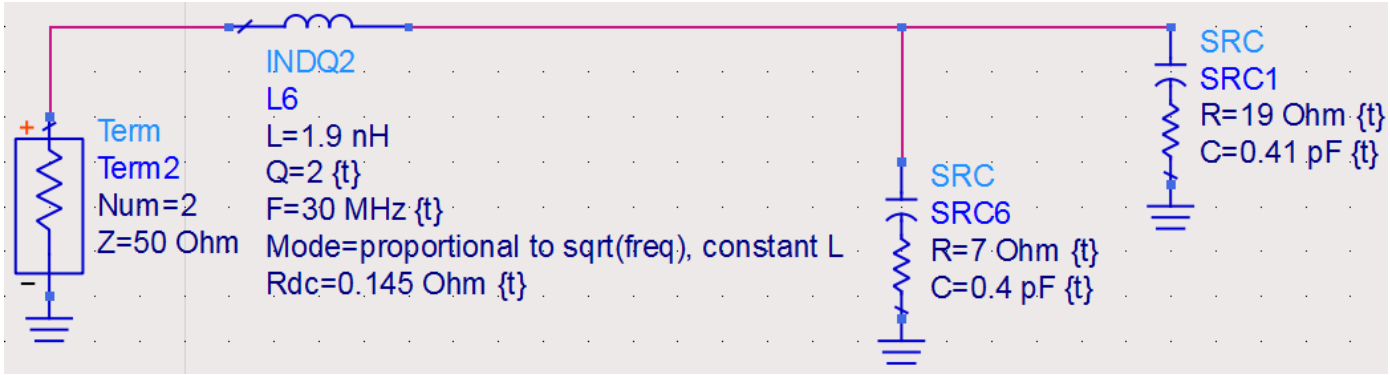
C_pkg (no die)



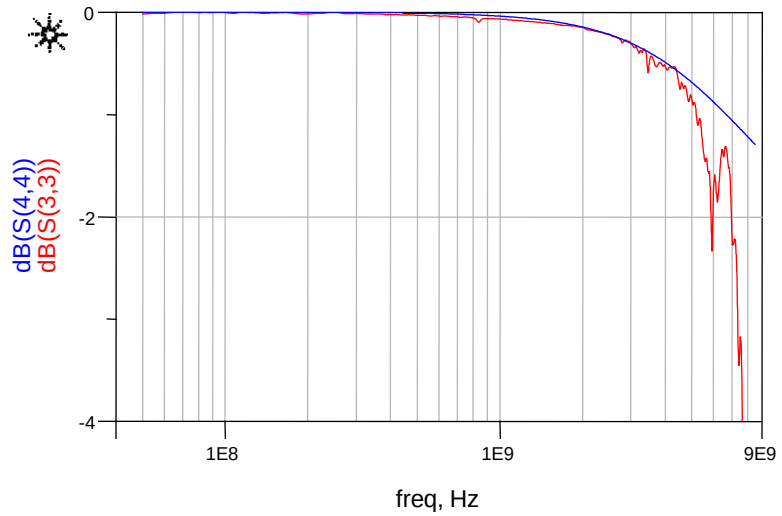
L_pkg (shorted die)

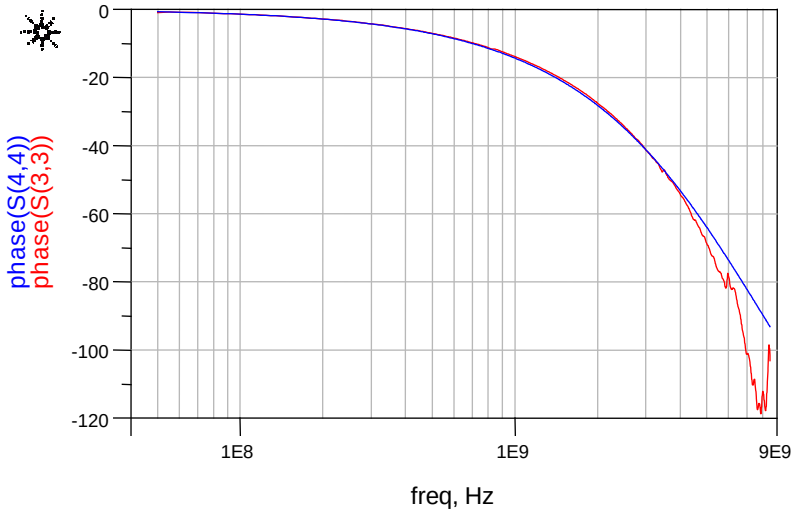


C_pkg, L_pkg, C_die (live die)



Step 1: C_pkg Simulation (S11, Mag/Phase)

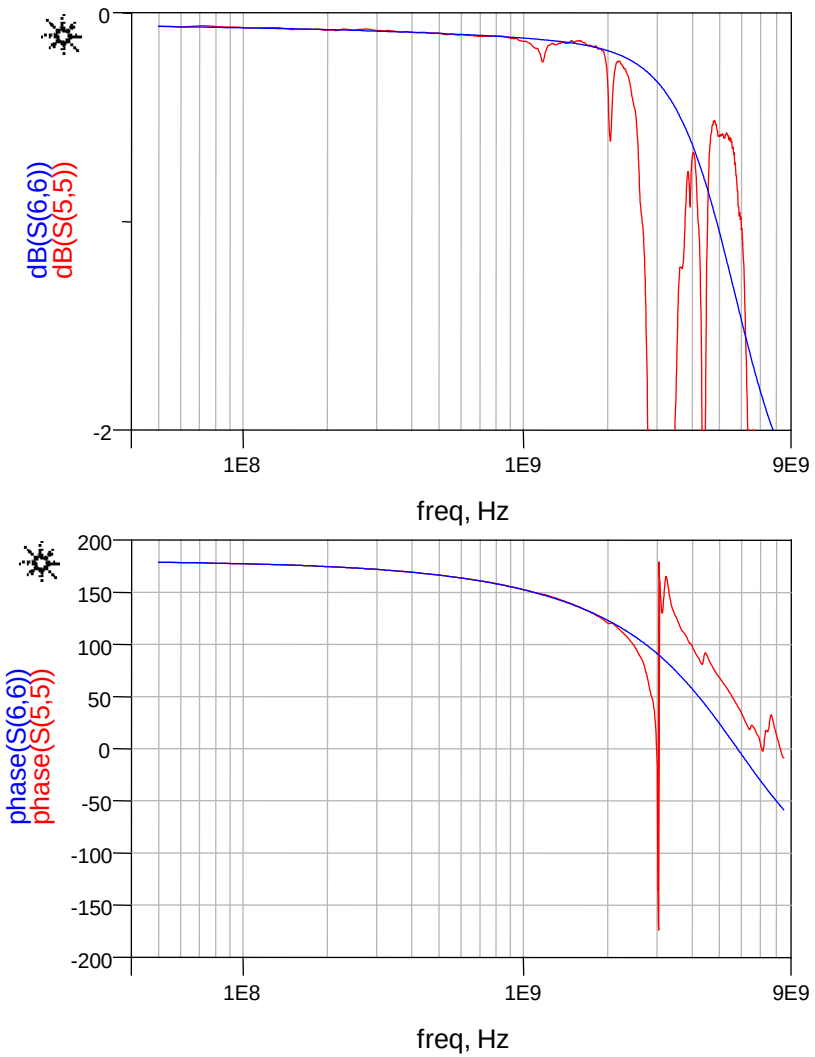




Model

Measurement

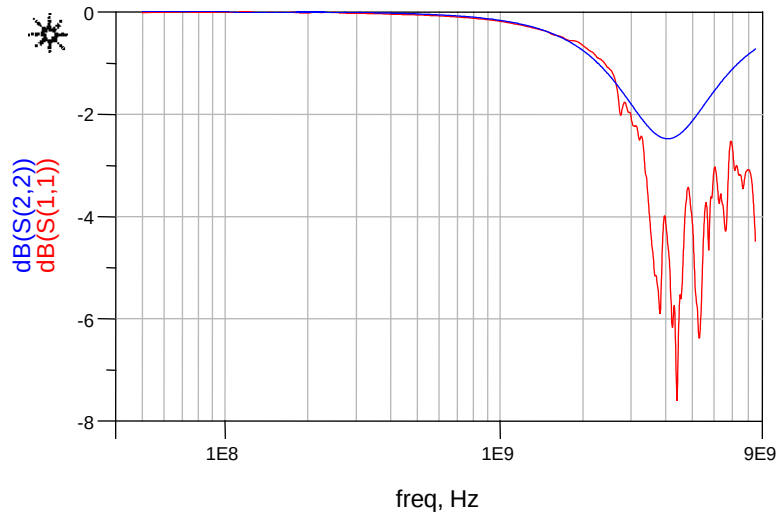
Step 2: L_pkg Simulation (S11, Mag/Phase)



Model

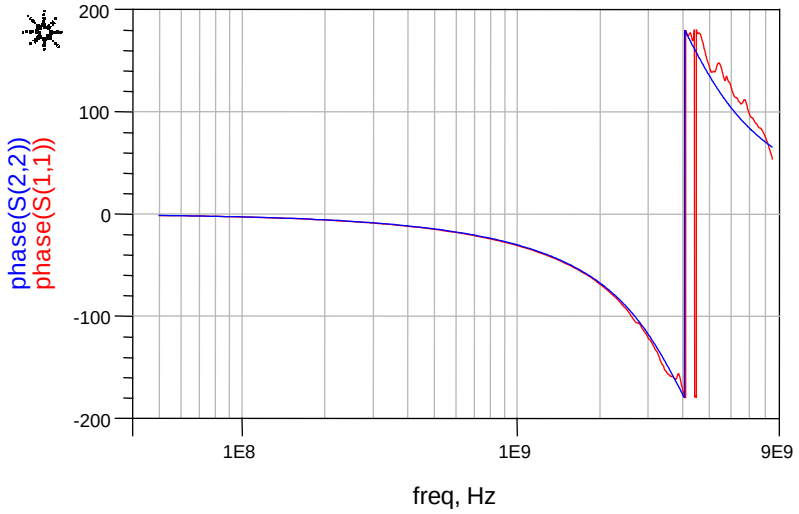
Measurement

Step 3: C_pkg, L_pkg, C_die Simulation (S11, Mag/Phase)



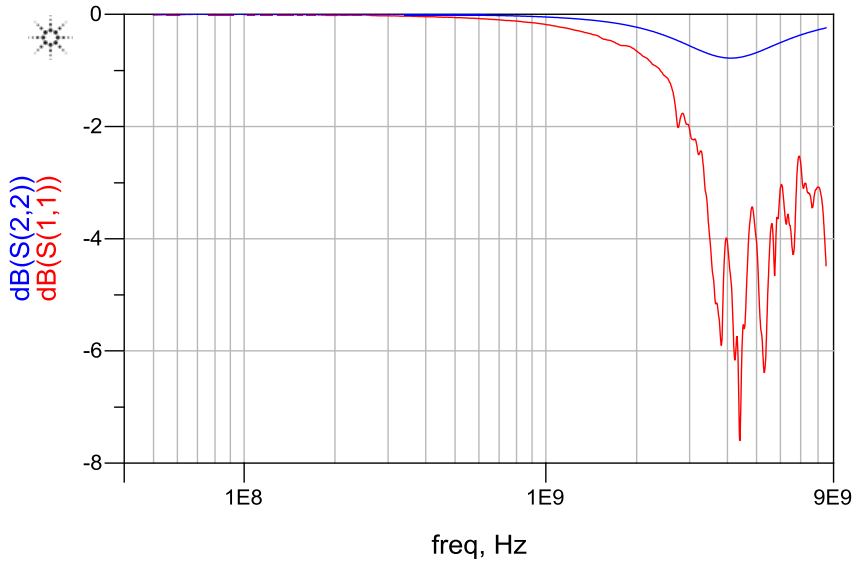
Model
Measurement

Result:
ESR of C_comp
is ~ 19 Ohms

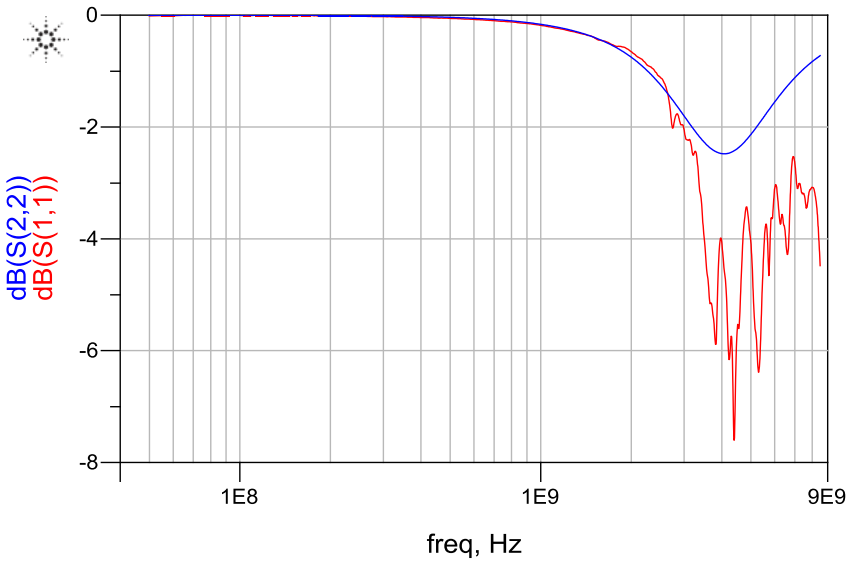


Step 3: C_pkg, L_pkg, C_die Simulation (S11, Mag)

ESR=0 Ohms (Original)



ESR=19 Ohms (Lossy)



Model

Measurement

Test Case Simulation

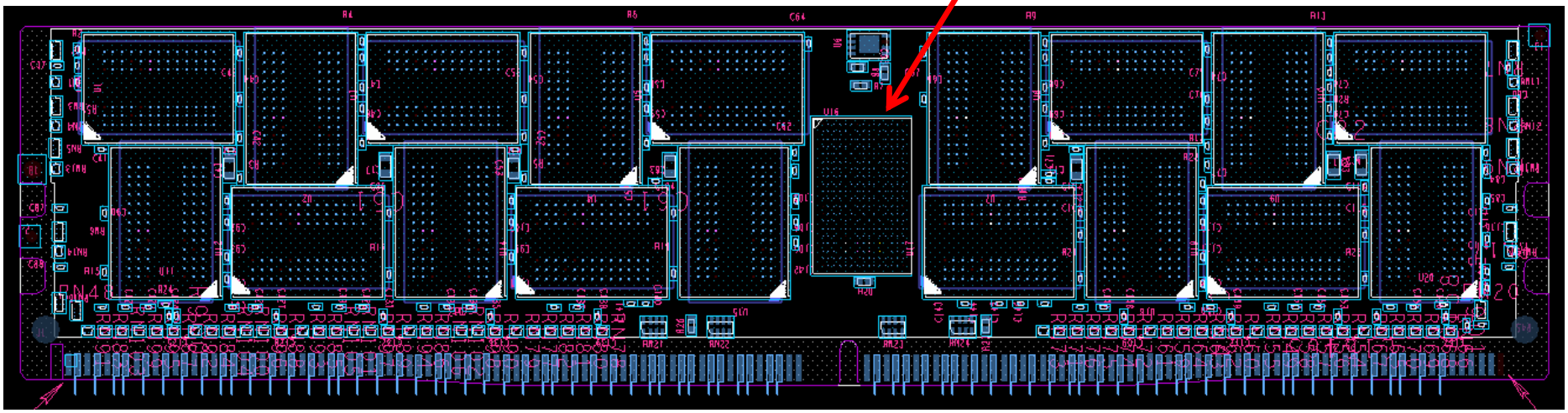
DDR4 LRDIMM

- Uses previously measured DDR4 SDRAM die
- Simulated post-register Address net
  - DDP devices (2 die in package)
  - 40 loads total
  - DDR4-2400, 1.2Gbps for Address
  - 255-bit PRBS stimulus
  - Light and Strong drive Register driver settings
- Compared simple C_comp model to lossy C_comp model

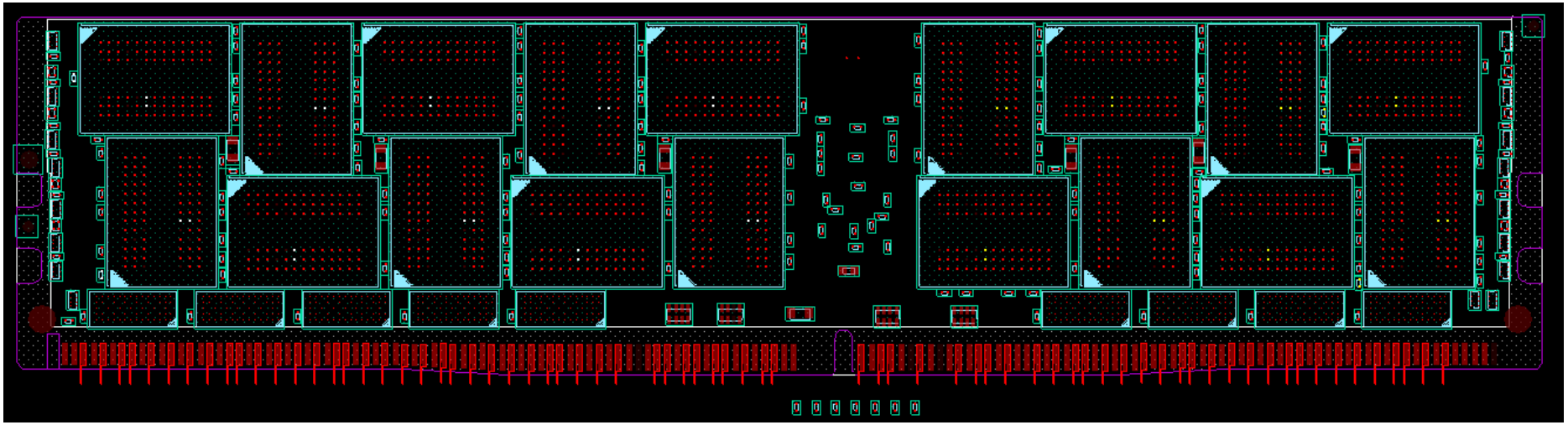
LRDIMM Layout

Front side

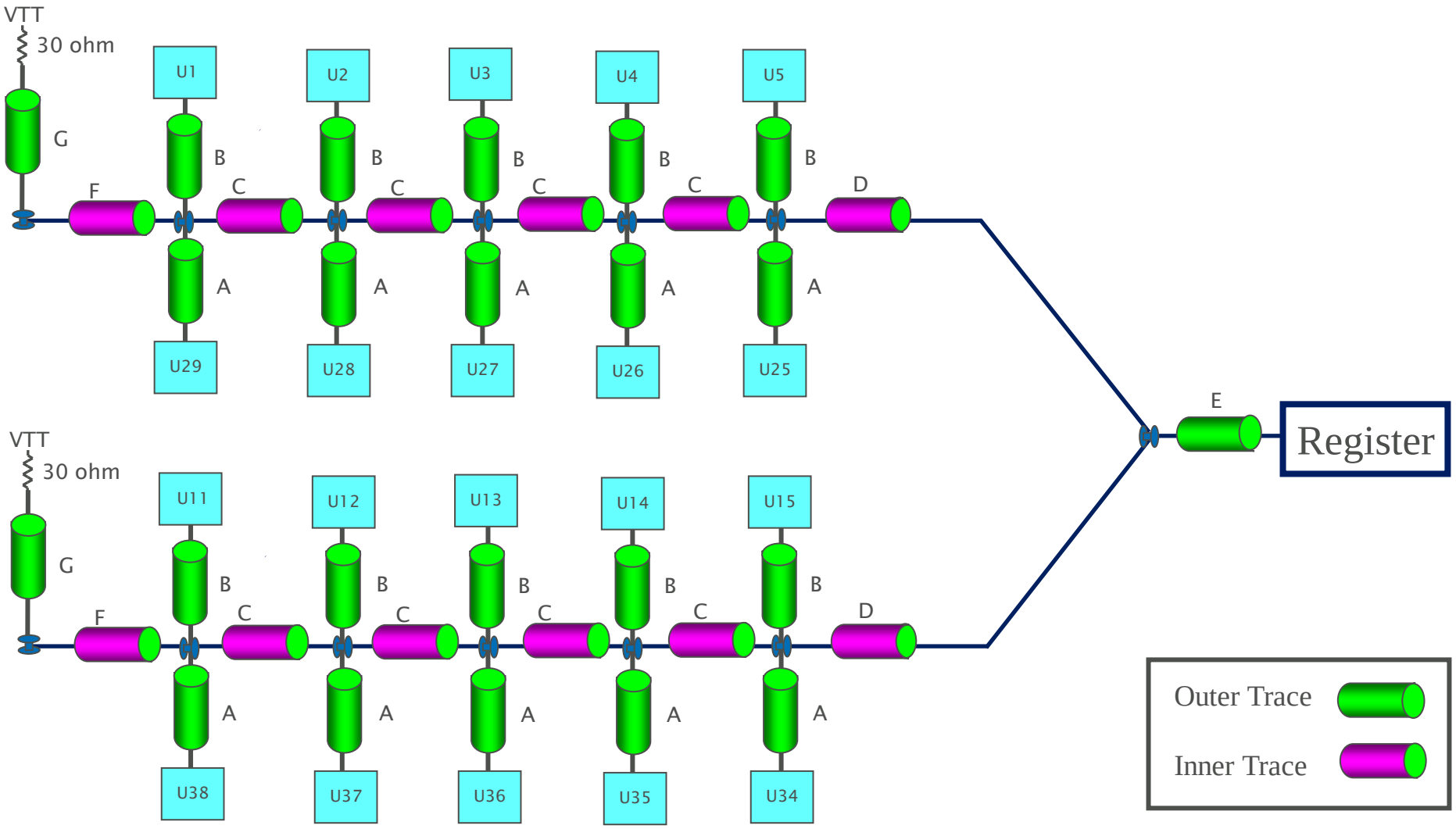
Register



Back side



Net A09A Topology, Flower pattern

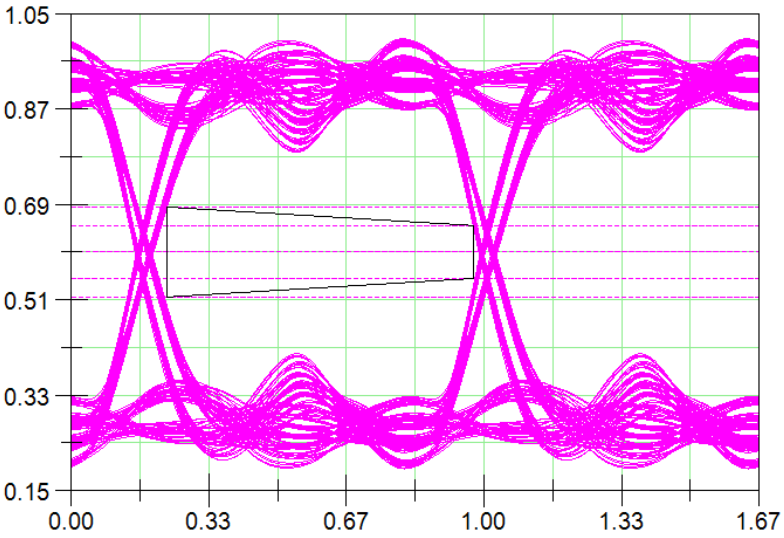


Non-Lossy C_comp, Strong Drive

U25

Jitter = 45ps AptACDC = 0.742ns VMarginDC = 139mV

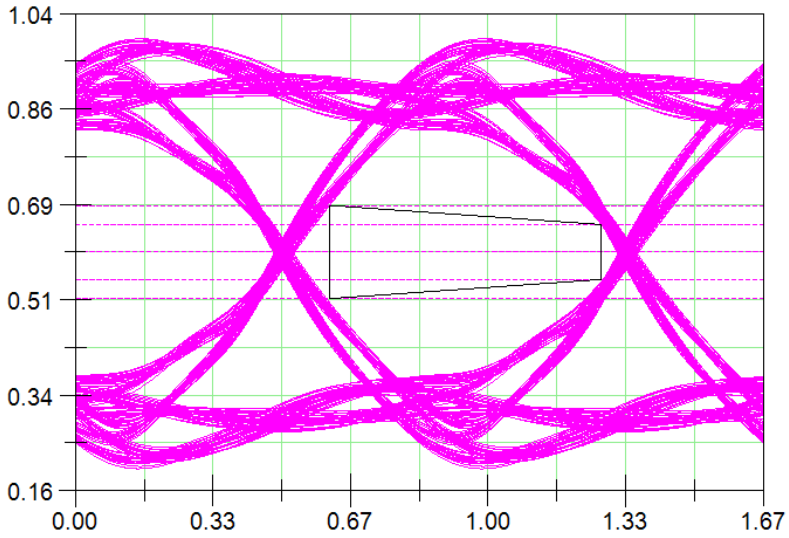
MinSlew = 2.58V/ns ArrTime = 0.177ns



U29

Jitter = 52ps AptACDC = 0.659ns VMarginDC = 173mV

MinSlew = 0.92V/ns ArrTime = 0.505ns



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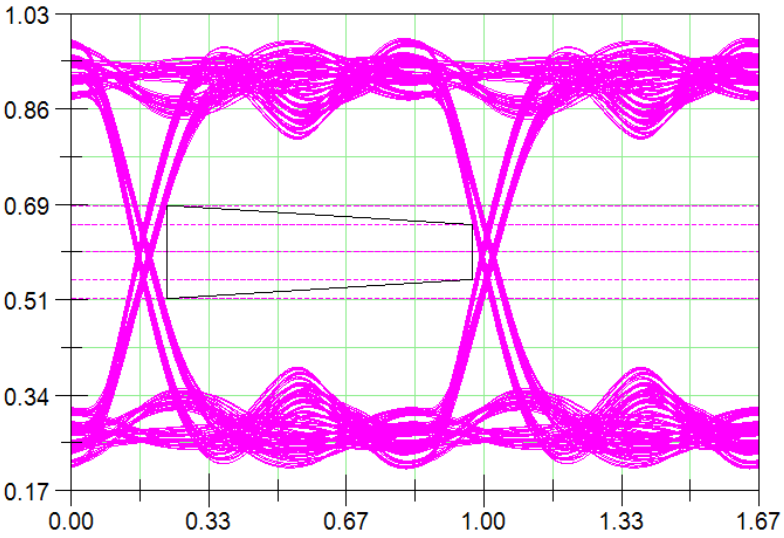
Lossy C_comp, Strong Drive

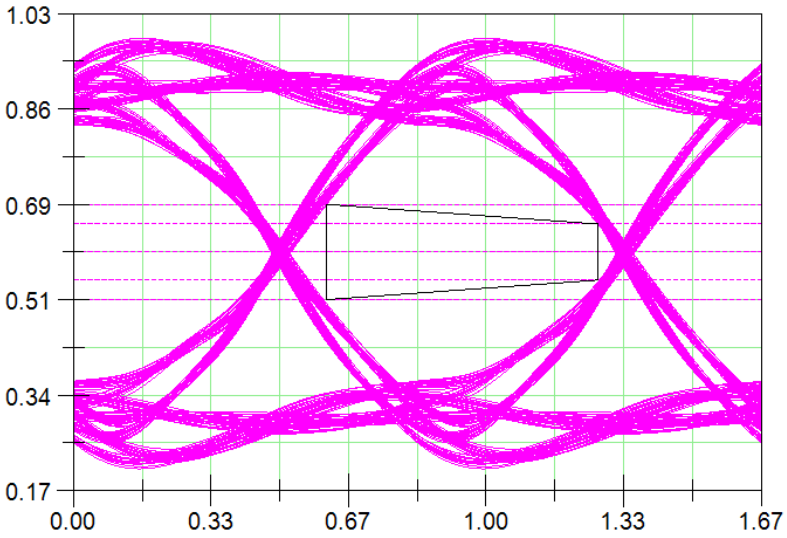
U25

Jitter = 45ps AptACDC = 0.742ns VMarginDC = 155mV
MinSlew = 2.54V/ns ArrTime = 0.177ns

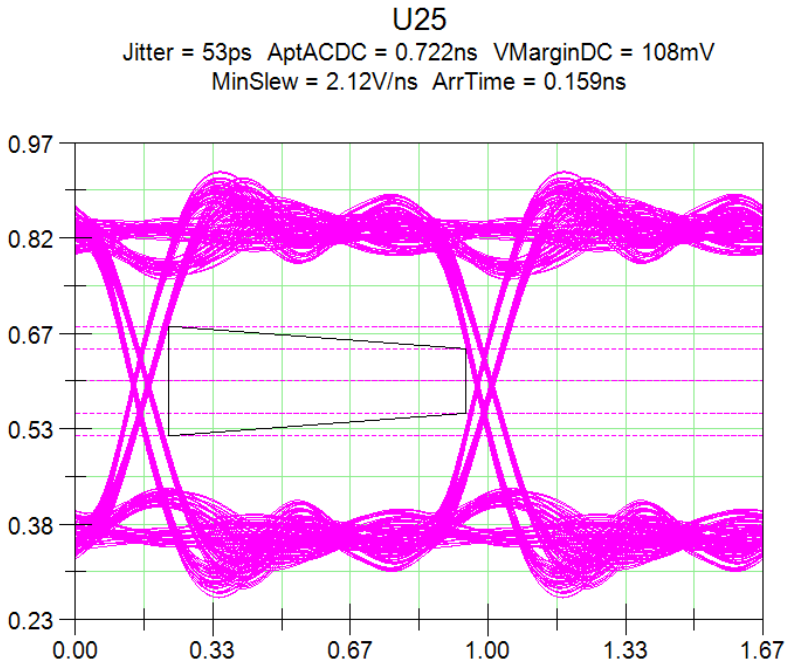


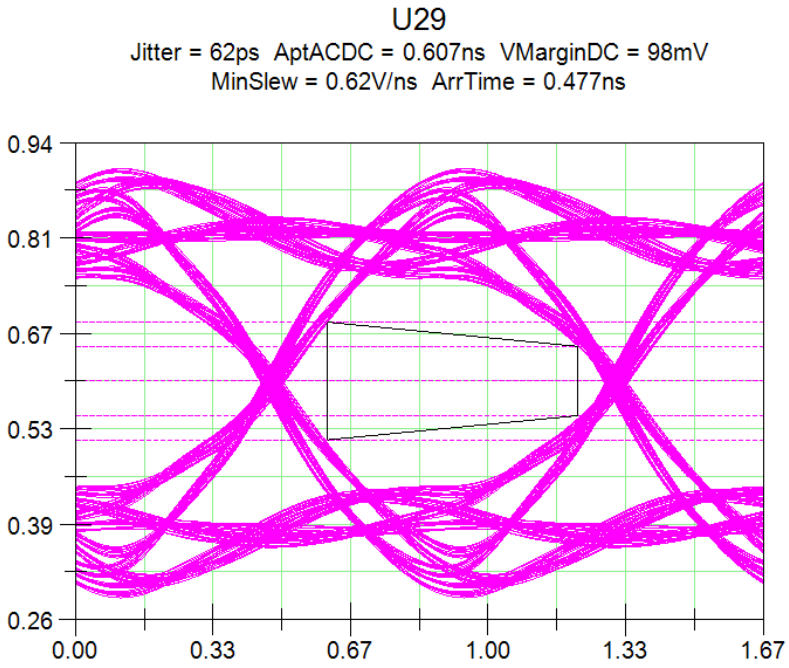
U29

Jitter = 48ps AptACDC = 0.657ns VMarginDC = 182mV
MinSlew = 0.90V/ns ArrTime = 0.503ns

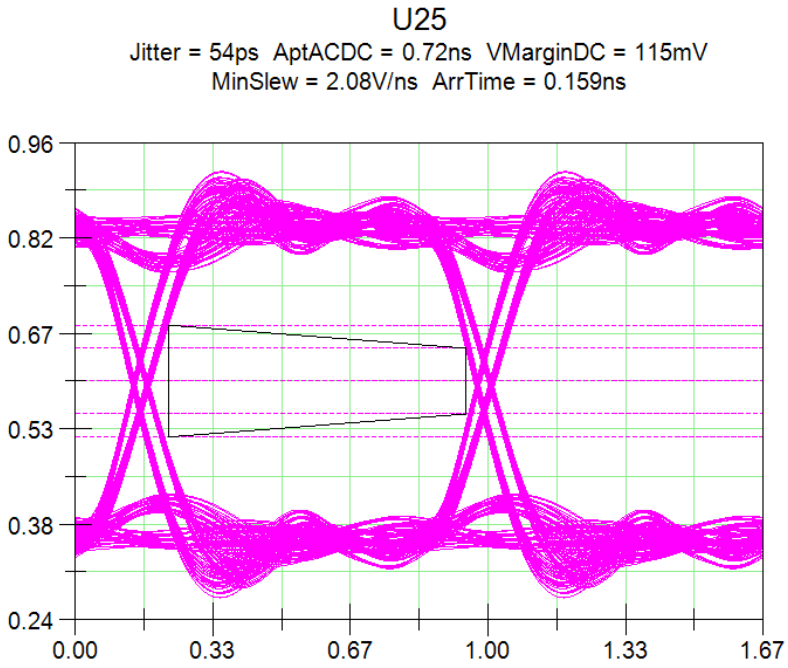


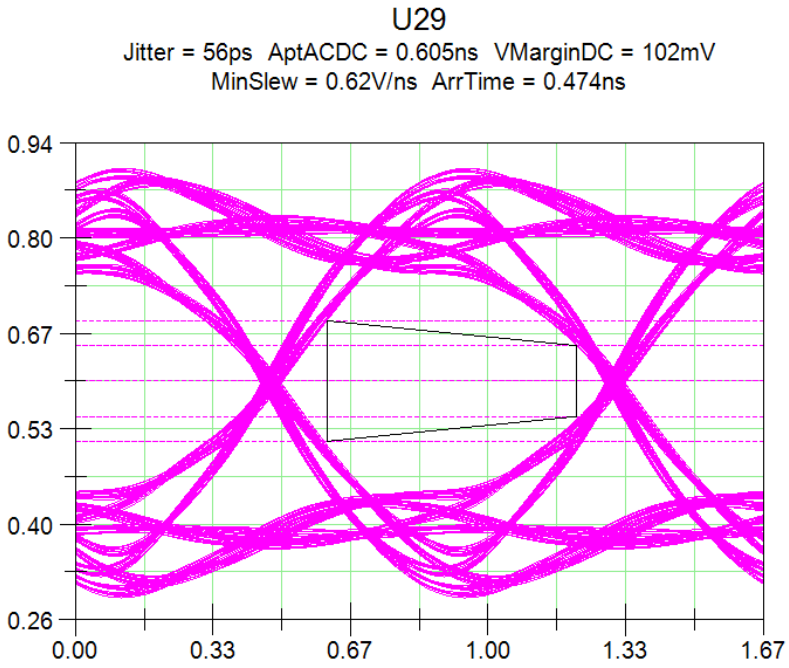
Non-Lossy C_comp, Light drive





Lossy C_comp, Light drive





Conclusions

Driver Setting	C_comp Model	Vmargin DC - U25	Vmargin DC – U29
Strong Drive	Non-lossy (original)	139mV	173mV
Strong Drive	Lossy (with ESR)	155mV	182mV
Light Drive	Non-lossy (original)	108mV	98mV
Light Drive	Lossy (with ESR)	115mV	102mV

Including ESR improves voltage margin by 16mV , 11.5% (best case)

ESR filters high frequency content at the die, which can improve SI

Improving the C_comp model is needed for improving the accuracy and usefulness of IBIS models.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