# Improved C\_comp Model Case Study

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# Outline

#### Improving the C\_comp model

Case Study for a Lossy C\_comp model

- Creating a Measurement Based Model
- Test Case Simulation with two C\_comp Models

#### Conclusion



### Improving the C\_comp Model

IBIS-ISS based C\_comp subcircuit model in development by the ATM and Interconnect task groups



Model could represent a frequency dependent C\_comp behavior



# Creating a Measurement Based C\_comp model

#### 8Gb DDR4 x8

- 25nm process
- 78-ball single layer FBGA

#### 3-DUTs

- C\_pkg (no die)
- L\_pkg (shorted die)
- C\_pkg, L\_pkg, C\_die (live die)

#### **VNA Measurement:**

- S11
- 50MHz 8.5GHz
- 5.28125MHz steps

#### Modeled several Address inputs

	1	2	3	4	5	6	7	8	9	
Α	$\bigcirc$	$\bigcirc$						()	(	Α
В		<b>v</b> <sub>ssq</sub>	TDQS_c				DBI_n/TDQS	t Vssq	()	в
c			DQS_C						ŽQ ()	c
D			DQS_t					V <sub>SS</sub>		D
E								()	V <sub>SSQ</sub>	E
F	$\bigvee_{SS}$								() V	F
G							$\bigcirc$	$\bigcirc$		G
н	())									н
J		() ()					A12/PC		$\bigcirc$	J
к		$\bigcirc$							$\bigcirc$	к
L	()		A4						())	L
м										м
N	V <sub>DD</sub> () V <sub>SS</sub>	A8	AZ () PAR				A9	A/		N



### **Model Schematics – Address Inputs**



#### C\_pkg, L\_pkg, C\_die (live die)

+ Ter Ter Nul Z=t	m m2 m=2 50 Ohm	INDQ2 L6 L=1.9 nH Q=2 {t} F=30 MHz {t} Mode=proportional to sqrt(freq), constant L Rdc=0.145 Ohm {t}	SRC SRC6 R=7 Ohm {t} C=0.4 pF {t}	SRC SRC1 R=19 Ohm {t} C=0.41 pF {t}
. = .			=	 



### Step 1: C\_pkg Simulation (S11, Mag/Phase)





freq, Hz



# Step 2: L\_pkg Simulation (S11, Mag/Phase)



#### Model Measurement

freq, Hz



### Step 3: C\_pkg, L\_pkg, C\_die Simulation (S11, Mag/Phase)





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**Result:** ESR of C\_comp is ~ 19 Ohms

### Step 3: C\_pkg, L\_pkg, C\_die Simulation (S11, Mag)

#### ESR=0 Ohms (Original)

#### ESR=19 Ohms (Lossy)



Model Measurement



### **Test Case Simulation**

#### DDR4 LRDIMM

- Uses previously measured DDR4 SDRAM die
- Simulated post-register Address net
  - DDP devices (2 die in package)
  - 40 loads total
  - DDR4-2400, 1.2Gbps for Address
  - 255-bit PRBS stimulus
  - Light and Strong drive Register driver settings
- Compared simple C\_comp model to lossy C\_comp model



## **LRDIMM Layout**



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### Net A09A Topology, Flower pattern





### Non-Lossy C\_comp, Strong Drive



U29 Jitter = 52ps AptACDC = 0.659ns VMarginDC = 173mV MinSlew = 0.92V/ns ArrTime = 0.505ns





### Lossy C\_comp, Strong Drive



U29 Jitter = 48ps AptACDC = 0.657ns VMarginDC = 182mV MinSlew = 0.90V/ns ArrTime = 0.503ns





### Non-Lossy C\_comp, Light drive



U29 Jitter = 62ps AptACDC = 0.607ns VMarginDC = 98mV MinSlew = 0.62V/ns ArrTime = 0.477ns





# Lossy C\_comp, Light drive







1.67

1.33

### Conclusions

Driver Setting	C_comp Model	Vmargin DC - U25	Vmargin DC – U29
Strong Drive	Non-lossy (original)	139mV	173mV
Strong Drive	Lossy (with ESR)	155mV	182mV
Light Drive	Non-lossy (original)	108mV	98mV
Light Drive	Lossy (with ESR)	115mV	102mV

Including ESR improves voltage margin by 16mV , 11.5% (best case) ESR filters high frequency content at the die, which can improve SI

Improving the C\_comp model is needed for improving the accuracy and usefulness of IBIS models.



