LSI Power and Ground Model for EMI Simulation

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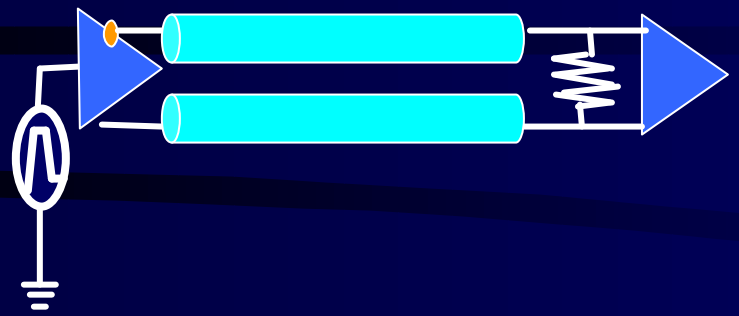
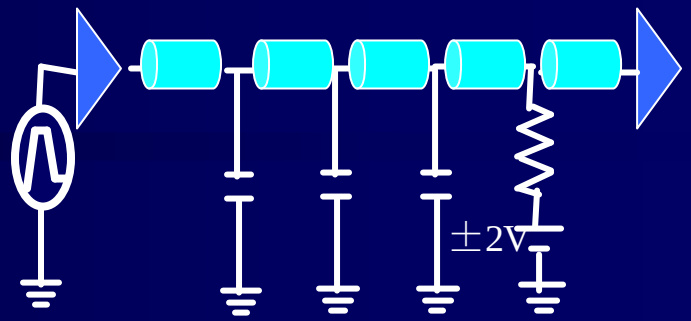
Outlines

1. Introduction
2. LSI Power and Ground Modeling
3. Accuracy

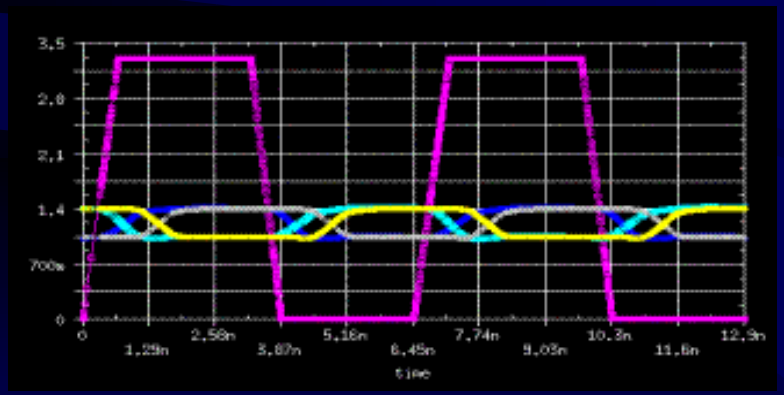
1. Introduction

IBIS works well for LVDS & (P)ECL

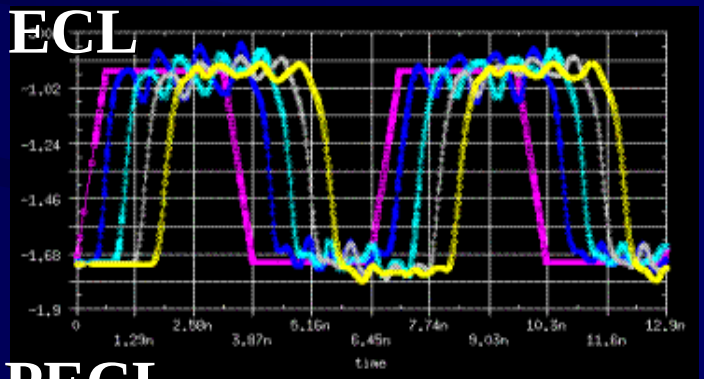




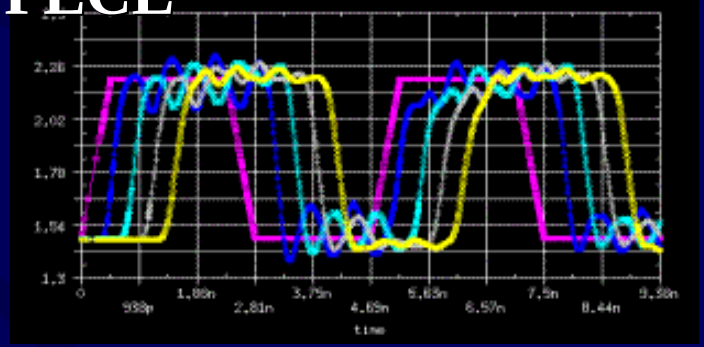
LVDS



ECL

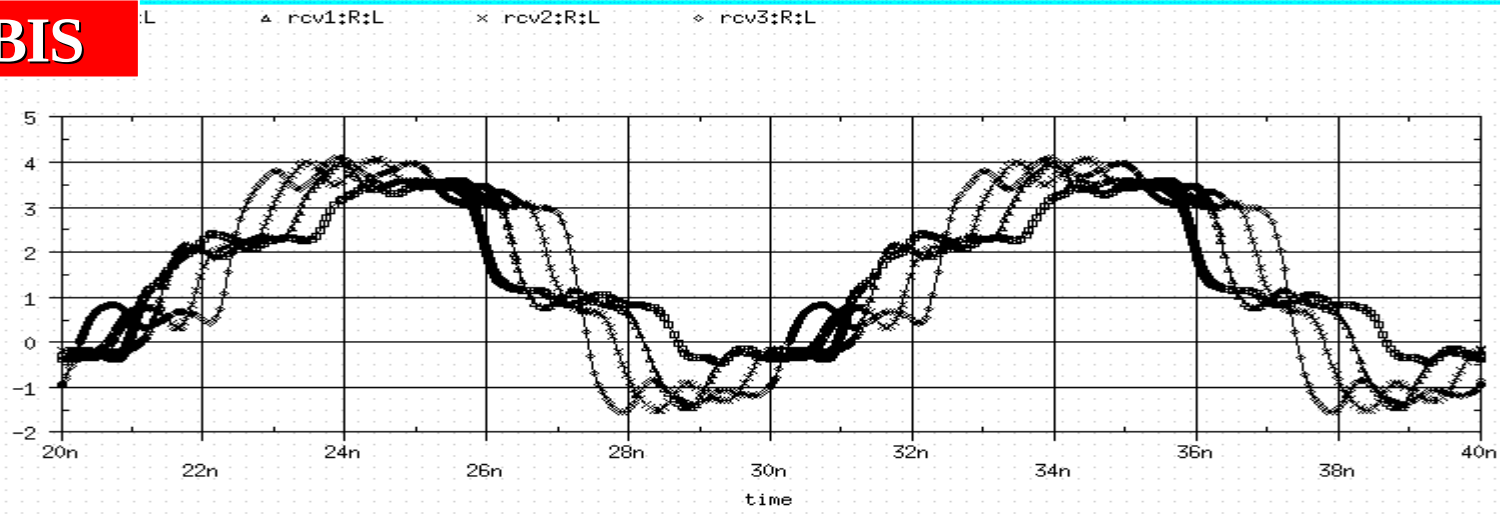


PECL

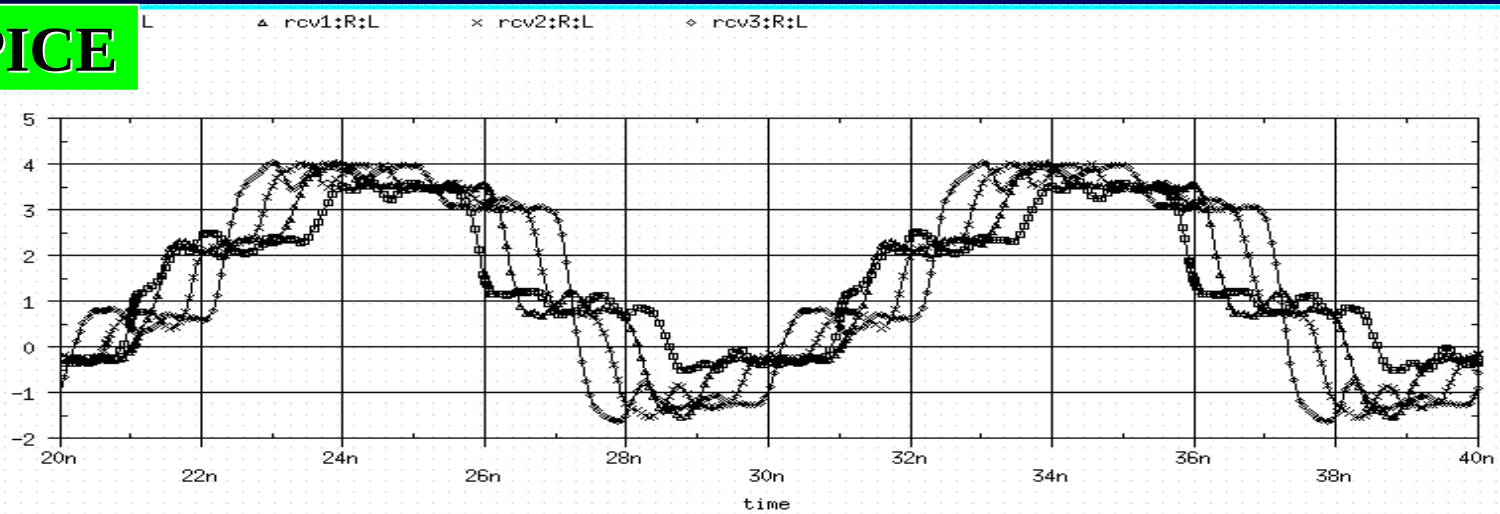


IBIS vs SPICE for Inverter (Voltage Waveforms)

IBIS

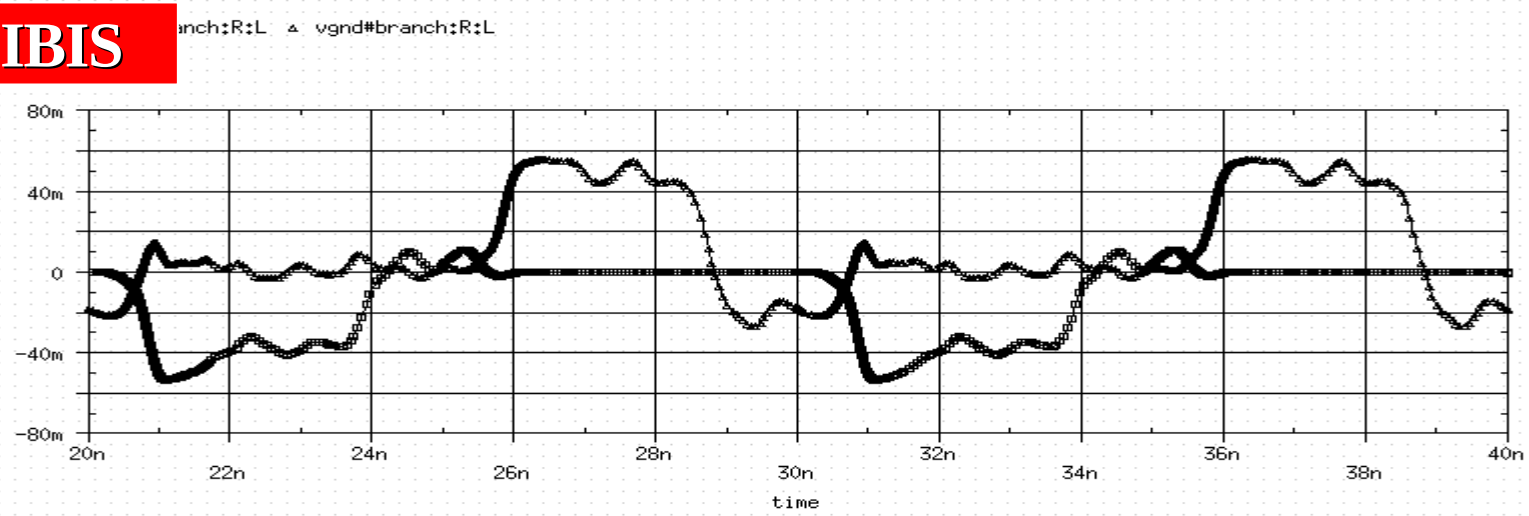


SPICE

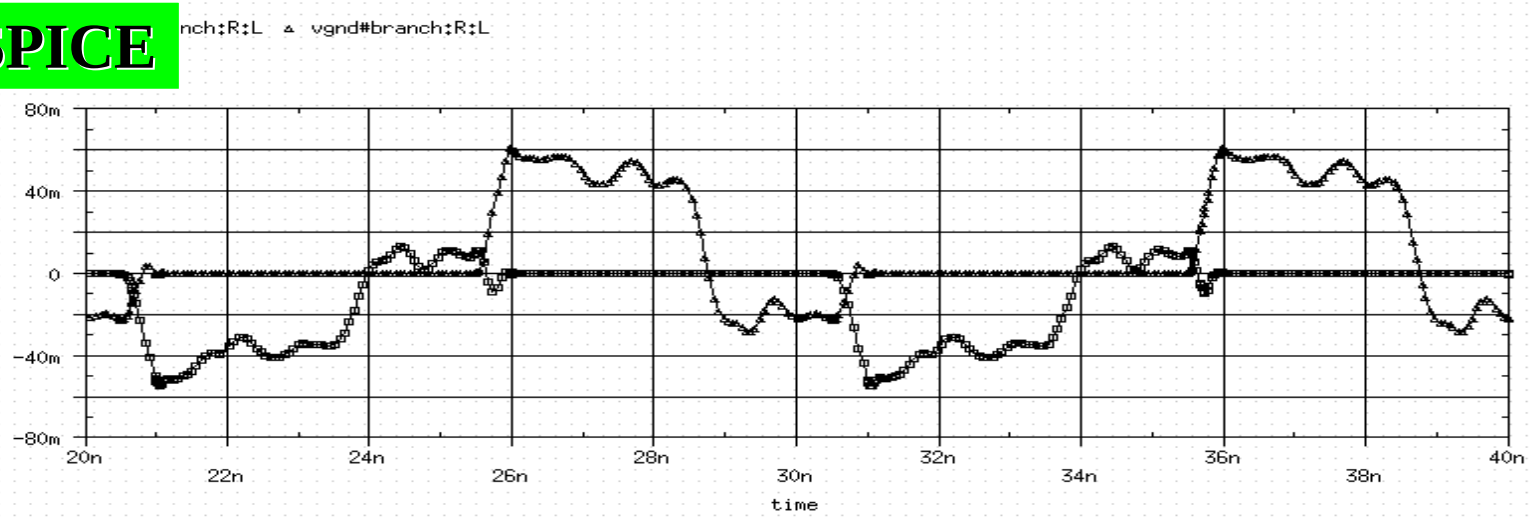


IBISvs SPICE for Inverter (Current Waveforms)

IBIS

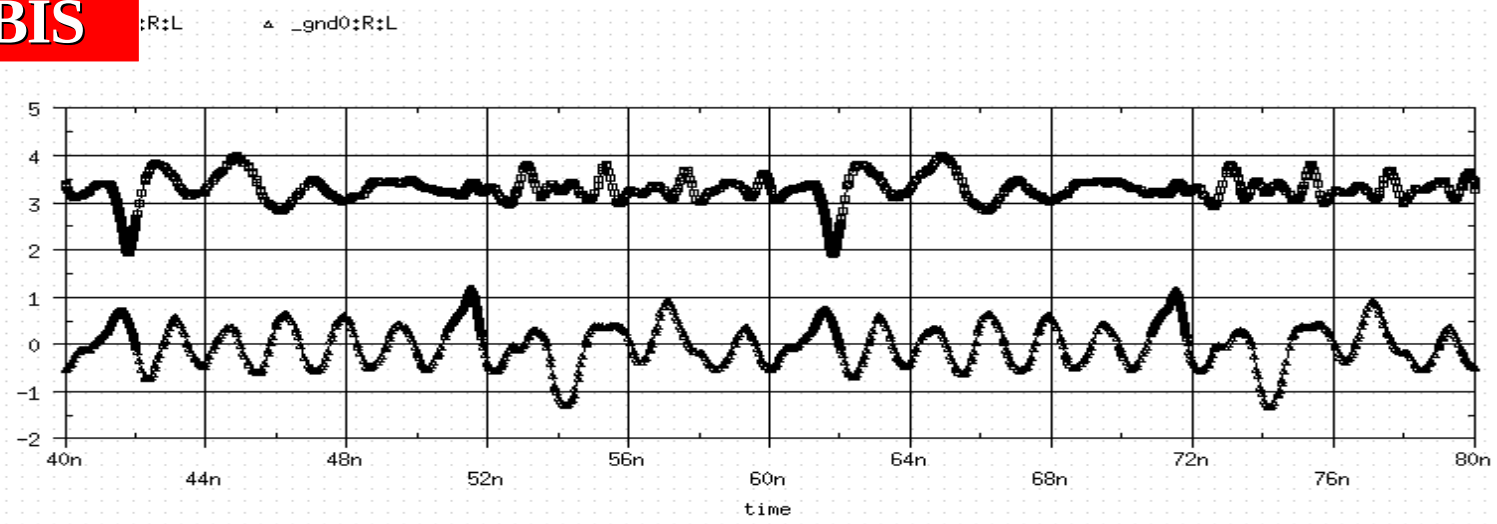


SPICE

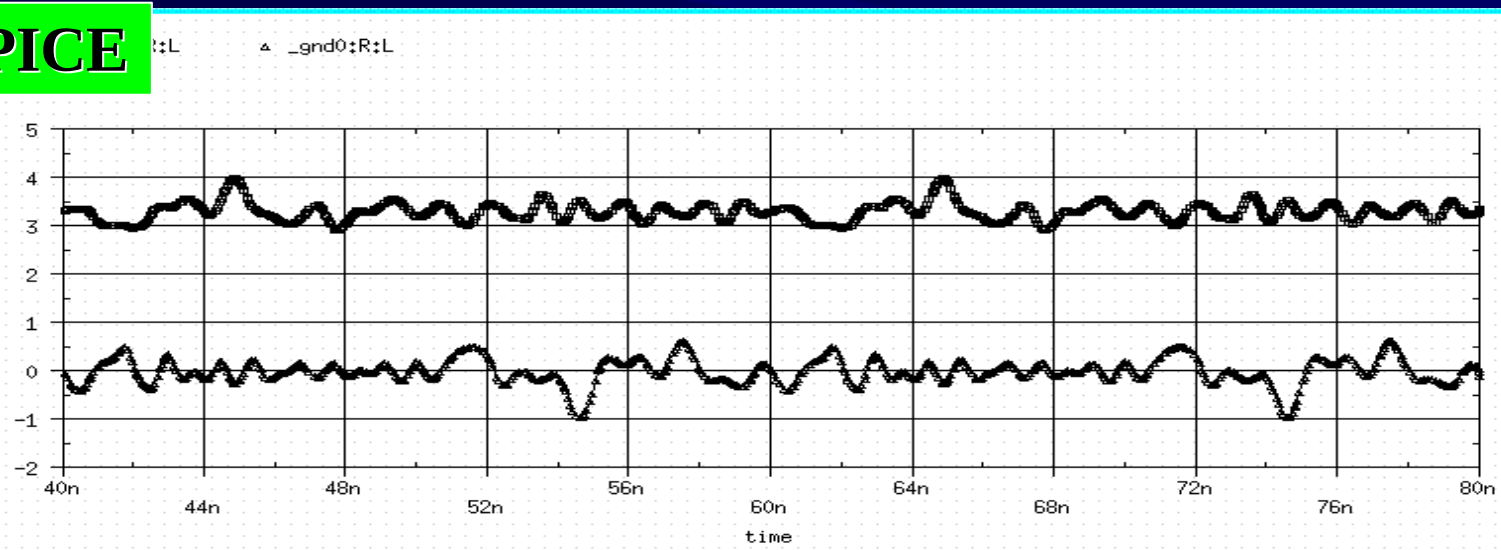


IBIS vs SPICE for SSO for Inverter

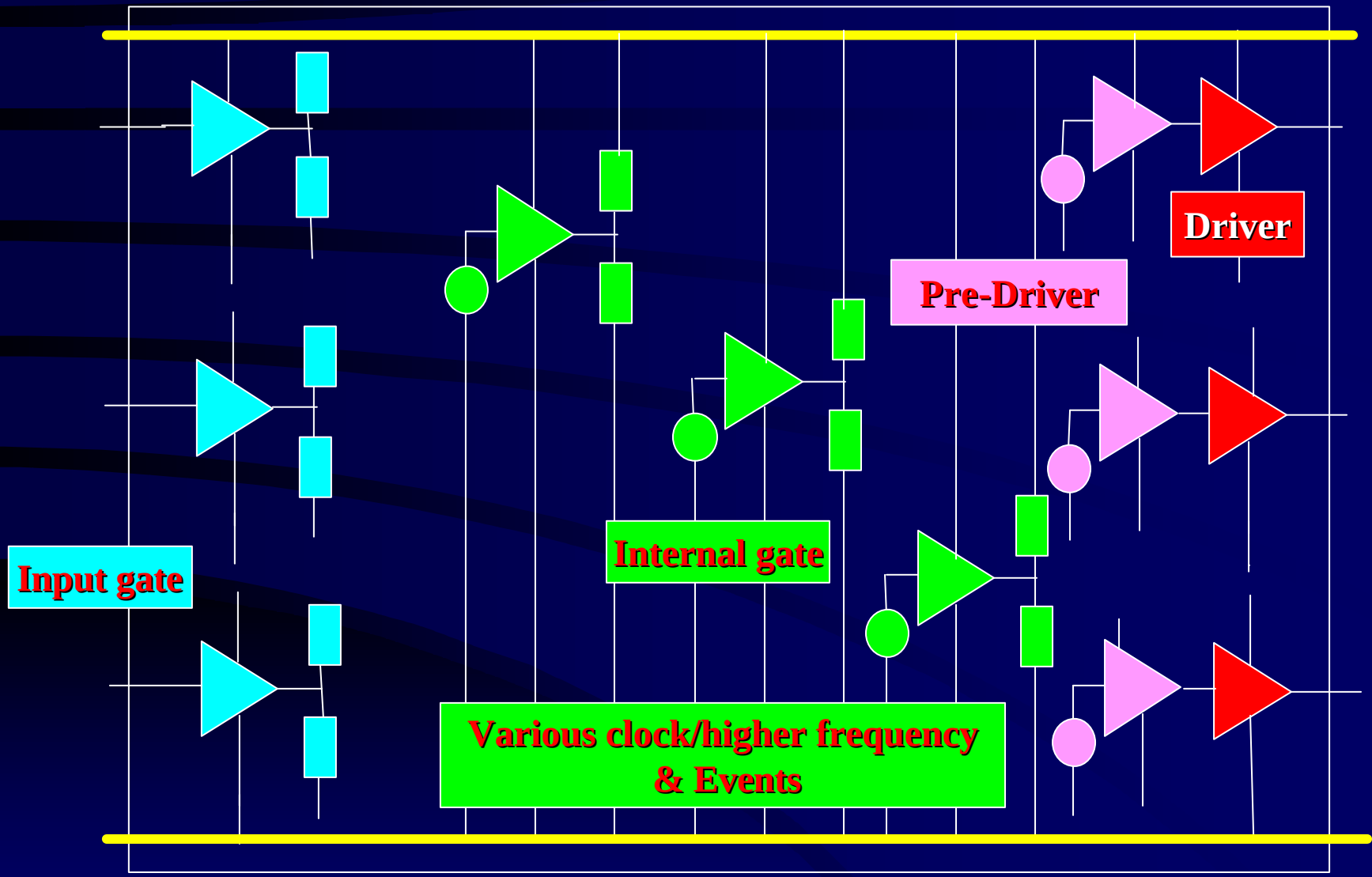
IBIS



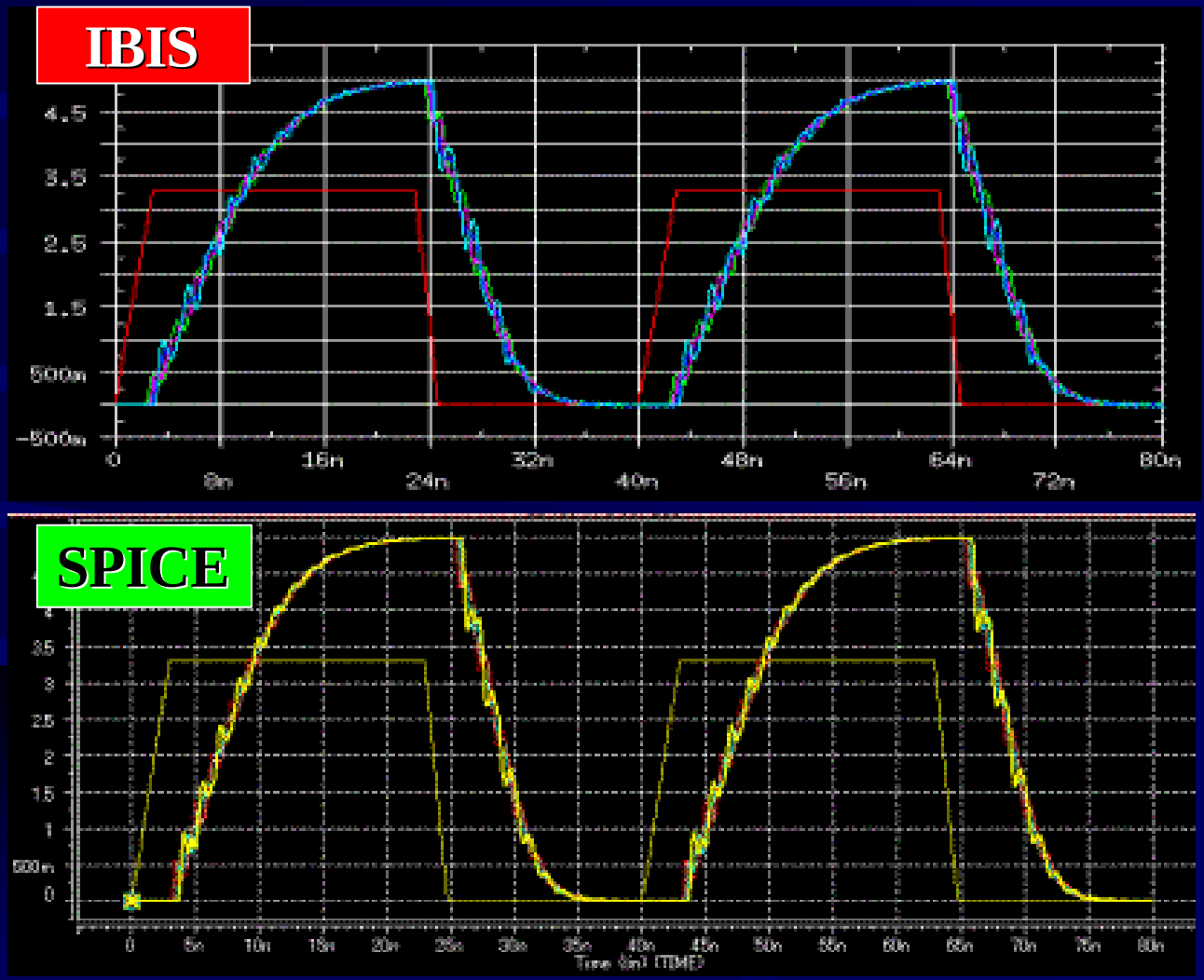
SPICE



IBIS for Real Complex IC and Power/Ground

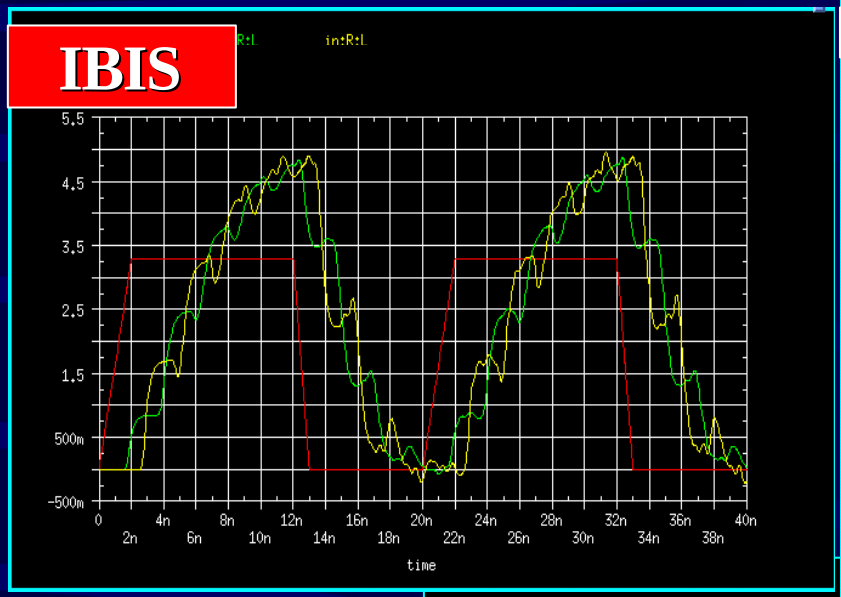


IBIS vs SPICE
for Output of System LSI with 100 Translators

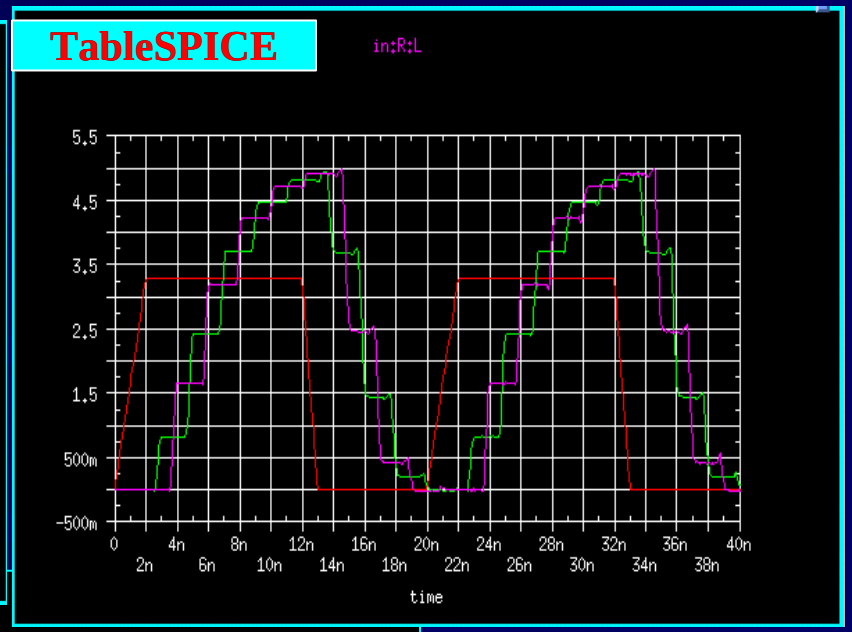


IBIS vs SPICE
for Output of System LSI for Transmission Lines

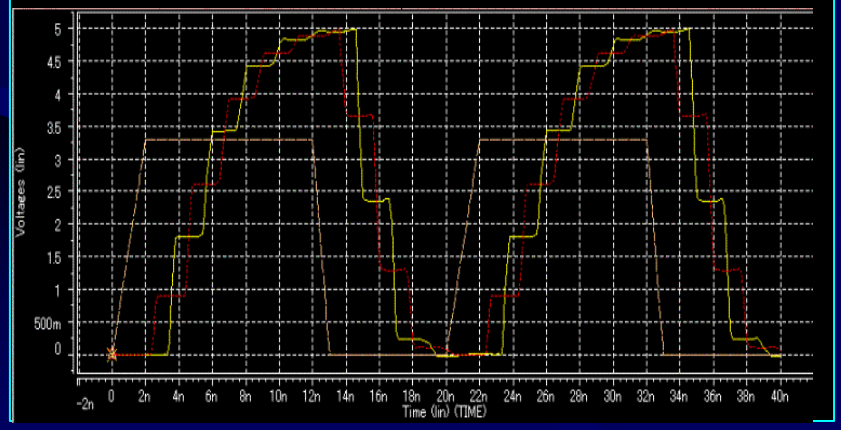
IBIS



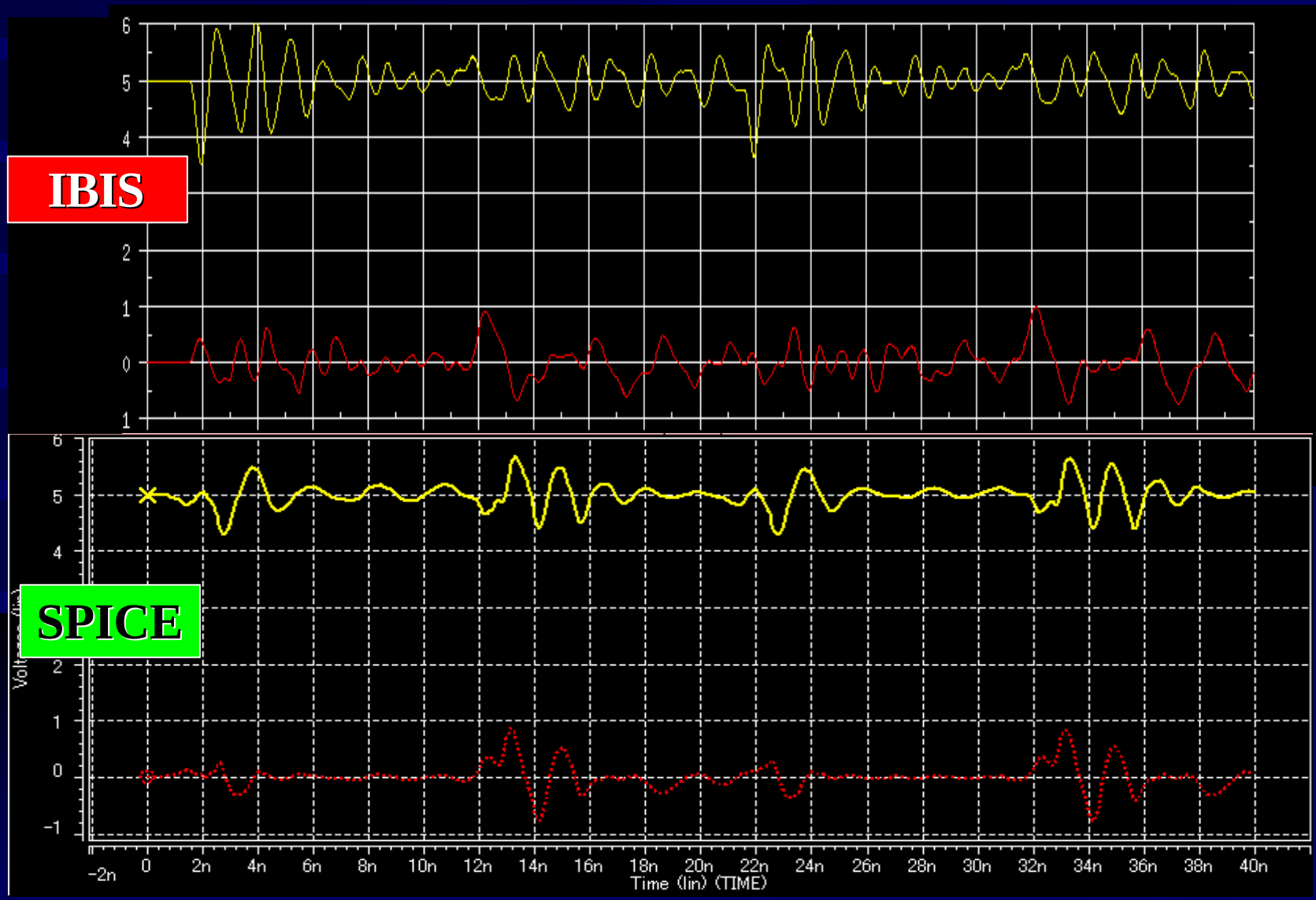
TableSPICE



SPICE

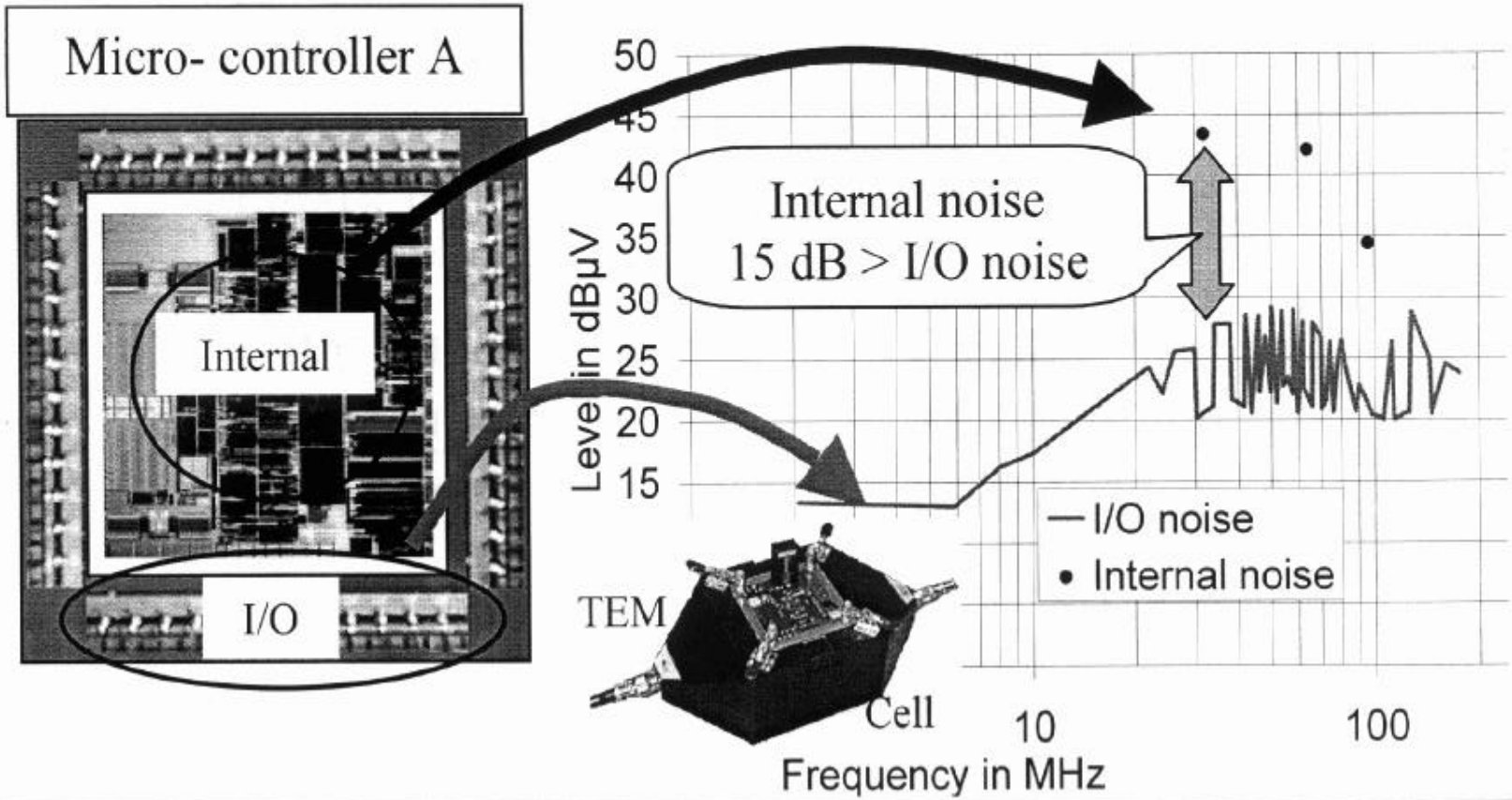


IBIS vs SPICE for SSO for System LSI



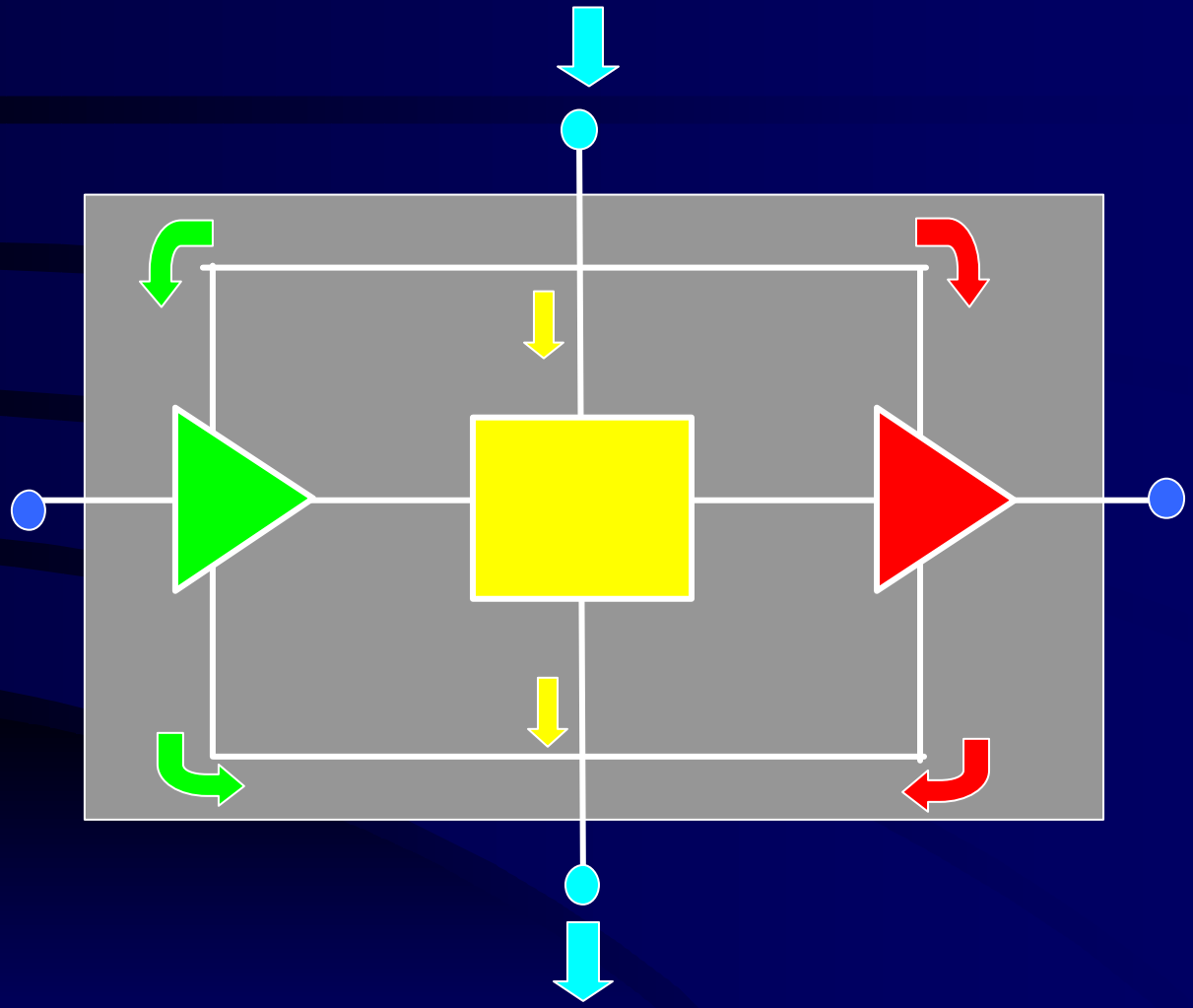
EMC models for Integrated Circuits

★Increased role of IC in global EMC behaviour of equipments and systems



Source : EMC Models for Integrated Circuits by Marot Christian (Siemens)

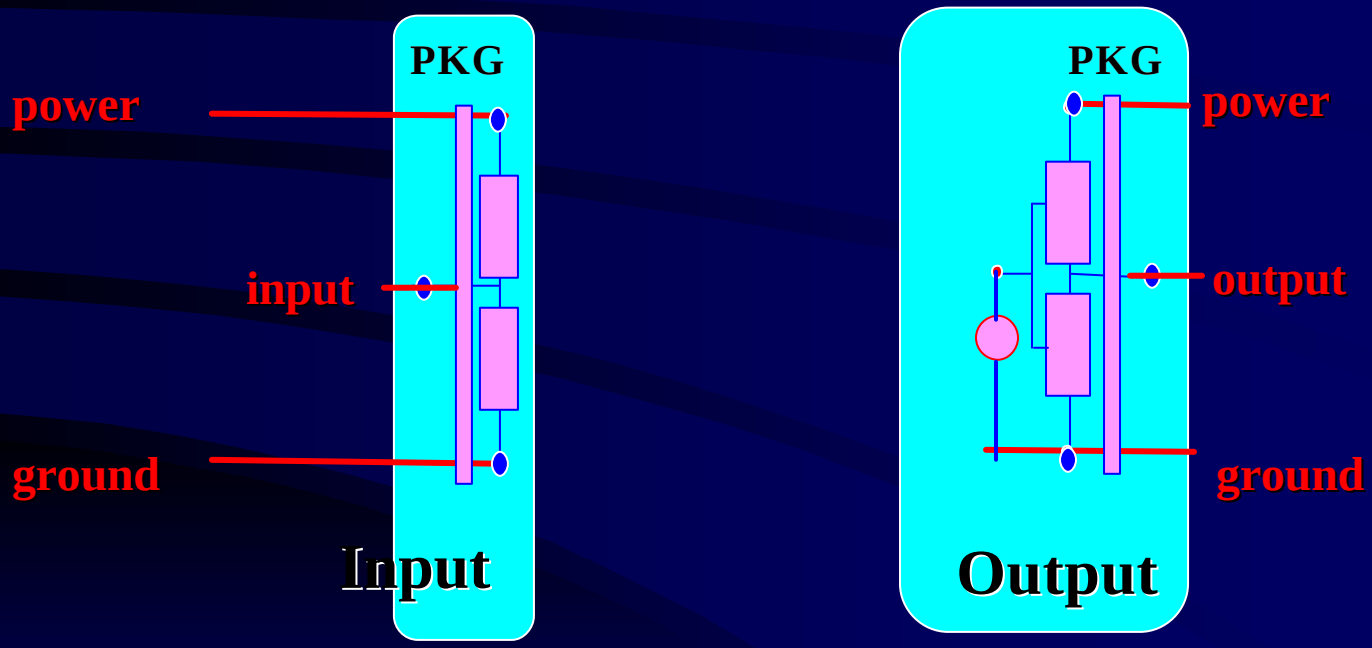
SSO/EMI needs Internal Currents and Impedance



2. LSI Power and Ground Modeling

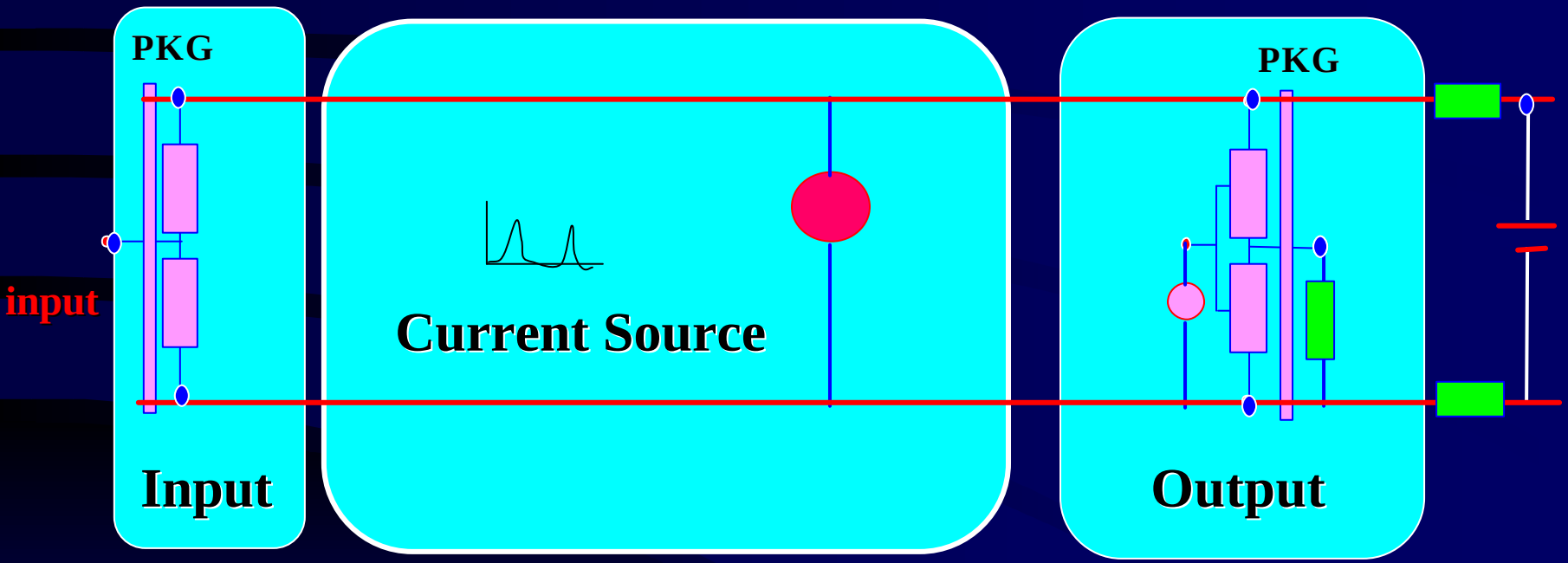
Conventional Model（I/O）

Can’t describe internal currents

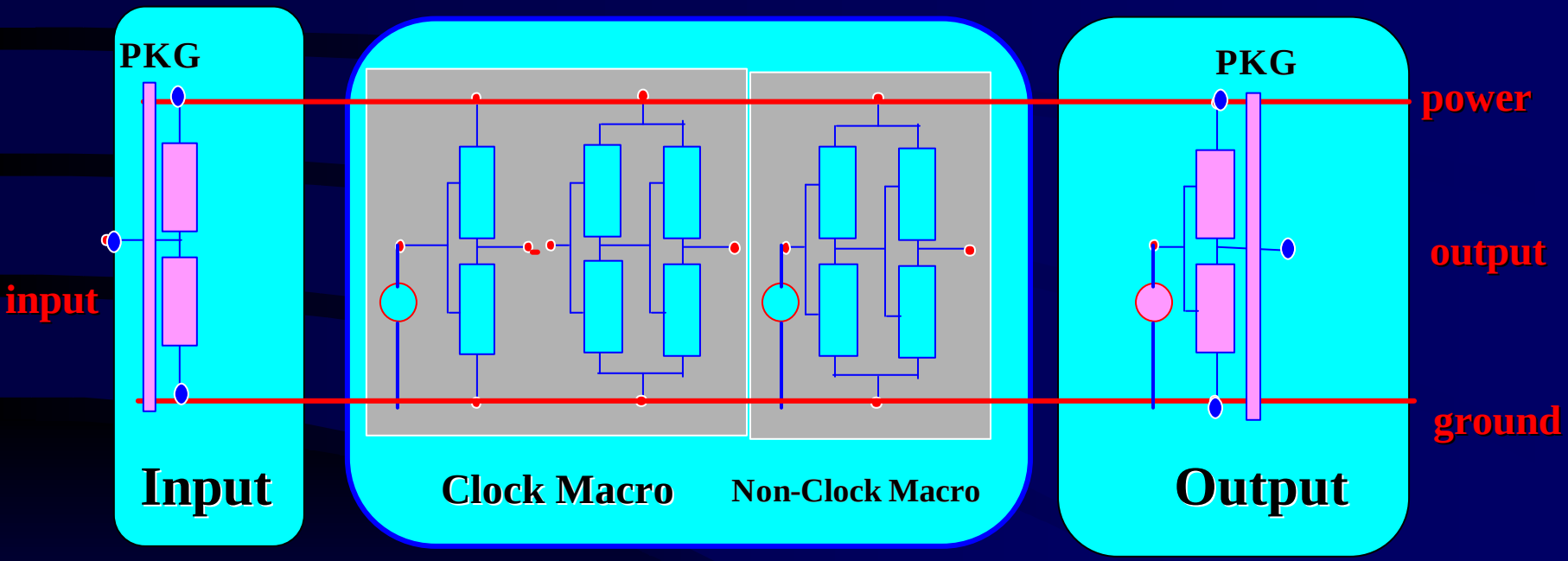


Conventional Model (Internal Current Source)

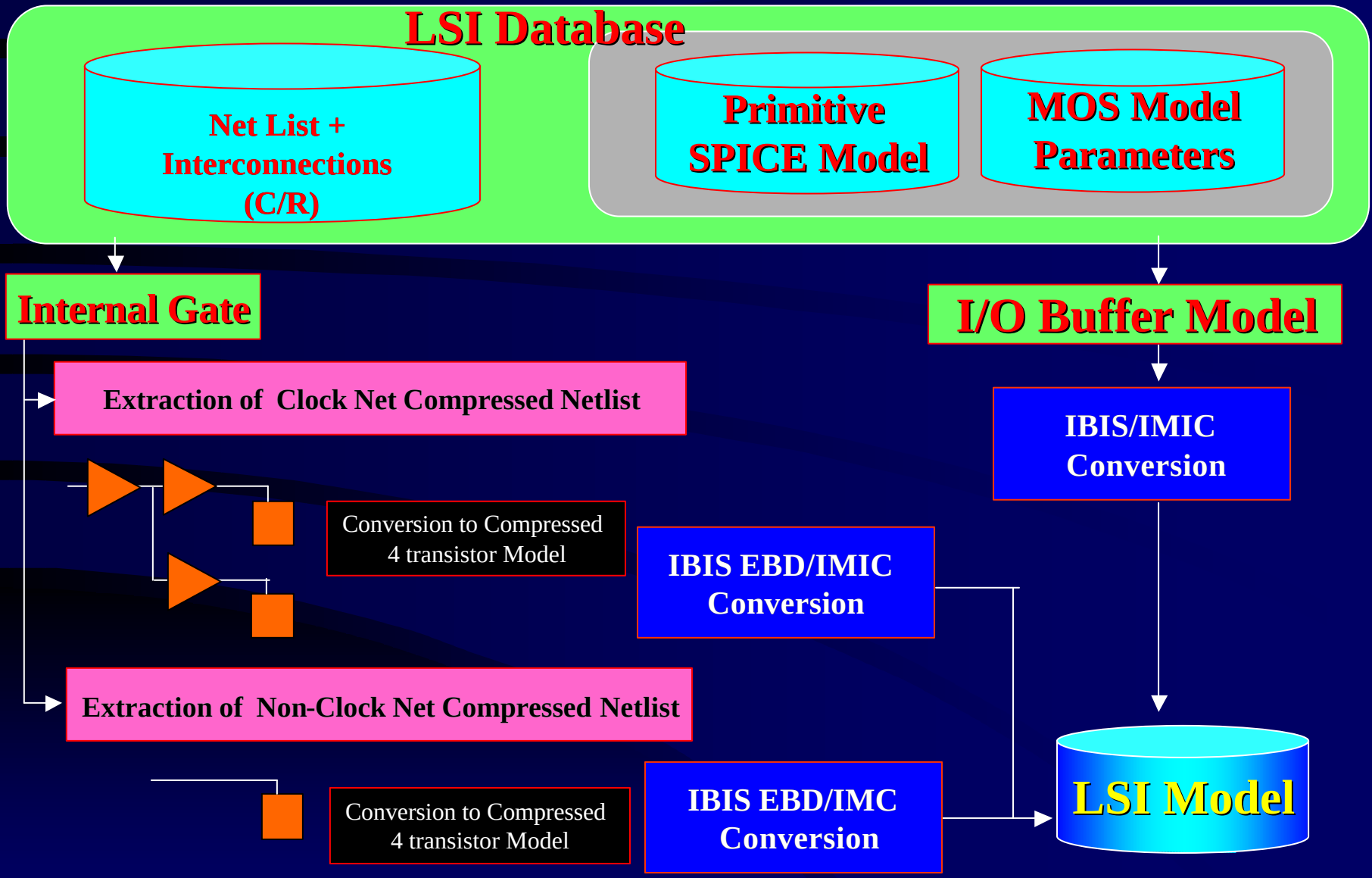
(Can't consider loading effect)



New Model



Data Flow in Modeling



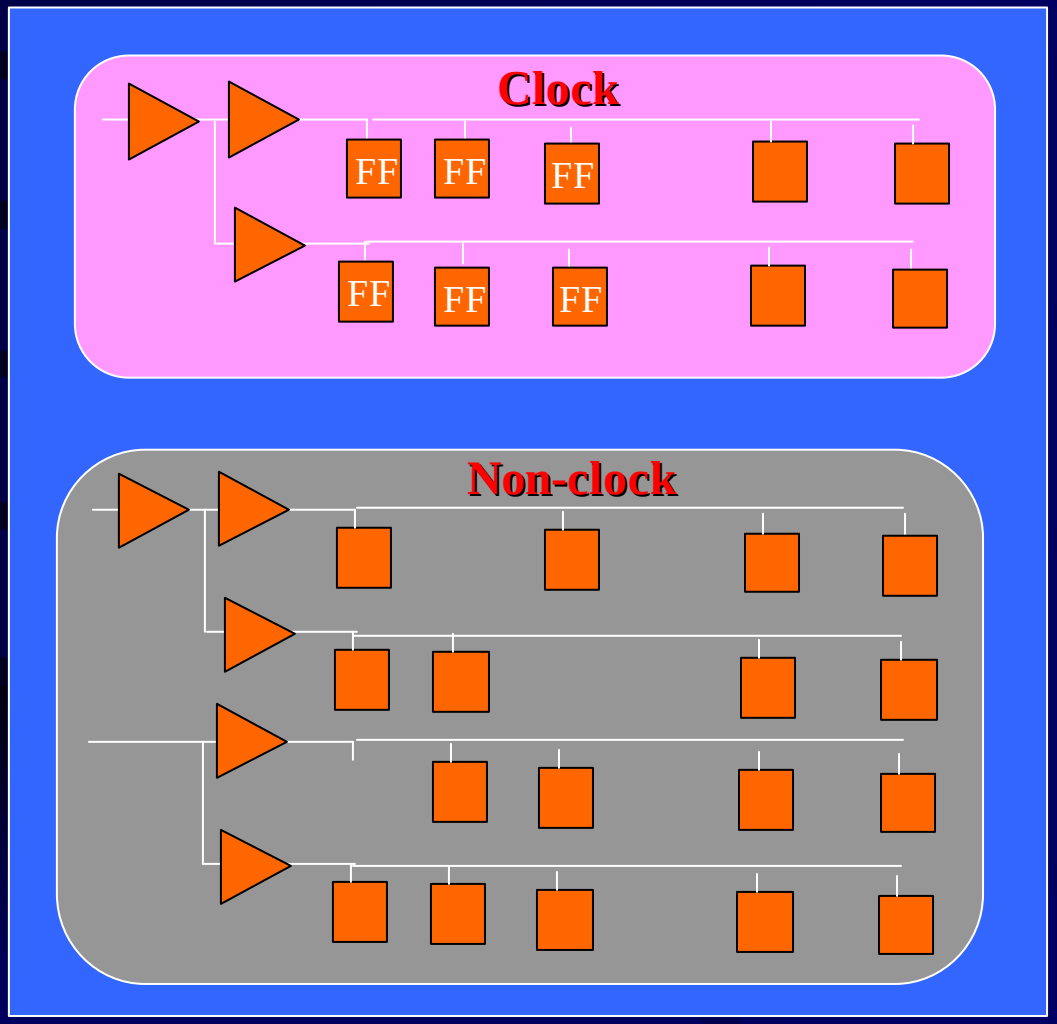
Techniques in Macro Modeling

- *I/O* — *IBIS or IMIC for I/O + Package*
- *Clock* — *10% consumes most power (highest Frequency)*
- *Non-Clock* — *Behaves as Filters/Decoupling Capacitors*

All Primitive Circuits will be decomposed into Two Invertors.
Added gate width as large transistors.
Net List Description of Internal Gates using EBD.
IBIS/EBD or IMIC (to be used existing tools)

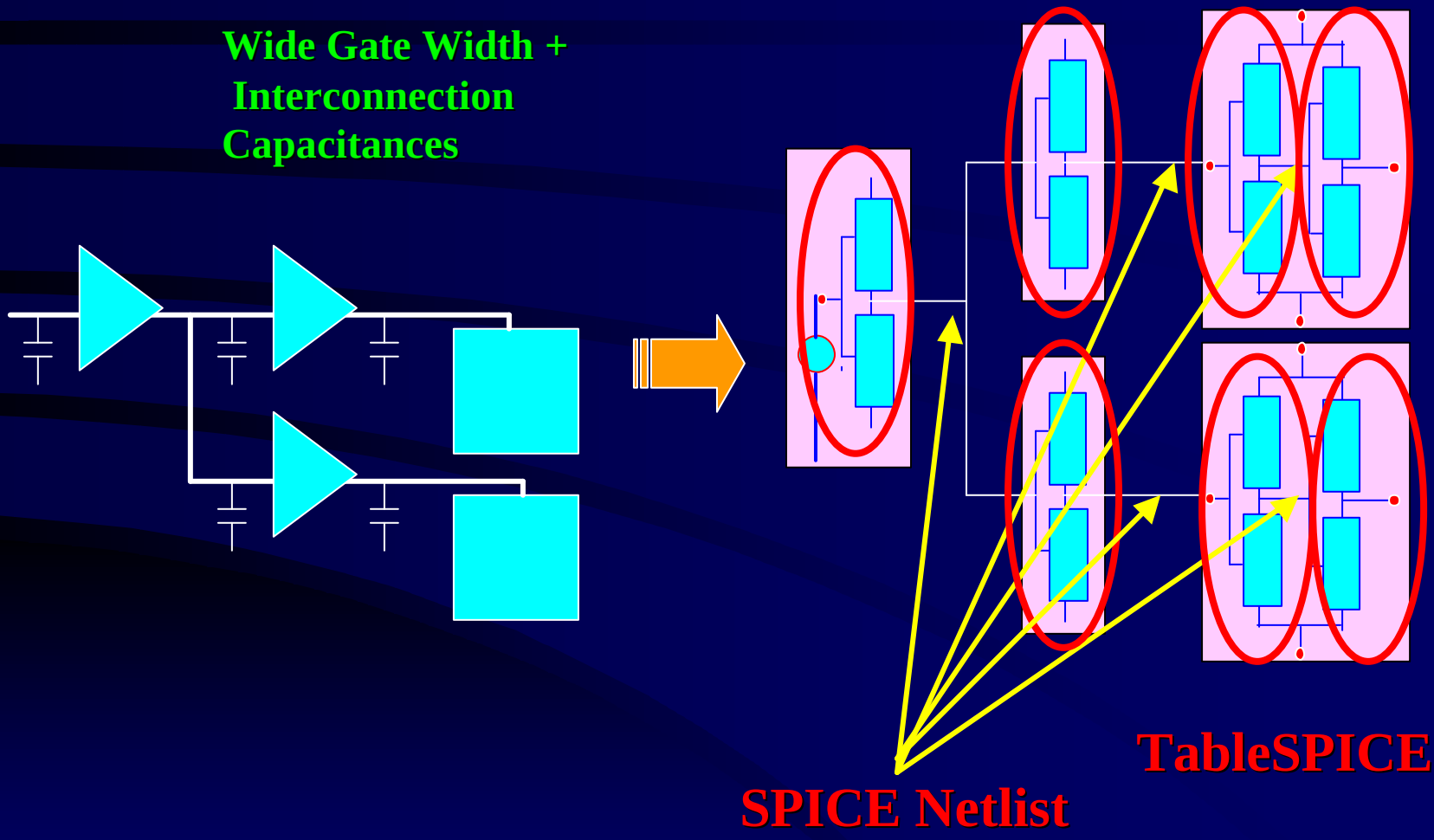
Procedures of Macro Modeling

Wide Gate Width + Interconnection Capacitances



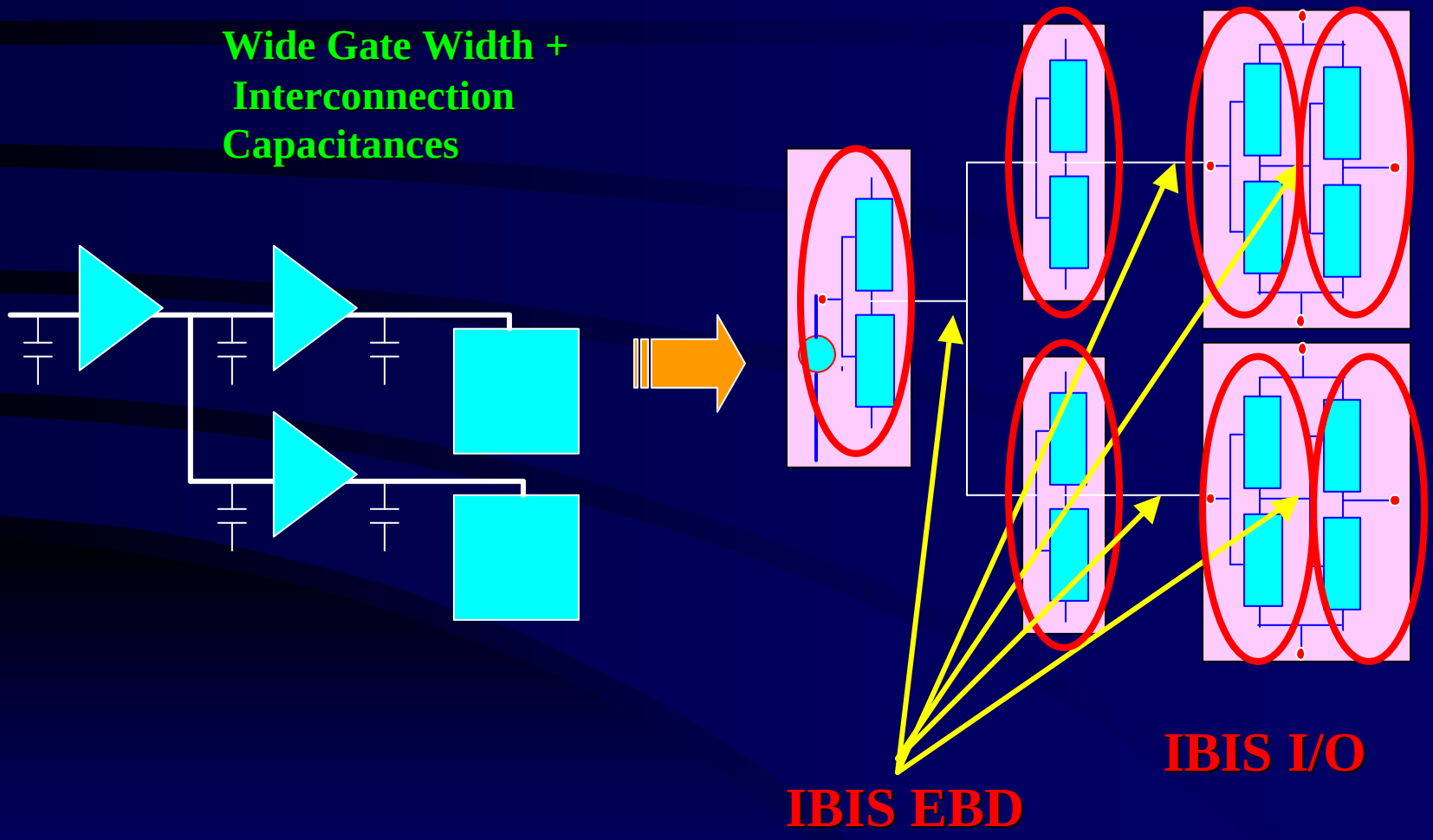
Net List described in IMIC (TableSPICE)

Wide Gate Width +
Interconnection
Capacitances

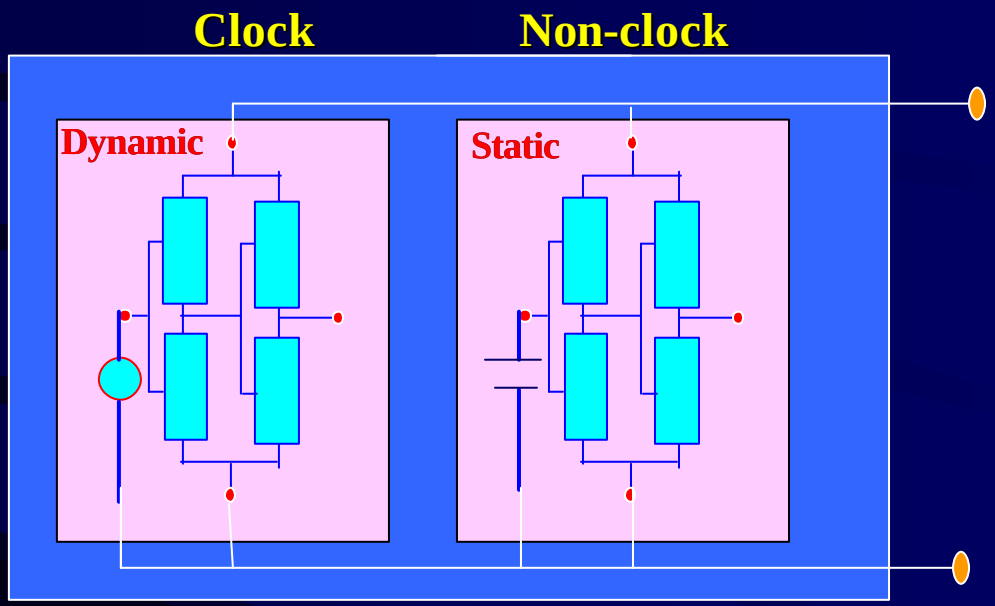


Netlist described in IBIS/EBD

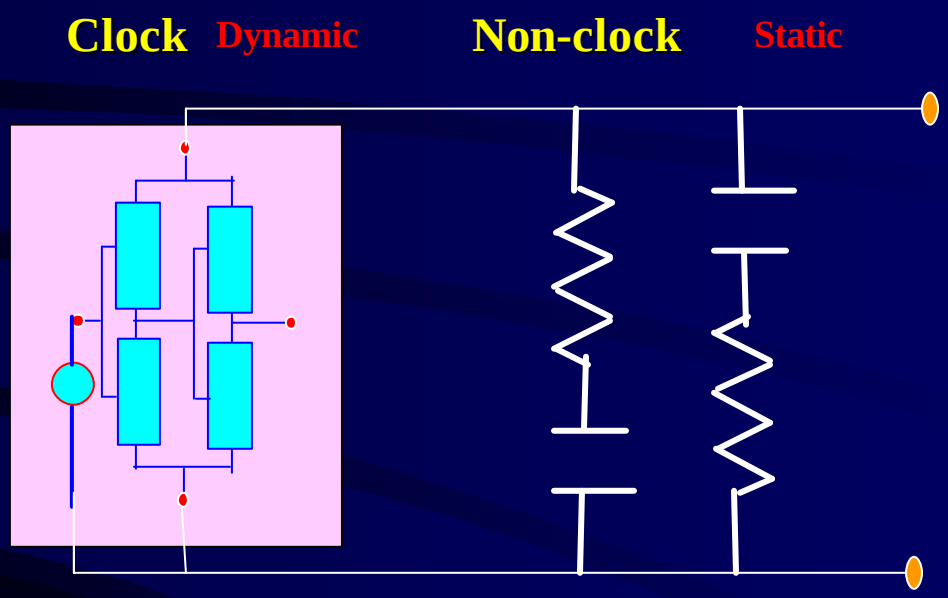
Wide Gate Width +
Interconnection
Capacitances



Clock and Non-clock Model

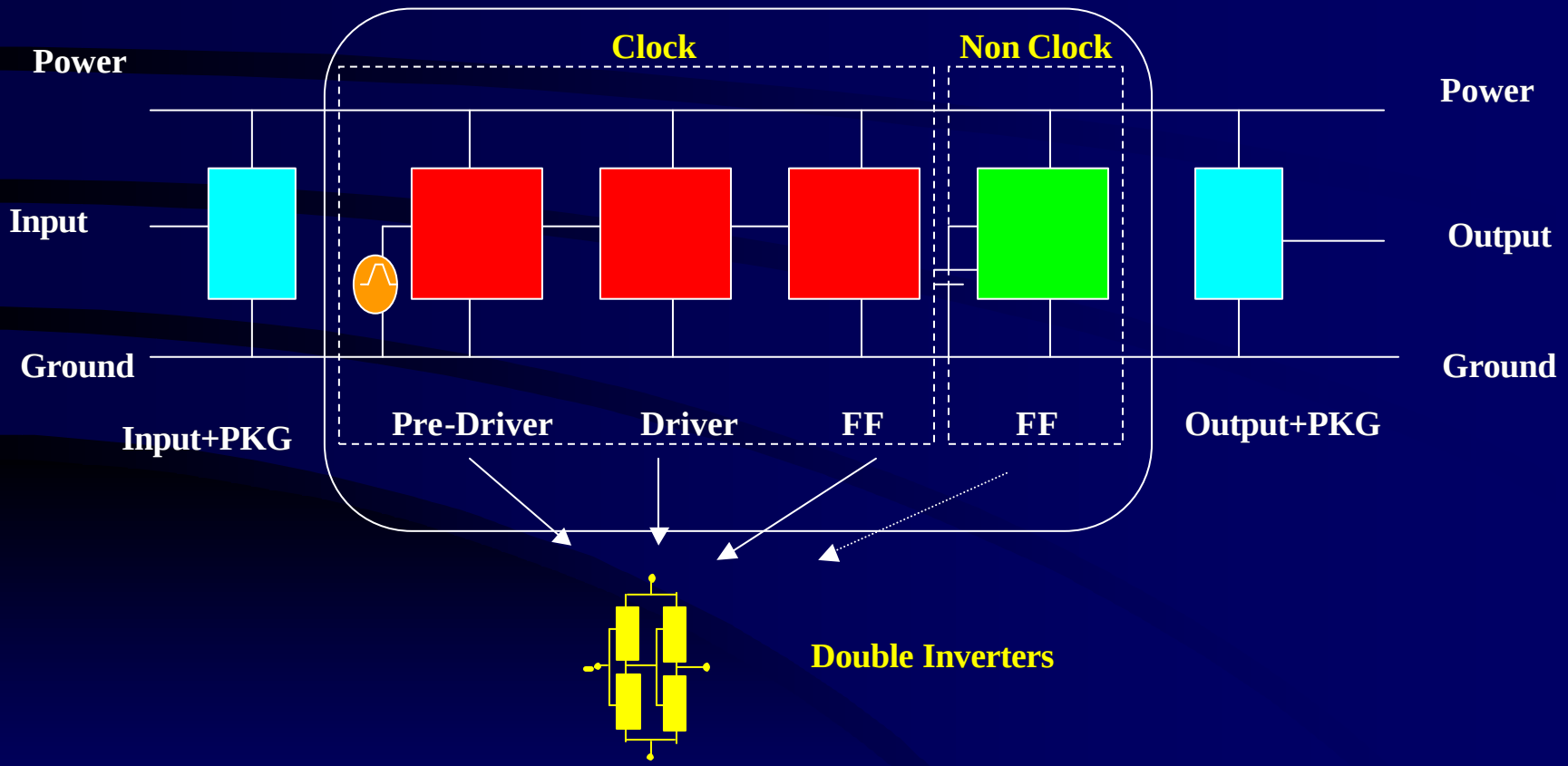


Simplest Model in IBIS Format

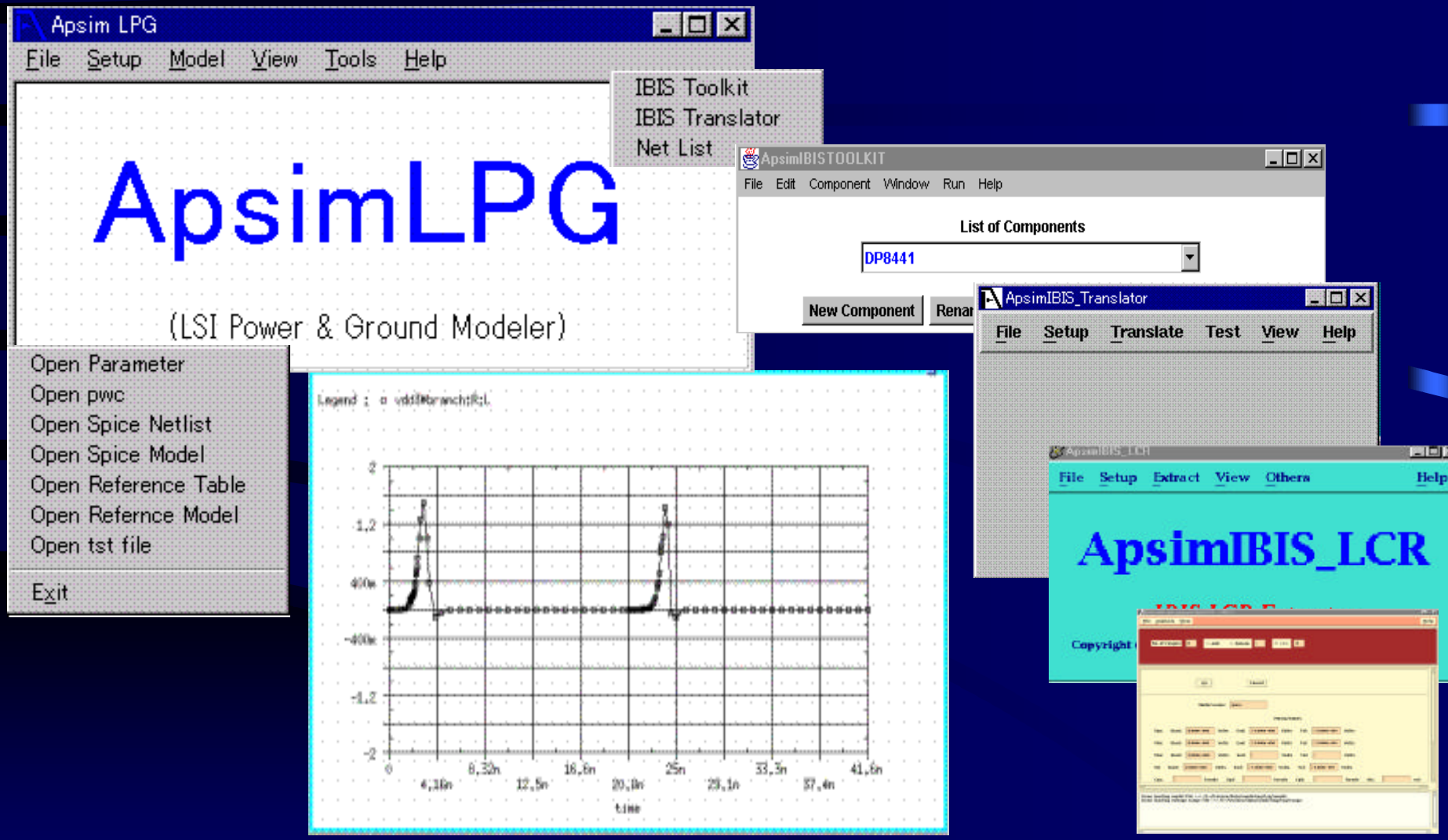


Cascaded Double IBIS I/O

Final Model described in IBIS/EBD or IMIC



Total Current Waveforms for 32 bit LSI



IBIS/EBD, IMIC Model

500 Tr Model

```
Apsim LSI Powre and Ground model ckt file
* Command:       ApsimLPG      1.000.d
* Date:  Mon Jan 29 21:37:24 2001
* File:  a.ckt
* NetList
xclock1 IN D2P_N0039026 D2P_N0000004 D2P_N0000003 D2P_N0000002 D2P_N0000001 clock1
cD2P_N0039026_1 D2P_N0039026 VDD 2.192774e-013
cD2P_N0039026_2 D2P_N0039026 VSS 2.192774e-013
xD2P_I0033331.in VDD VSS D2P_N0039026 mid_D2P_I0033331 F111.in
xD2P_I0033331.out VDD VSS mid_D2P_I0033331 D2P_N0029114 F111.out
cD2P_N0029114_1 D2P_N0029114 VDD 5.332500e-016
cD2P_N0029114_2 D2P_N0029114 VSS 5.332500e-016
xD2P_I0033330.in VDD VSS D2P_N0029114 mid_D2P_I0033330 F111.in
xD2P_I0033330.out VDD VSS mid_D2P_I0033330 D2P_N0028992 F111.out
cD2P_N0028992_1 D2P_N0028992 VDD 3.680150e-015
cD2P_N0028992_2 D2P_N0028992 VSS 3.680150e-015
xD2P_I0033329.in VDD VSS D2P_N0028992 mid_D2P_I0033329 F111.in
xD2P_I0033329.out VDD VSS mid_D2P_I0033329 D2P_N0028991 F111.out
cD2P_N0028991_1 D2P_N0028991 VDD 8.436000e-016
cD2P_N0028991_2 D2P_N0028991 VSS 8.436000e-016
```

IMIC MOS

```
* Thu Aug 10 11:29:38 PDT 2000
.model NENH nmos model=table
+
+ nolimiting
+ data=channel
+ points=1326
+ grid=yes
+ vbs = 0.000e+00
*   Vgs       Vds          Ids         Cgs         Cgd         Cgb
*
+ 0.000e+00  0.000e+00  0.000e+00  2.093e-16  2.093e-16  2.763e-16
+ 0.000e+00  1.000e-01  1.821e-12  2.093e-16  2.093e-16  2.749e-16
+ 0.000e+00  2.000e-01  2.039e-12  2.093e-16  2.093e-16  2.734e-16
+ 0.000e+00  3.000e-01  2.240e-12  2.093e-16  2.093e-16  2.720e-16
+ 0.000e+00  4.000e-01  2.460e-12  2.093e-16  2.093e-16  2.706e-16
+ 0.000e+00  5.000e-01  2.704e-12  2.093e-16  2.093e-16  2.691e-16
```

Converted IBIS

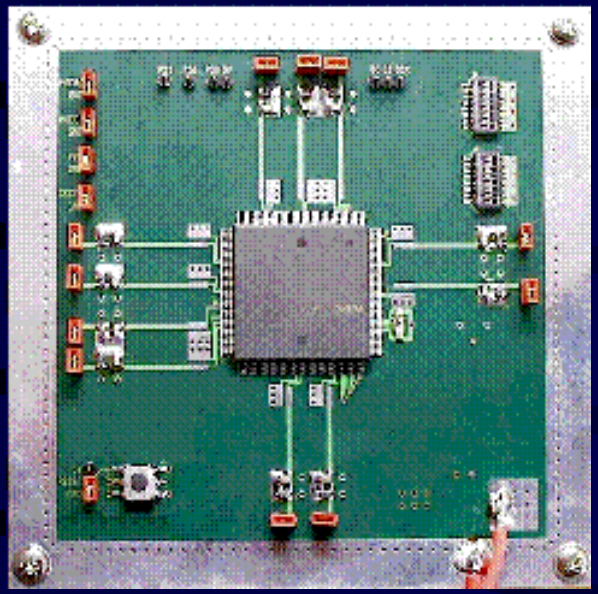
```
Apsim LSI Powre and Ground model ckt file
* Command:       ApsimLPG      1.000.d
* Date:  Mon Jan 29 21:37:24 2001
* File:  a.ckt
* NetList
CIN_1 IN VDD
CIN_2 IN VSS
xCLK.in VDD VSS IN CKLMID CLK.in
xCLK.out VDD VSS CKLMID DRVIN CLK.out
xDRV.in VDD VSS DRVIN DRVMID DRV.in
xDRV.out VDD VSS DRVMID DRVOUT DRV.out
xFF.in VDD VSS DRVOUT FFMID FF.in
xFF.out VDD VSS FFMID OUT FF.out
rFF.out OUT 0 100meg
* Loads
Cp VDD mid1
Rn mid1 VSS
Rp VDD mid2
Cn mid2 VSS
Cli VDD VSS
* Voltage source
vvdd VDD 0 dc 3.3
vvss VSS 0 dc 0.0
* Include file
.include      E:¥lsi_emi¥012901¥a.tst
.include      E:¥lsi_emi¥012901¥mos_tsp.lib
.include      a_t.sub
* Save current
.save vvdd#branch vvss#branch
.end
```

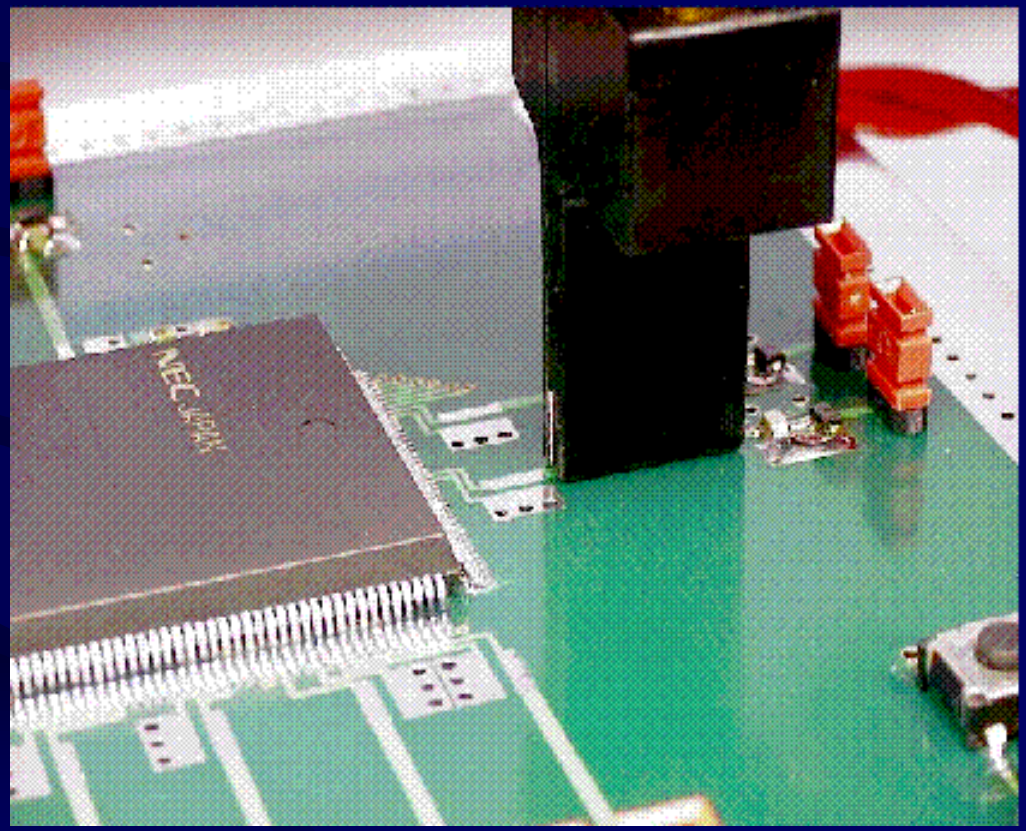
EBD

```
[Begin Board Description]
[Manufacturer]
[Number Of Pins] 5
[Pin List]
1          D2P_N0000001
2          D2P_N0000002
3          D2P_N0000003
4          D2P_N0000004
5          D2P_N0039026
|
[Path Description] D2P_N0000001
Pin 1
Len = 0 C=4.759600e-013 /
Node D2P_I0001118.H01
Node D2P_I0001118.N01
Len = 0 C=5.584200e-013 /|
Node D2P_I0001119.H01
Node D2P_I0001119.N01
Len = 0 C=5.265550e-013 /
Fork
Node D2P_I0001121.H01
Node D2P_I0001121.N01
Len = 0 C=2.773510e-014 /
Node FF3.IN1
Endfork
Fork
Node D2P_I0001120.H01
Node D2P_I0001120.N01
Len = 0 C=2.987680e-014 /
Node FF2.IN1
Endfork
```

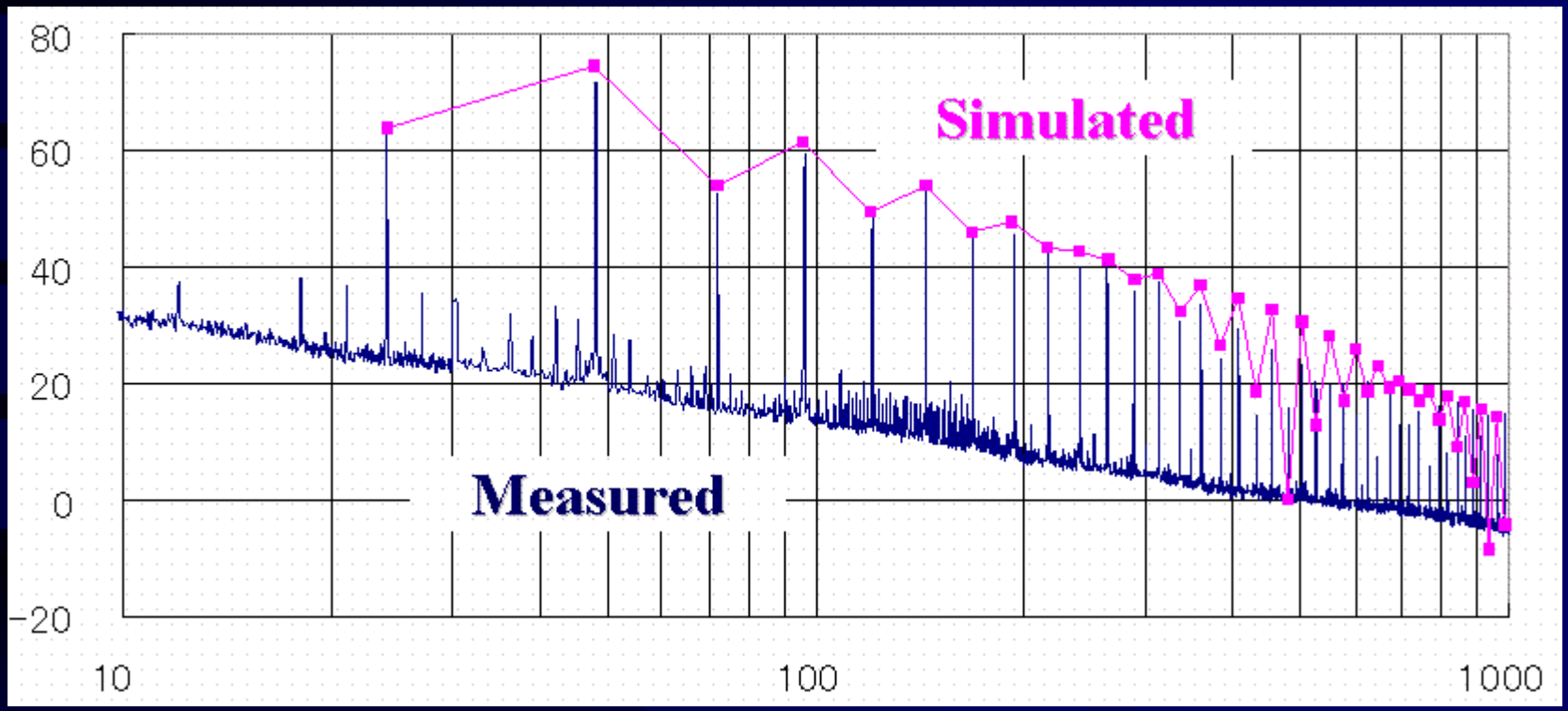
3. Accuracy

Micro Proving Magnetic Fields





Comparison Simulation and Measurement



Various Simplified Models