



# Channel Simulation Using IBIS Models with Asymmetric Rising and Falling Edges

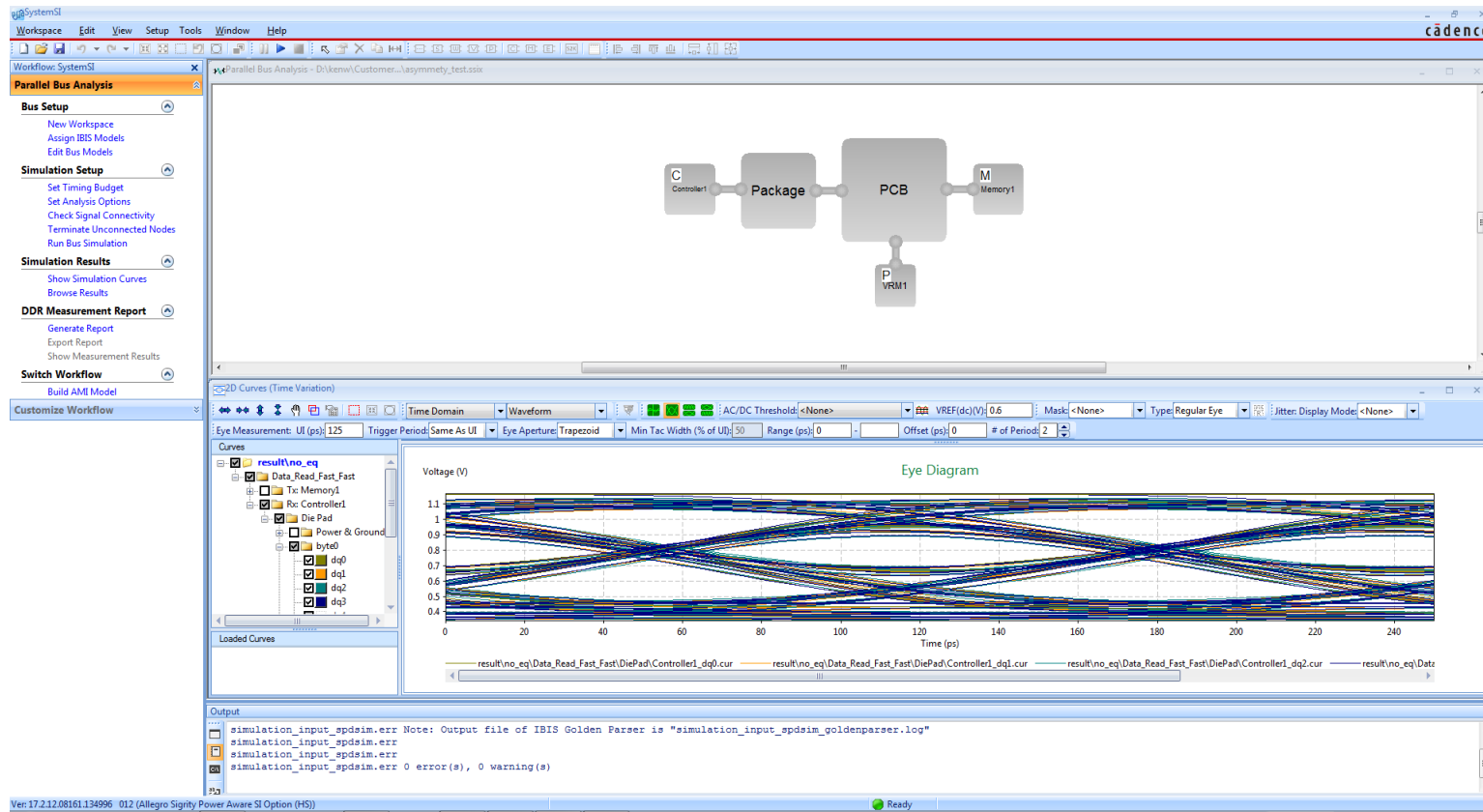
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IBIS Summit – DesignCon 2019  
Santa Clara, California  
February 1, 2019

# Overview

- As channel simulation and IBIS-AMI modeling methods are adapted from serial link to DDR interface analysis, we encounter IBIS IO models with asymmetric rising and falling edges
- This is different from the highly symmetric drivers we typically encounter with serial link analysis
- Traditional single step response methods for impulse response generation may not reproduce circuit simulation results accurately enough
- These slides show how an EDA tool can handle this (without changes to the IBIS specification)
- All cases use Micron's **y11a.ibs** file for 8Gbps DDR5, provided by Randy Wolff

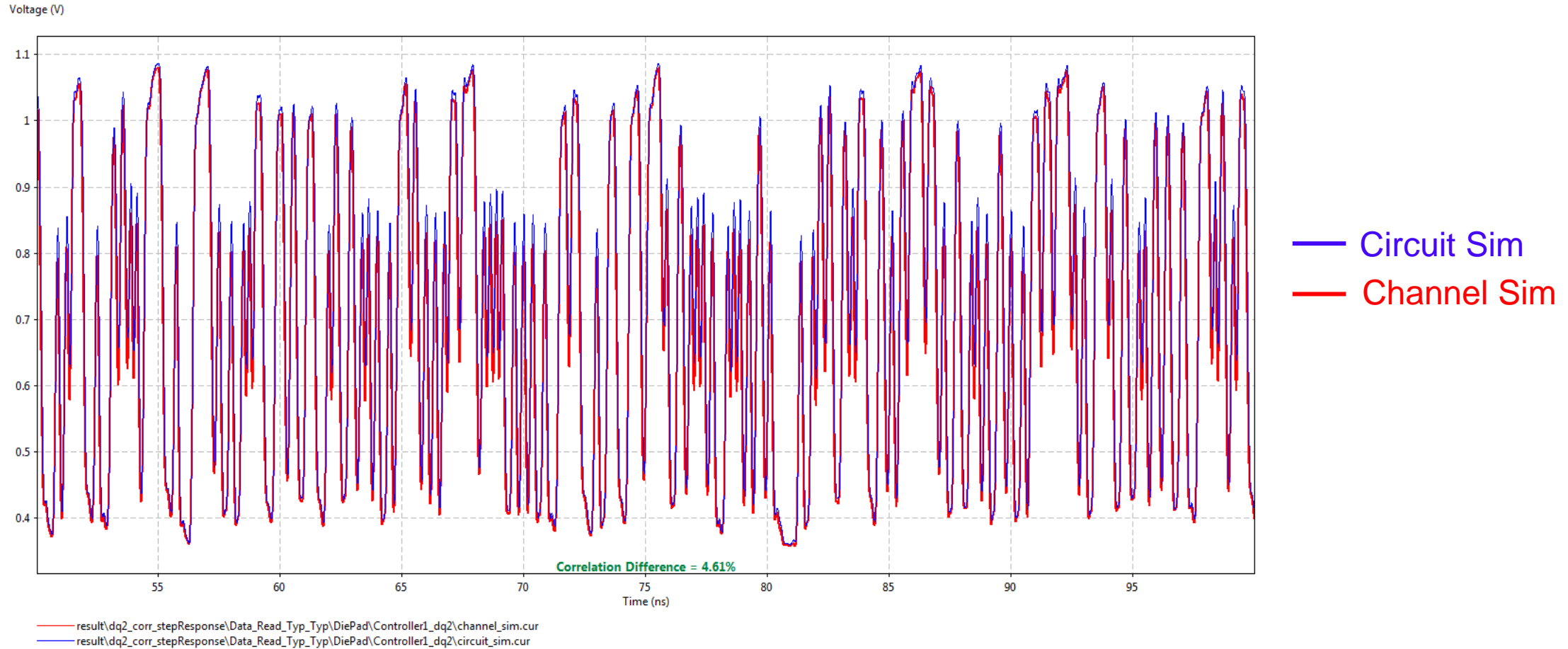
# SystemSI Testbench

- Package block uses an extracted RLCK Spice model
- PCB block uses W-elements with 0.3 meter lengths

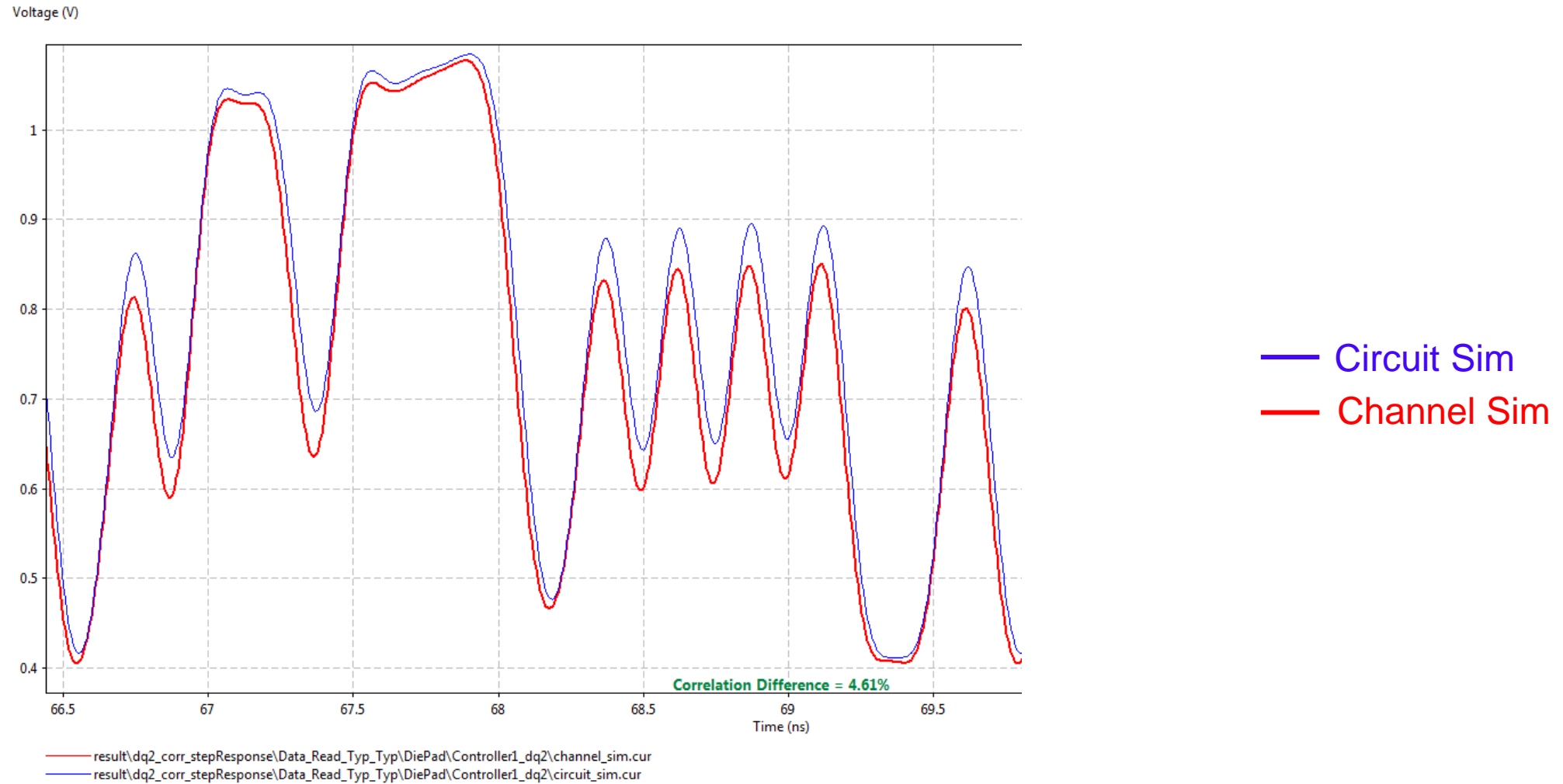


# Using Standard Step Response Characterization

- Correlation difference 4.61%

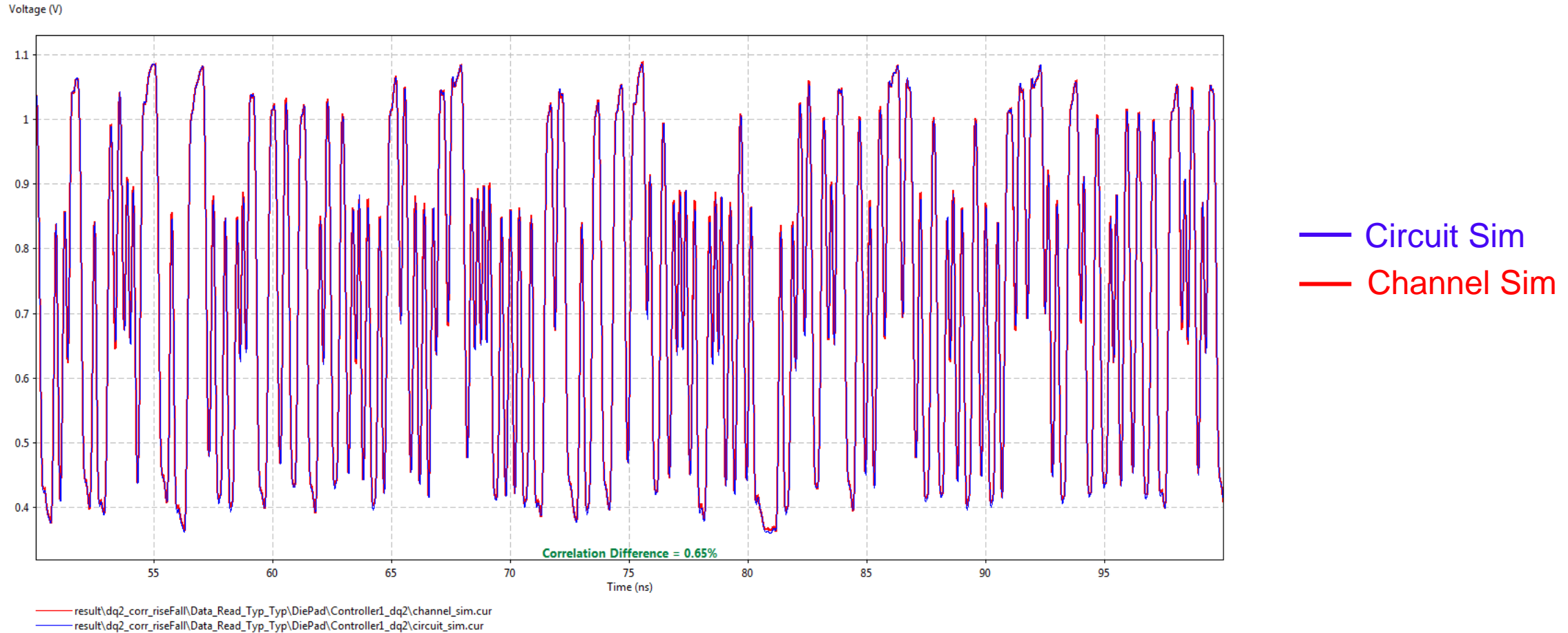


# Same Result Zoomed In

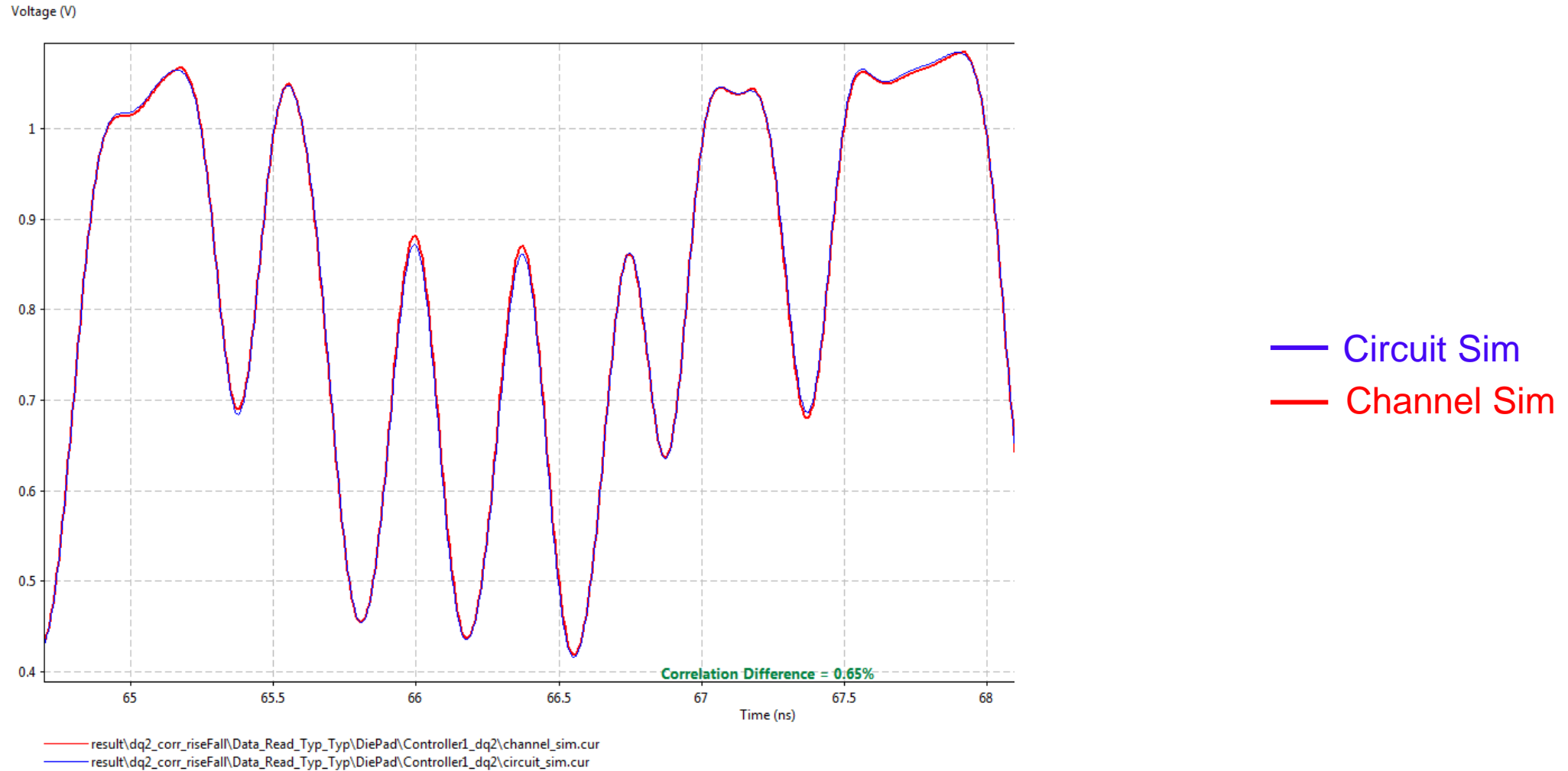


# Using Rising and Falling Edge Characterization

- Correlation difference 0.65%

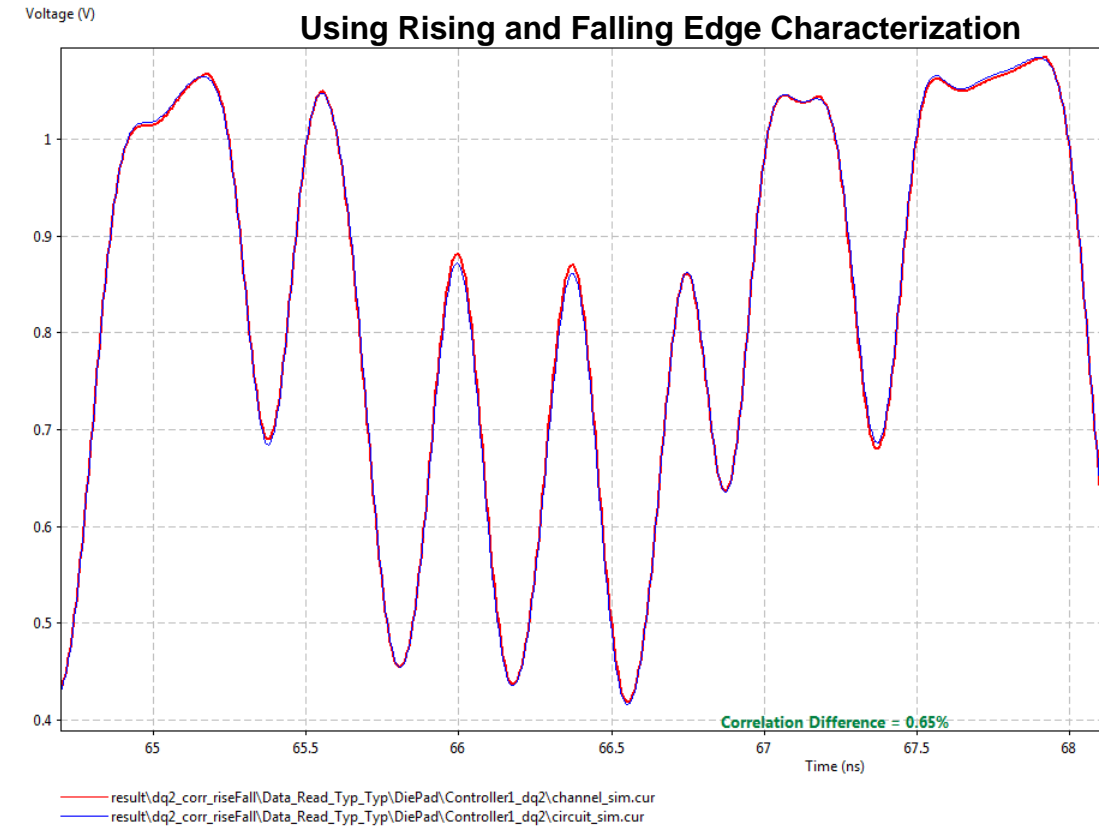
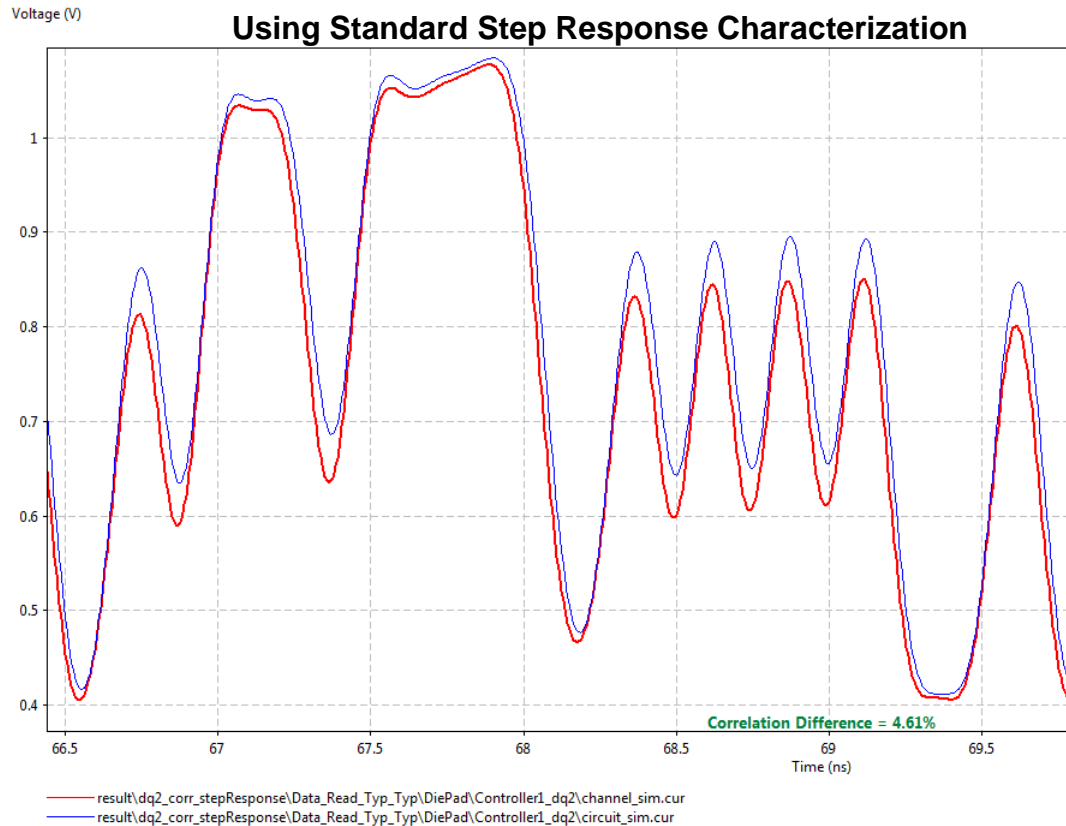


# Same Result Zoomed In



# Comparison of Both Methods

- Correlation error vs. circuit simulation reduced by about 4%





# Summary

- The **DQ\_34\_3600** IO model has some asymmetry in its rising and falling edges
- Standard SerDes step response characterization did not do a great job in capturing this behavior, as seen in the circuit / channel sim correlation
- Characterization methods using rising and falling edges captured this behavior very well for channel simulation

```
| *****  
|  
| [Ramp]  
| R_load = 50  
|  
|          typ          min          max  
|  
| dV/dt_r 3.7990E-01/6.4024E-11  3.4860E-01/8.7846E-11  4.0938E-01/4.9359E-11  
| dV/dt_f 4.4605E-01/5.4840E-11  4.2048E-01/7.6564E-11  4.6793E-01/4.2557E-11  
| *****
```

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