**IBIS On-Site and Virtual Summit with DesignCon 2022**

April 8, 2022

**Agenda**

All times PDT

|  |  |
| --- | --- |
| 8:00 AM  8:15 AM | **CHECK IN AND REFRESHMENTS**  **Meeting Welcome** Randy Wolff (Micron Technology, USA)  (Chair, IBIS Open Forum) |
| 8:20 AM | **IBIS Chair’s Report**  Randy Wolff (Micron Technology, USA)  (Chair, IBIS Open Forum) |
| 8:40 AM | **Fitted Poles/Residues: File Format, Transformations, Limitations**  Vladimir Dmitriev-Zdorov (Siemens EDA, USA) |
| 9:10 AM | **Circuit Synthesis of Multiport Networks from Passive Poles and Residues**  Chiu-Chih Chou\*, Jose Schutt-Aine\*\*  (National Central University, ROC\*; University of Illinois, USA\*\*)  [Presented by Chiu-Chih Chou\*, Jose Schutt-Aine\*\*] |
| 9:40 AM | **Questions and Discussion** |
| 10:00 AM | **BREAK (10 minutes)** |
| 10:10 AM | **Time-Domain Extraction and SPICE Macromodeling**  Bob Ross (Teraspeed Labs, USA) |
| 10:55 AM | **Port Naming Enhancement for Touchstone Files**  Walter Katz (MathWorks, USA) |
| 11:10 AM | **Discussion** |
| 11:25 AM | **IBIS-AMI Modeling and Correlation Methodology for ADC-Based SerDes Beyond 100Gbps**  Aleksey Tyshchenko\*#, Clinton Walker\*\*##, David Halupka\*#, Richard Allred\*\*\*##, Tripp Worrel\*\*\*##, Barry Katz\*\*\*##, Adrien Auge\*\*#  (SeriaLink Systems\*, Alphawave IP\*\*, MathWorks\*\*\*; Canada#, USA##)  [Presented by Aleksey Tyshchenko (SeriaLink Systems, Canada)] |
| 11:55 AM | **Free On-Line SerDes System Channel Simulation**  John Baprawski (SerDesign.com, USA) |
| 12:25 PM | **CLOSING REMARKS**  - Next IBIS Open Forum Meeting on April 22, 2022 |
| 12:30 PM | **FREE LUNCH, NETWORKING**  End of Virtual Meeting |
| 1:00 PM | **END OF MEETING** |

