**IBIS Open Forum Minutes**

Meeting Date: **May 11, 2016**

Meeting Location: **SPI-E IBIS Summit, Turin, Italy**

**VOTING MEMBERS AND 2016 PARTICIPANTS**

ANSYS Curtis Clark, Toru Watanabe

Applied Simulation Technology (Fred Balistreri)

Broadcom (Avago Technologies) Bob Miller

Cadence Design Systems Ken Willis, Brad Brim

Cisco Systems Giuseppi Selli, Brian Baek

CST Stefan Paret\*

Ericsson Anders Ekholm, David Zhang, Zilwan Mahmod\*

GLOBALFOUNDRIES Steve Parker

Huawei Technologies (Jinjun Li)

IBM Adge Hawes, Luis Armenta

Infineon Technologies AG (Christian Sporrer)

Intel Corporation Hsinho Wu, Mohammad Bapi, Michael Mirmak,

 Masahi Shimanouchi, Todd Bermensolo, Zao Liu,

 Gong Ouyang, Udy Shrivastava, Gianni Signorini\*,

 Richard Mellitz\*

IO Methodology Lance Wang\*

Keysight Technologies Radek Biernacki, Heidi Barnes\*, Jian Yang, Fangyi Rao, Stephen Slater, Pegah Alavi, Edwin Young

Maxim Integrated Products Yan Liang, Don Greer, Thinh Nguyen, Joe Engert,

 Hock Seon

Mentor Graphics Arpad Muranyi, Vladimir Dmitriev-Zdorov, John Angulo,

 Mikael Stahlberg\*

Micron Technology Randy Wolff\*

Signal Integrity Software Mike LaBonte, Walter Katz\*, Todd Westerhoff,

 Richard Allred\*

Synopsys Ted Mido, Kevin Li, Massimo Prando\*

Teraspeed Labs Bob Ross

Toshiba (Yasumasa Kondo)

Xilinx (Raymond Anderson)

ZTE Corporation (Shunlin Zhu)

Zuken Michael Schaeder\*, Amir Wallrabenstein

**OTHER PARTICIPANTS IN 2016**

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Fujitsu Advanced Technologies Shogo Fujimori

Ghent University Paolo Manfredi\*

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Hamburg University of Technology Jan Preibisch\*, David Dahl\*

Independent Carl Gabrielson

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KEI Systems Shinichi Maeda

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Monsoon Solutions Nathan Hirsch\*

Northrup Grumman Alex Golian

NXP Jon Burnett

Politecnico di Torino Claudio Siviero\*, Stefano Grivet-Talocia\*,

 Igor Simone Stievano\*

Rambus John Yan

Raytheon Joseph Aday

SAE International (Logen Johnson)

SILABTECH Biman Chattopadhyary

Signal Metrics Ron Olisar

SiGuys Donald Telian\*

Sony Corporation Hiroaki Ammo\*

Sony LSI Design Takashi Hasegawa\*

SPISim Wei-hsing Huang

STMicroelectronics Fabio Brina\*, Olivier Bayet\*

Technoprobe Alberto Berizzi\*, Lorenzo Bernasconi\*, Simona Cucchi\*

Université de Bretagne Occidentale Mihai Telescu\*

In the list above, attendees at the meeting are indicated by \*. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

**UPCOMING MEETINGS**

The bridge numbers for future IBIS teleconferences are as follows:

Date Meeting Number Meeting Password

May 20, 2016 205 475 958 IBIS

For teleconference dial-in information, use the password at the following website:

 <https://ciscosales.webex.com/ciscosales/j.php?J=205475958>

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

 <http://www.cisco.com/web/about/doing_business/conferencing/index.html>

NOTE: "AR" = Action Required.

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**OFFICIAL OPENING**

The IBIS Open Forum Summit was held in Turin, Italy at the Starhotels Majestic Hotel following the 2016 SPI conference. About 30 people (at least 36 people were counted) representing 22 organizations were recorded in attendance.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

<http://www.eda.org/ibis/summits/may16/>

Lance Wang welcomed all the participants and thanked the sponsors ANSYS, CST, Keysight Technologies, Synopsys and Zuken. Lance asked the attendees to introduce themselves. There were a wide variety of people from many countries and organizations including academia and industry.

**IBIS UPDATE**

Mike LaBonte\*, Lance Wang\*\*, \*Signal Integrity Software (SiSoft); USA, \*\*IO Methodology; USA

Lance Wang presented. He noted that the IBIS website is now at <http://ibis.org>. IBIS 6.1 is the latest version, and IBISCHK6.1.2 is available for download. Many updates are in the works within the task groups. Lance encouraged participation within the task groups.

**UNDERSTANDING IBIS-AMI SIMULATIONS**

Richard Allred, Signal Integrity Software (SiSoft); USA

Richard introduced the fundamentals of IBIS-AMI modeling. Models are separated into analog portions and algorithmic portions, separated by a high impedance node. The model may also include a package model. The first analysis stage is network characterization and the second is channel simulation. The output of network characterization is the impulse response of the channel. Statistical analysis can be performed with IBIS-AMI. Time domain simulation is also possible, and this is useful for adaptive RX equalization. Models can be either statistical, time domain based, or both. Richard described three of the most used simulation cases for combinations of RX and TX models. It is important to understand the model capabilities so that any type of dynamic equalization is properly included. He went on to describe recovered clock processing and the handling of jitter and noise.

Richard Mellitz asked how crosstalk analysis is incorporated into IBIS-AMI. Richard Allred described that after the analog channel is characterized, there are impulse responses for the main channel as well as impulse responses for the crosstalk. How the crosstalk is processed is up to the AMI model maker. The simulator determines the phase of the crosstalk. Walter Katz noted that there is no crosstalk cancellation in IBIS-AMI.

**USING IBIS-AMI MODELS TO MAXIMIZE DATA RATE GIVEN SERDES EQ AND CHANNEL ISI/LOSS**

Donald Telian, SiGuys; USA

Donald Telian noted that IBIS-AMI is the biggest discontinuity in IBIS, allowing for the processing of millions of bits. AMI modeling has matured significantly. When analyzing system level simulations, thousands of channels can be reduced into points on a chart of eye height versus eye width. Thousands of links are still “serial” in that they are differential with some equalization, but there can be many parallel links. When analyzing performance, the relevant metric is bit error rate (BER), not eye height and eye width, but a combination of eye metrics which may be plotted as a diagonal line. Signal integrity is not only a focus on passive channel improvements but also RX and TX settings handled through firmware. Equalization complexity is increasing more in the RX than the TX. Training algorithms are becoming increasingly popular. Donald warned that AMI model EQ settings do not always match hardware register settings.

He compared an ideal pulse response of a channel to a realistic pulse response with peak voltage less than the step response voltage and a long tail. Equalization will reduce the eye height but remove most ISI at the sampling time. Some ISI cannot be removed. A TX post-cursor equalization and RX CTLE can have similar effects on the pulse response. TX equalization is best at pre-cursor equalization.

Donald described a case study of co-optimizing TX and RX settings for several SerDes channels. For PAM4 channels, co-optimization will be very important.

**INITIAL DELAY ISSUES IN ANALOG IBIS BUFFERS**

Michael Schaeder, Mariusz Faferko, Amir Wallrabenstein, Zuken; Germany

Michael Schaeder noted that initial delay issues have been discussed for many years. Most models show some initial delay in their V-T waveforms. He reviewed the general IBIS simulation equations. An example of k-table coefficients was shown for some [Rising Waveform]s. Initial delay can cause overclocking problems unless it is removed. Manual trimming of V-T waveforms can be done. Michael showed some automatic waveform trimming approaches that define a tolerance range based on a percentage of the total signal swing. Both approaches are sensitive to waveform specific tolerances. Another approach is based on absolute tolerance of the 0/1 levels of the k-table. The [Initial Delay] keyword is available in IBIS 6.1 for model makers to specify initial delay removal times specific to V-T and I-T waveforms. An IBISCHK enhancement is needed for the parser to check I-V and V-T mismatch at the [Initial Delay] time.

**IBIS + MPILOG: CURRENT AND FUTURE DEVELOPMENTS ON I/O-BUFFER MODELING**

Gianni Signorini\*#, Claudio Siviero\*\*##, Igor Simone Stievano\*\*##, Stefano Grivet-Talocia\*\*##, Michael Mirmak\*###, \*Intel Corporation, \*\*Politecnico di Torino; #Germany, ##Italy, ###USA

Gianni Signorini presented. He noted requirements for an I/O macromodel (DUM is a Device Under Modeling). He began by showing the two-piece modeling structure available in IBIS and its circuit equivalent. For power-awareness, coefficients are calculated from an IBIS 5.0 model to approximate supply noise effects on output static characteristics. Inaccuracies exist because switching profiles can have complex dependencies with supply voltage variations. Pre-driver/crowbar current also has a complex dependency with supply voltage variations. Supply port impedance is also important to model correctly.

Gianni introduced an advanced model structure to capture 3-D surface characteristics of I-V and V-T switching including power supply variation. The advanced model correlates very well to Spice model simulations. He proposed a method to enhance IBIS models by using the 3-column data approach of IBIS to approximate a 3-D surface model. The data tables model a single Process-Time corner with VDD variation.

Donald Telian asked how the data tables are implemented. Gianni responded that the data tables are still lookup tables, but they implement an additional variable. Michael Schaeder noted that original IBIS supports multiple waveform tables. He wondered if the effects could be included with multiple waveform tables. Gianni responded that the data just needs to be included in a supported fashion, whatever format that is.

**MODELS FOR IC BUFFERS: A TOP-DOWN APPROACH**

Cherif Diouf\*#, Mihai Telescu\*\*#, N. Tanguy\*\*#, Igor Simone Stievano\*\*\*##, Flavio G. Canavero\*\*\*#, \*Ecole Nationale d’Ingénieurs de Brest, \*\*Université de Bretagne Occidentale, \*\*\*Politecnico Di Torino; #France, ##Italy

Mihai Telescu presented a nonlinear Thévenin-like model for IC buffers inspired by the Thévenin model for linear circuits. The general idea for the model was presented at the SPI IBIS Summit meeting in 2013.

One advantage of the model compared to an IBIS model is a solution to overclocking, as the output of the algorithms is dependent on the input for both weighted switching functions as well as conductance modeling. A hybrid approach to an IBIS model takes the IBIS weighting functions and drives them through a Hammerstein structure. The model can be implemented with standard Spice simulations and standard Spice elements. Power supply variation modeling is also being added to the model. The model has good potential for solving inaccuracies related to overclocking and jitter.

**MULTIPORT I/O MODEL COMPUTATION FOR POWER-AWARE SI SIMULATION**

Wael Dghais\*, Fethi Bellamine\*\*, \*Institut Supérieur des Sciences Appliquées et de Technologie de Sousse, \*\*Université de Carthage; Tunisia

Wael Dghais presented. He described the derivation of a hybrid automaton IBIS driver model that implements continuous switching behavior mixing the event-triggered pre-driver’s switching dynamics with the non-linear steady state dynamics of the pullup and pulldown models of the driver’s last stage. The model also includes power-aware effects such as gate modulation and switching currents through both the power and ground nodes.

Walter Katz noted that in IBIS you present a data table and the EDA tool interprets the data for simulation. Using a .dll where you give the ports of the buffer and you implement the algorithms in a standard way for EDA software to execute them could be viable. Wael noted that there are circuit elements that could be used in the model, or Verilog-A, but an executable could work. Walter added that it has been difficult to implement simple ideas in IBIS, so a complex model would be best implemented in a .dll executable format.

**ON-DIE DECOUPLING MODEL IMPROVEMENTS FOR IBIS POWER AWARE MODELS**

Randy Wolff#, Aniello Viscardi##, Micron Technology; #USA, ##Italy

Randy Wolff presented. He noted that on-die decoupling models for power aware modeling must be added external to the IBIS model currently. To correlate an IBIS model simulation with a transistor model simulation, the decoupling model may need multiple terminals. A Spice model may include a pre-driver on a separate power supply from the driver, and coupling may exist between the pre-driver supply and the final driver supply. The pre-driver and final driver may also share a common ground. One method for creating a non-proprietary decoupling model involves creating an S-parameter model. The S-parameter model could have multiple port options and may require a node 0 reference. Randy showed results of two simulations including package models with either an ideal or non-ideal connection to the pre-driver supply of the Spice model. A 2-port decoupling model was necessary for good correlation in the case with the ideal connection to the pre-driver supply. A 3-port decoupling model was necessary for good correlation in the case with the non-ideal connection to the pre-driver supply. Randy concluded that a multi-port decoupling model is most versatile. Unused ports not connected to a package model should be connected to node 0, which is also the reference port for the S-parameter model.

Walter Katz noted that the Interconnect task group BIRD will fully support the addition of decoupling models such as S-parameter or Spice models. Randy was asked about his thoughts on power aware modeling in IBIS in the context of the other presentations about improved power aware modeling. Randy responded that although there are some known deficiencies with the current IBIS modeling algorithms, he saw good correlation results with most models. He noted that the decoupling model can make a large difference in obtaining good correlation, and a broadband model is really needed compared to a simple C or RC model for the on-die decoupling.

**CONCLUDING ITEMS**

Lance Wang closed the meeting by thanking the co-sponsors and the presenters as well as SPI organizers. He also thanked all the attendees for making the meeting a success. The meeting concluded at approximately 5:40 PM.

**NEXT MEETING**

The next IBIS Open Forum teleconference meeting will be held May 20, 2016. The following IBIS Open Forum teleconference meeting will be held June 10, 2016.

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**NOTES**

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This meeting was conducted in accordance with ANSI guidance.

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* To subscribe to one of the task group email lists: ibis-macro@freelists.org, ibis-interconn@freelists.org, or ibis-quality@freelists.org.
* To inquire about joining the IBIS Open Forum as a voting Member.
* To purchase a license for the IBIS parser source code.
* To report bugs or request enhancements to the free software tools: ibischk6, tschk2, icmchk1, s2ibis, s2ibis2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

<http://www.ibis.org/bugs/ibischk/>
[http://www.ibis.org/ bugs/ibischk/bugform.txt](http://www.ibis.org/%20bugs/ibischk/bugform.txt)

The BUG Report Form for tschk2 resides along with reported BUGs at:

<http://www.ibis.org/bugs/tschk/>
<http://www.ibis.org/bugs/tschk/bugform.txt>

The BUG Report Form for icmchk resides along with reported BUGs at:

<http://www.ibis.org/bugs/icmchk/>
<http://www.ibis.org/bugs/icmchk/icm_bugform.txt>

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<http://www.ibis.org/bugs/s2ibis/bugs2i.txt>
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<http://www.ibis.org/bugs/s2iplt/bugsplt.txt>

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

<http://www.ibis.org/>

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

<http://www.ibis.org/directory.html>

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**SAE STANDARDS BALLOT VOTING STATUS**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Organization** | **Interest Category** | **Standards Ballot Voting Status** | **March 18, 2016** | **April 8, 2016** | **April 29, 2016** | **May 11, 2016** |
| ANSYS | User | Active | X | X | X | - |
| Applied Simulation Technology | User | Inactive | - | - | - | - |
| Broadcom Ltd. | Producer | Inactive | - | - | - | - |
| Cadence Design Systems | User | Inactive | X | - | - | - |
| Cisco Systems | User | Inactive | - | - | - | - |
| CST | User | Inactive | - | - | - | X |
| Ericsson | Producer | Inactive | - | - | - | X |
| GLOBALFOUNDRIES | Producer | Inactive | - | X | - | - |
| Huawei Technologies | Producer | Inactive | - | - | - | - |
| Infineon Technologies AG | Producer | Inactive | - | - | - | - |
| IBM | Producer | Inactive | X | X | - | - |
| Intel Corp. | Producer | Active | X | X | X | X |
| IO Methodology | User | Active | - | - | X | X |
| Keysight Technologies | User | Active | X | X | X | X |
| Maxim Integrated Products | Producer | Inactive | X | - | - | - |
| Mentor Graphics | User | Active | X | X | X | X |
| Micron Technology | Producer | Active | X | X | - | X |
| Signal Integrity Software  | User | Active | X | X | X | X |
| Synopsys | User | Active | X | X | X | X |
| Teraspeed Labs | General Interest | Active | X | X | X | - |
| Toshiba | Producer | Inactive | - | - | - | - |
| Xilinx | Producer | Inactive | - | - | - | - |
| ZTE | User | Inactive | - | - | - | - |
| Zuken | User | Inactive | - | - | - | X |

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* Must attend two consecutive meetings to establish voting membership
* Membership dues current
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Interest categories associated with SAE standards ballot voting are:

* Users - members that utilize electronic equipment to provide services to an end user.
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