Extraction of Transient Behavioral Model of Digital I/O Buffers from IBIS

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Abstract

A method for extraction and simulation of transient behavioral models of state transition of digital I/O buffers is introduced. This scheme increases the speed of chip interconnect simulations with large number of simultaneous switching devices, while maintaining good accuracy compared to corresponding transistor level models. This paper covers the derivation procedures of such transient state transition behavioral models from IBIS modeling data. A comparison of simulation results between these models and transistor level models (SPICE models) is also included.

1. Introduction

Improvement of chip and package design technology accompanying industrial competition has resulted in the need for new descriptive models of integrated circuit drivers and receivers. These models should be nonproprietary and be capable of maintaining suitable accuracy and speed in the simulation of transmission lines and signal integrity related effects such as crosstalk and power/ground bounce (noise).

Simulation of digital I/O buffers together with their chip packages and printed circuit boards can mainly be done in two ways. The traditional approach is to use transistor level models which is useful when small scale simulations or analysis of some particular network is the objective of the simulation. On the contrary, this approach would be very time consuming for simulations of large number of buffers and their interconnections. Transistor level models may also reveal vendor's proprietary device information. As a solution to this problem, behavioral models of devices such as I/O Buffer Information Specification (IBIS) are introduced [1]. The behavioral IBIS modeling data can be derived from measurements as well as circuit simulations. Simulations with behavioral models can generally be executed faster than the corresponding simulations with transistor level models. A behavioral device model does not reveal any detailed and sensitive information about the design technology and underlying fabrication processes, so the vendor intellectual property would be protected.

The behavioral IBIS based models of a device provide the DC current vs. voltage curves along with a set of rise and fall times of the driver output voltage and packaging parasitic information of the I/O buffer [2]. It should be noted that the IBIS modeling data itself doesn't provide explicit information on driver transient state transitions. Although the extraction of the model of transient state transition of buffers is necessary and has apparently been accomplished by some investigators, no publications have appeared in the public domain on how this extraction is accomplished.

In this paper we present an efficient extraction methodology for analyzing and modeling transient state transitions of output buffers based on IBIS modeling data. The behavioral model is then integrated with circuit simulators for transient analysis when output buffers are connected to arbitrary loads.

2. General electrical model of an I/O buffer

2.1 Determination of High and Low I/V Characteristics

IBIS behavioral model presentation of a device as shown in figure 1 provides information about the I/V characteristics of the power and ground clamp diodes of the buffer, the input or output die capacitance (C_{comp}) and the characteristics of the package (the values of the lead inductance (L_{pkg}), resistance (R_{pkg}) and capacitance(C_{pkg})). IBIS modeling data also includes DC steady state I/V characteristics of the upper and lower devices and the voltage vs. time characteristics of (high-to- low) and (low-to-high) transition for a specific set of given load Z_{meas} (normally a passive resistor).

The values for upper and lower device I/V characteristics are provided in two different tables. Each table the contains the values for a maximum and a minimum I/V characteristic. The actual I/V curve must vary between these two set of I/V characteristics.

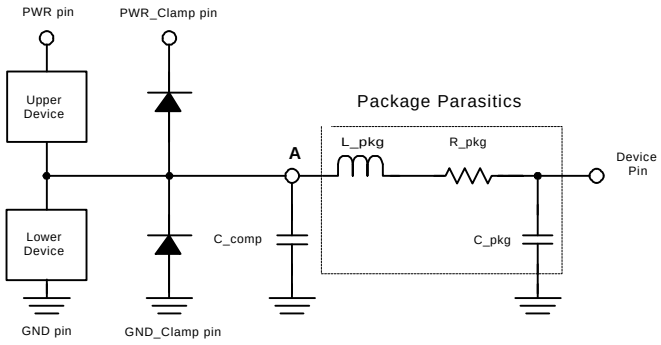

Figure 1. IBIS representation of an I/O buffer

The rise/fall voltage waveform is measured at point (A) shown in figure 1 with all package parasitics removed and the clamping diodes disconnected so the output buffer configuration changes to the one shown in figure 2. Denote the V_{meas} and I_{meas} as shown in this figure. Then I_{meas} can be expressed as:

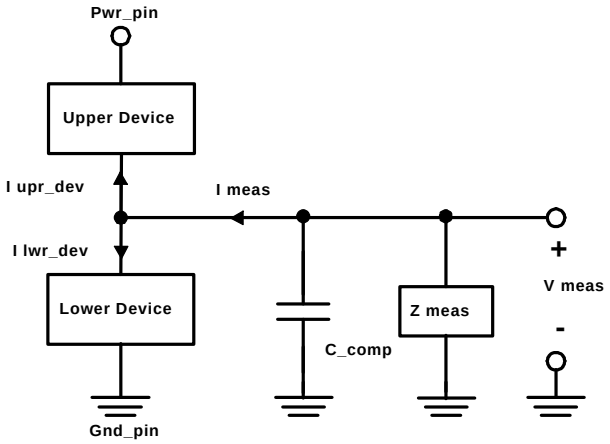

Figure 2. IBIS transition measurement circuit

$$I_{meas}(t) = -(C_{comp}\frac{d}{dt}V_{meas}(t) + \frac{1}{Z_{meas}}V_{meas}(t)) \qquad (1)$$

When a device transition occurs, after a certain time, the output I/V trajectory of this transition falls on the steady state I/V characteristics. The measurement voltage and current associated with it, calculated by equation (1), provide this transient I/V trajectory. The termination points of this trajectory identify the actual steady state I/V characteristics. This curve must be located within the range specified by the maximum and minimum values of the corresponding steady state I/V characteristics. This feature can be used to find the actual I/V characteristics that govern the output buffer behavior in the steady state. Showing the maximum and minimum values of each quantity in it's specified range by sub index max and min, an alternative way to present the actual steady state I/V characteristics for high and low state can be expressed as follows:

$$\begin{aligned} I_{high} &= \eta_1 I_{high_{max}} + (1-\eta_1) I_{high_{min}} \\ I_{low} &= \eta_2 I_{low_{max}} + (1-\eta_2) I_{low_{min}} \end{aligned} \qquad (2)$$

where parameters η_1 and η_2 are the combinative coefficients of maximum and minimum values of steady state high and low I/V characteristics, so η_1 and η_2 can be evaluated by transition termination points as:

$$\begin{aligned} \eta_1 &= \frac{I_{high_{meas}} - I_{high_{min}}(V_{meas})}{I_{high_{max}}(V_{meas}) - I_{high_{min}}(V_{meas})} \\ \eta_2 &= \frac{I_{low_{meas}} - I_{low_{min}}(V_{meas})}{I_{low_{max}}(V_{meas}) - I_{low_{min}}(V_{meas})} \end{aligned} \qquad (3)$$

variables $I_{low_{meas}}, I_{high_{meas}}$ are obtained from equation (1) and correspond to the terminating values of the device current for high-to-low and low-to high output transition. These values along with V_{meas}, identify the termination points of transition I/V trajectory.

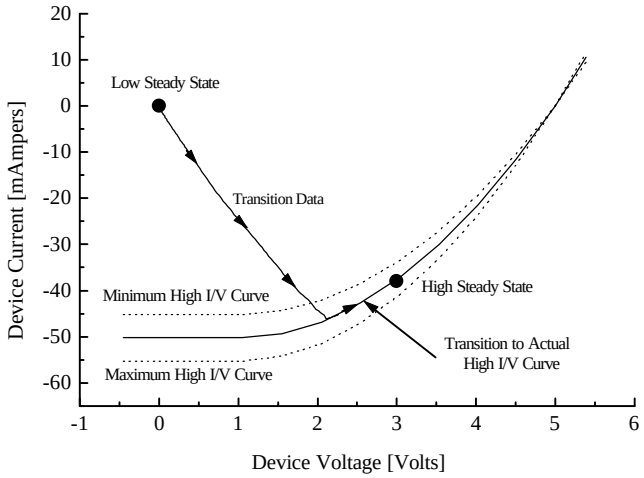

Figure 3. Determination of actual I/V characteristic

A realistic example of this scaling method for a low-to-high device transition of a buffer is presented in figure 3. This buffer is connected to a combination of capacitive and resistive load, and as it is illustrated the terminating points of the device transition I/V curve fall on the actual I/V characteristics of the buffer. By adopting this method the relationship between steady state voltage and current of a buffer can be expressed as follows:

$$I_{high} = f_h(V_{high}) \qquad I_{low} = f_l(V_{low}) \qquad (4)$$

or

$$V_{high} = g_h(I_{high}) \qquad V_{low} = g_l(I_{low}) \qquad (5)$$

Virtually the lower device doesn't operate in the high steady state., so the I/V characteristic of high state is generated only by the upper device as shown in figure 2. This means that, in either equation sets (4) and (5), the first equation provides the I/V characteristics of the buffer when it is in high steady state, and this I/V characteristic is produced by the upper device. The same reasoning shows that , the

second equation in this set provides the I/V characteristic of the buffer in low state and it is produced by the lower device.

2.2 Derivation of device transient state transition model

When a low-to-high state transition takes place, upper device of the buffer gradually turns on and it's I/V characteristic transforms to the high steady state I/V curve. Meanwhile the lower device of the buffer which was operating on the low steady state I/V curve gradually turns off and the current of the device approaches zero (figure 4-a, 4-b). This kind of transition is device dependent and not necessarily a linear function of time.

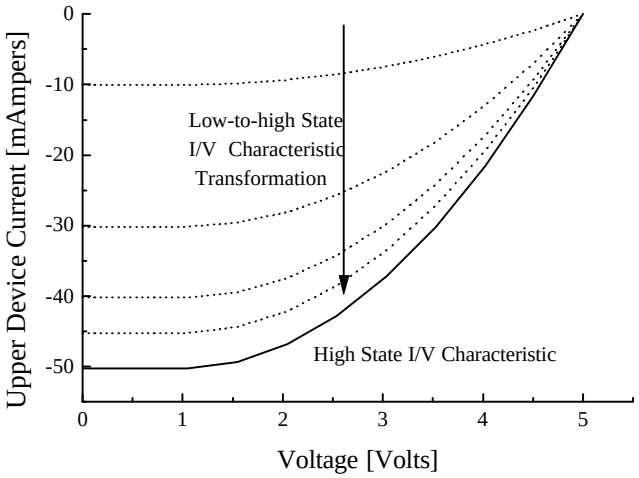

Figure 4-a. Upper Device State Characteristic Transformation

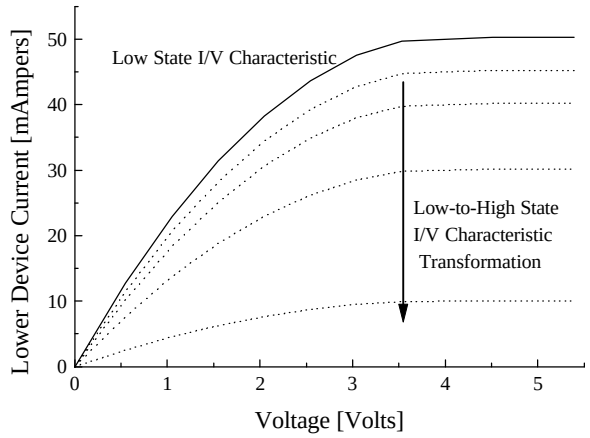

Figure 4-b. Lower Device State Characteristic Transformation

The overall transition is observed as a consistent evolution of low steady state to high steady state I/V characteristics at the buffer output (figure 5) . The same principle applies for high to low state transition.

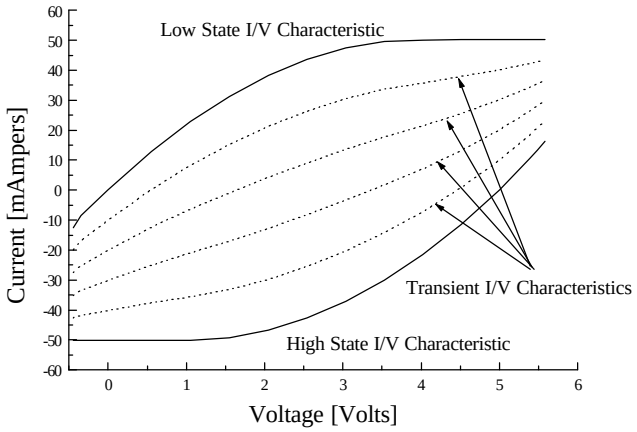

Figure 5. Device Overall Transient V/I Characteristics

Assuming this transition is related to device's DC high and low steady state static I/V characteristics, the instantaneous device currents of the buffer, shown by $I_{upr\_dev}(t)$ and $I_{lwr\_dev}(t)$ for the upper and lower device, can be expressed as:

$$\begin{aligned} I_{upr\_dev}(t) &= \alpha(t) \cdot f_h(V(t)) \\ I_{lwr\_dev}(t) &= \beta(t) \cdot f_l(V(t)) \\ I_{total}(t) &= I_{upr\_dev}(t) + I_{lwr\_dev}(t) \end{aligned} \quad (6)$$

For equation set (6), $\alpha(t)$ and $\beta(t)$ are time varying coefficients and V(t) is the buffer output voltage during the transition.

Applying this assumption along with a set of transition response for a specific known load provided in IBIS representation of a buffer , the following relationship can be obtained:

$$I_{meas}(t) = \alpha(t) \cdot f_h(V_{meas}(t)) + \beta(t) \cdot f_l(V_{meas}(t)) \quad (7)$$

Equation (7) describes transient I/V characteristics of a buffer in terms of it's steady state I/V curves. Assume coefficients α and β vary in the range of [0,1] the relation between α and β at the beginning and end of the device transition satisfies:

$$\alpha = 1 - \beta \quad (8)$$

As an example, at the beginning of the low-to-high transition, the total current is provided by the lower device, so $\alpha=0$, $\beta=1$. Likewise at the end of low-to-high transition , the total current is provided by the upper device and $\alpha=1$, $\beta=0$.

Suppose equation (8) is valid at any specific time through the device transition then the output current of the buffer can be presented by a linear combination of output currents of upper and lower devices of this buffer, so using equations (7) and (8), we can write:

$$\alpha = \lambda \qquad \beta = 1 - \lambda \tag{9}$$

and the parameter λ is calculated as:

$$\lambda(t) = \frac{I_{meas}(t) - f_l(V_{meas}(t))}{f_h(V_{meas}(t)) - f_l(V_{meas}(t))} \tag{10}$$

where the factor λ is the measure that describes the distribution of device total current between the upper and lower sections of the buffer. α and β show the proportion of significance of high and low state I/V characteristics of the buffer during the state transition.

Each set of α and β provides an instantaneous I/V curve (figure 4-a and 4-b) for the upper and the lower devices of the buffer. These curves in addition to clamping diodes associated with their power and ground voltages and the die capacitor illustrate the behavioral device model during the transition.

At a specific instant of time, the load connected to this buffer could be modeled by a thevenin equivalent circuit. The intersection of the load line obtained from this equivalent circuit with the transition I/V characteristic of the buffer would produce the transient operating point of the device. Using this operating point, corresponding points on transient high and low I/V characteristics can be obtained. IBIS modeling data provides high and low steady state I/V characteristics in discrete format. These characteristics along with α, β values for that instant produce the discrete transient I/V characteristics according the equation (6). These curves can be used as piecewise linear curves and each section can be dealt with as lumped circuits . This procedure is illustrated by figure 6.

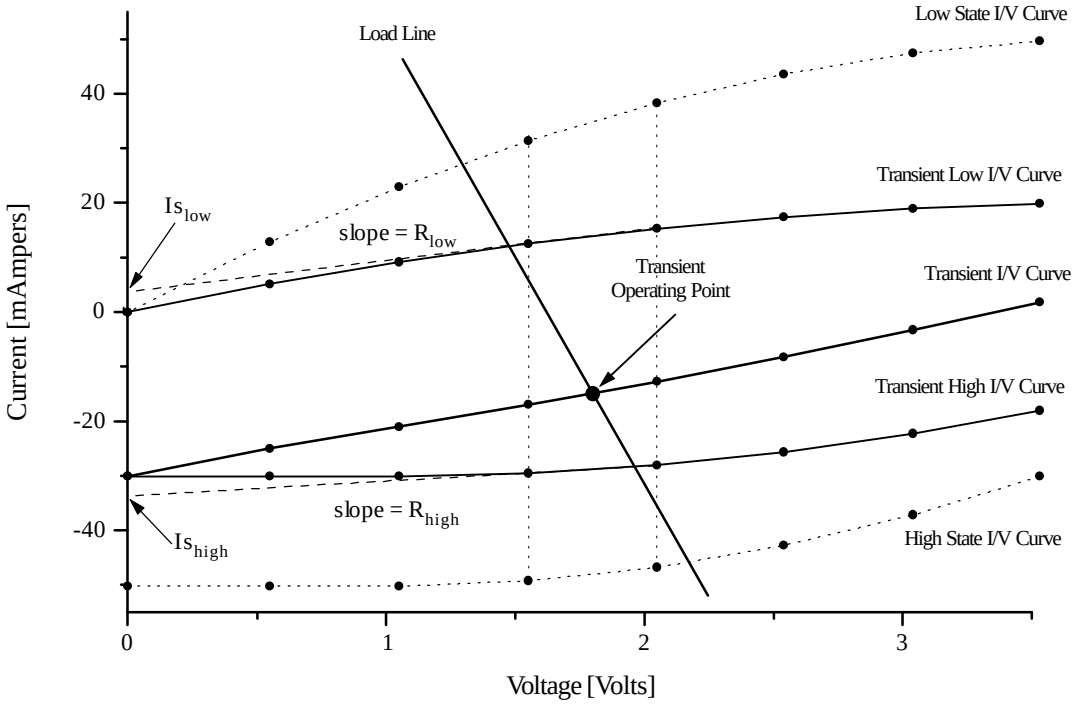

Figure 6. Discrete Transition I/V Characteristic and lumped circuit equivalent

Employing this feature the equivalent circuit model of the driver can be presented as shown in figure 7. This circuit can be solved directly using linear circuit solvers. This effect reduces the convergence problems as well as increasing the speed of non linear circuit simulations. Figure 8 shows a test configuration used to verify the results obtained by I/O buffer behavioral model simulations and figures 9 and 10 provide the voltage waveform at the output pin of a driver buffer and the input pin of a receiver buffer in comparison with SPICE results.

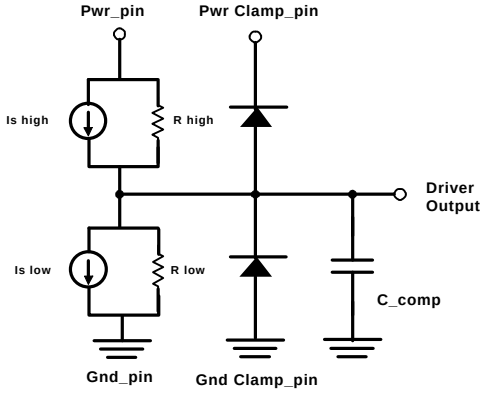

Figure 7. IBIS equivalent electrical model

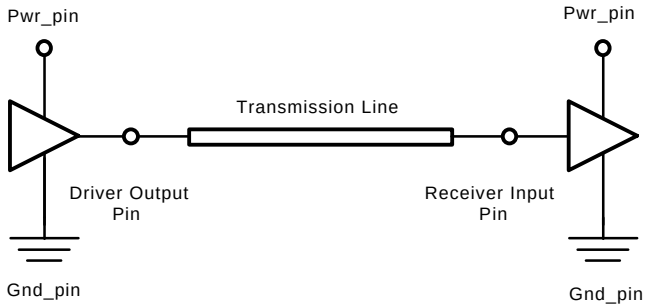

Figure 8. I/O Buffer behavioral model simulation test configuration

Although this scheme is easy to implement, it over estimates the current in the non active device during the state transition thus related circuit factors such as power/ground noise (bounce) and device input/output delays are not calculated precisely. This phenomena can be observed in figures 13 and 14, where a comparison of device currents between this behavioral model and SPICE simulations is provided.

2.3 Derivation of modified state transition model

In order to decrease the error in the calculated upper and lower device currents, two factors should be taken into account. First, state transition is device property and varies for different devices and the second that upper and lower

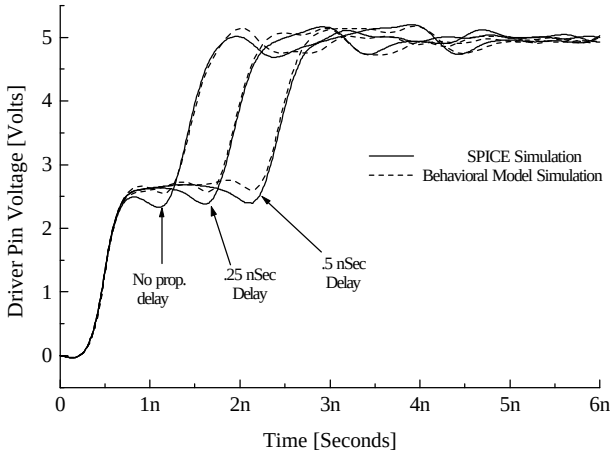

Figure 9. Driver buffer pin voltage with different propagation delays

devices do not necessarily start and end the switching process at the same period of time. These effects are illustrated in figures 13 and 14, as it can be seen from the SPICE simulations (solid lines). For a 5 nSec low-to-high buffer transition, the upper device of this buffer starts the switching with a 1.2 nSec delay with respect to the lower device and finishes it about 1.8 nSec after it.

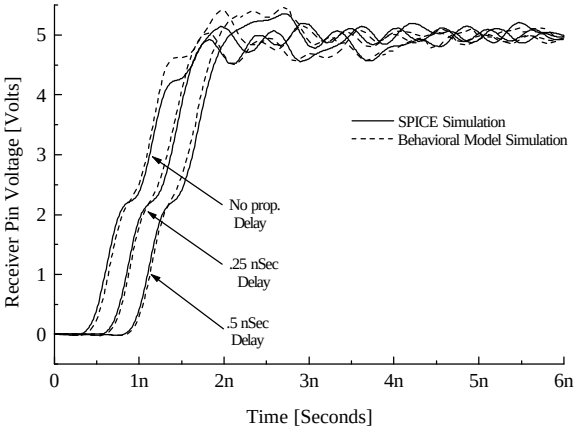

Figure 10. Receiver buffer pin voltage with different propagation delays

Considering these effects, the transition model of device state transition can be modified as follows. Assume a low-to-high buffer state transition occurs at initial time (t=0). Lower device of this buffer starts the transition process instantaneously and provides the output current of the device, meanwhile the upper device is not active. The upper device starts it's transition with the time delay t_1 with respect to initial time. After time t_1, both of the devices are active and the output current is the addition of the upper and the lower device current. At time t_2, the lower device finishes it's transition and from this time on, the output current is only

provided by the upper device of the buffer. In this manner the transition time can be divided into three sections. These sections are shown in figure 11 which displays the buffer output measurement voltage provided in IBIS modeling data.

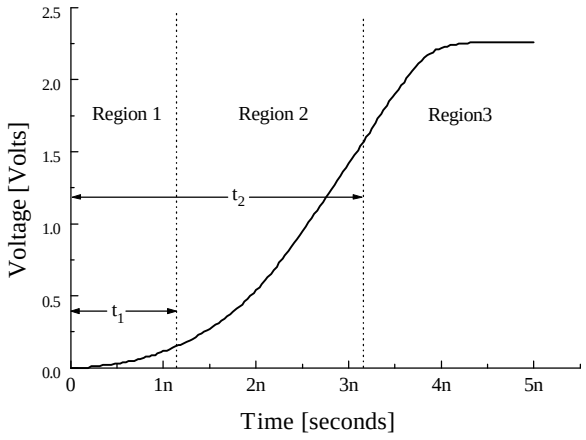

Figure 11. Buffer Output Measurement Sample

For the section ($t < t_1$) only the lower device provides the output current, so according equations (6) and (7), the transition model could be provided as:

$$\alpha(t) = 0$$
$$\beta(t) = \frac{I_{meas}(t)}{f_l(V_{meas}(t))} \tag{11}$$

in this equation set, $I_{meas}(t)$ is calculated using equation (1).

Using the same reasoning, for the last section ($t > t_2$) only the upper device provides the output current, so the transition model for this section can be:

$$\alpha(t) = \frac{I_{meas}(t)}{f_h(V_{meas}(t))}$$
$$\beta(t) = 0 \tag{12}$$

for the middle section ($t_1 < t < t_2$) equations (8) and (9) can be modified as follows:

$$\alpha_{mod} = \alpha_1 \cdot \lambda \quad , \quad \beta_{mod} = \beta_1 \cdot (1-\lambda) \tag{13}$$

Parameters α_1 and β_1 are transition adjustment factors and can be found based on the continuity condition for α and β value on the boundary of the middle region so α_1 and β_1 can be calculated as:

$$\alpha_1 = \frac{I_{meas}(t_1)}{f_h(V_{meas}(t_1))}$$
$$\beta_1 = \frac{I_{meas}(t_2)}{f_l(V_{meas}(t_2))} \tag{14}$$

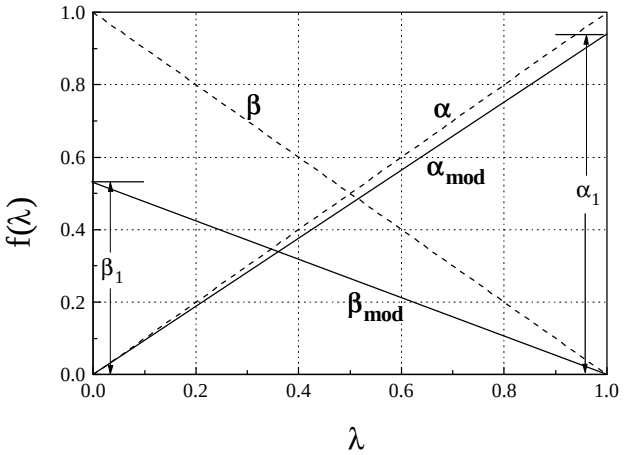

Figure 12. Modified weighting factors

Figure 12 displays this modification versus the first method and figures 13, 14 illustrates the increased accuracy of the modeling of the transient state transitions in an I/O buffer. Using equations (7) and (13) λ is calculated for this method as follows:

$$\lambda(t) = \frac{I_{meas}(t) - \beta_1 \cdot f_l(V_{meas}(t))}{\alpha_1 \cdot f_h(V_{meas}(t)) - \beta_1 \cdot f_l(V_{meas}(t))} \tag{15}$$

3. Verification

To verify the results obtained by this behavioral model, we extracted the steady state high and low current/voltage characteristics and a set of rise/fall time transient responses for a 1 nSec transition of a standard digital buffer connected to a typical load using SPICE simulations.

The buffer used for simulation purposes is a level 1 MOSFET invertor model made by a PMOS and a NMOS device. The PMOS device has a channel width of 136.4 micrometer and a surface mobility of 200 cm^2/Vs. The NMOS device has a channel width of 341.0 micrometer and a surface mobility of $500cm^2/Vs$. Both of the devices the channel length of 1.5 micrometer, oxide thickness of 2.5 micro micrometer, substrate doping of $1x10^{16}$ cm^{-3} and the threshold voltage of 1 volts.

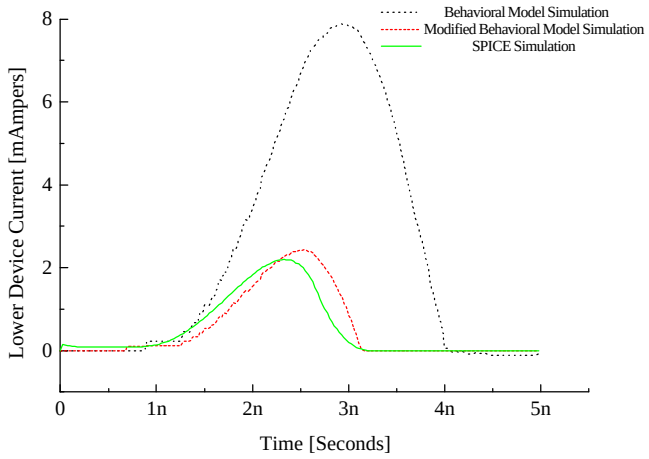

Figure 13. Comparison of I/O buffer behavioral model simulation and SPICE results for Lower Device Current during transition.

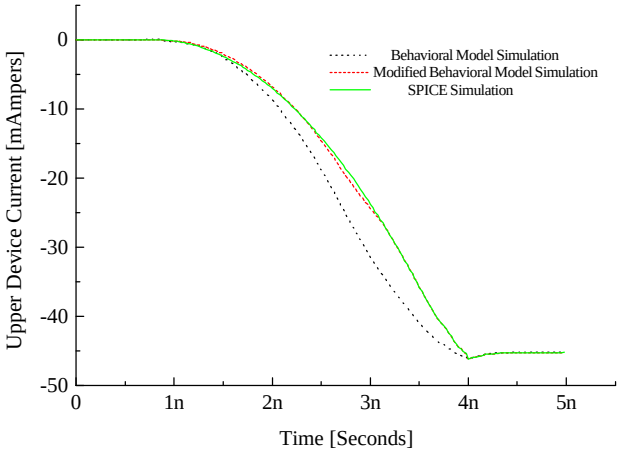

Figure 14. Comparison of I/O buffer behavioral model simulation and SPICE results for Upper Device Current during transition.

We used I/V characteristics and the transient measurement data along with our behavioral model to generate the buffer transient response for load configuration shown in figure 8. Simulations were performed with the SPICE based transistor models and our behavioral model for three cases of no propagation delay (without the transmission line), 0.25 nSec and 0.5 nSec propagation delay for the transmission line. The solid lines in figures 9 and 10 are obtained from SPICE simulations, whereas the dashed lines from I/O buffer behavioral model simulations, which are in good agreement with the SPICE simulation results. Modified transient behavioral model simulations are performed for α_1 and β_1 equal to 0.53 and 0.94 and the results are provided in figures 13 and 14.

4. Conclusion

A behavioral model of transient state transition for digital I/O buffers is introduced in this paper. This model can effectively be used in I/O buffer behavioral model simulations of high speed switching chip interconnects such as IBIS and increase the speed of these simulations.

5. Acknowledgments

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References

[1] W. Hobbs, A. Muranyi, R. Rosenbaum and D. Telian, Intel Corporation, " IBIS: I/O buffer Information Specification, Overview ", *http://www.vhdl.org*., January 14, 1994.

[2] Derrick Duehren, Will Hobbs, Arpad Muanyi, Robin Rosenbaum , Intel Corporation , "Specifying I/O Buffers with IBIS (Input / Output Buffer Information Specification)", *http://www.vhdl.org.* , September 26, 1994.

[3] Donald Telian, Intel Corporation, " Treat pc-board traces as transmission lines to specify drive buffers ", EDN, September 2, 1993, pp. 129-136.