(99):BIRD5.4 Pin Mapping for Ground Bounce Simulation

(260):GND - reserved model name, used with ground pins

(731):Description: Used to indicate the power and/or ground buses to which a given driver, receiver or terminator is connected.

(737):The second column, pulldown\_ref, designates the ground bus connections for the buffer or termination associated with that pin. The bus named under pulldown\_ref is associated with the [Pulldown] I-V table for non-ECL [Model]s. This is also the bus associated with the [GND Clamp] I-V table and the [Rgnd] model unless overridden by a label in the gnd\_clamp\_ref column.

(739):The fourth and fifth columns, gnd\_clamp\_ref and power\_clamp\_ref, contain entries, if needed, to specify additional ground bus and power bus connections for clamps. Finally, the sixth column, ext\_ref, contains entries to specify external reference supply bus connections.

(756):2 GNDBUS2 PWRBUS2 | ground, power and external

(767):11 GNDBUS1 NC | One set of ground connections.

(771):21 GNDBUS2 NC | Second set of ground connections

(777):33 NC PWRBUS1 | ground bus.

(1441):Other Notes: Power Supplies: It is intended that standard TTL and CMOS models be specified using only the [Voltage Range] keyword. However, in cases where the output characteristics of a model depend on more than a single supply and ground, or a [Pullup], [Pulldown], [POWER Clamp], or [GND Clamp] table is referenced to something other than the default supplies, use the additional “reference” keywords.

(1498):Therefore, for a 5 V model, -5 V in the table actually means 5 V above Vcc, which is +10 V with respect to ground; and 10 V means 10 V below Vcc, which is -5 V with respect to ground. Vcc-relative data is necessary to model a pullup structure properly, since the output current of a pullup structure depends on the voltage between the output and Vcc pins and not the voltage between the output and ground pins. Note that the [GND Clamp] I-V table can include quiescent input currents, or the currents of a 3-stated output, if so desired.

(1569):Description: The data points under the keyword [ISSO PD] define the effective current of the pulldown structure of a buffer as a function of the voltage on the pulldown reference node (the ground node), whereas the points under the keyword [ISSO PU] define the effective current of the pullup structure as a function of the voltage on the pullup reference node (the power node).

(1572):The [ISSO PD] table voltages are relative to the [Pulldown Reference] typ/min/max values (usually ground). The [ISSO PU] table voltages are relative to the [Pullup Reference] typ/min/max values (also usually the [Voltage Range] voltages). In the case of the [ISSO PU] table, the voltages follow the same Vtable = Vcc - Vmeasured convention as the [Pullup] table. Each of the tables are aligned with and span the typical -Vcc to Vcc voltages.

(1586):Other Notes: EDA tools can use such tables to calculate modulation coefficients to modulate the original pulldown and pullup currents when a voltage variation on the pullup and pulldown reference nodes is revealed during power and/or ground bounce, and/or SSO simulation events.

(1616):With no modulation, Ksso\_pd(0) = 1 and Ksso\_pu(0) = 1. However, if during simulation of the typical corner the Vcc voltage drops from 5.0 to 4.7, then Vtable\_pu = 5.0 - 4.7 = 0.3, and Ksso\_pu(0.3) is calculated. If at the same time the ground reference voltage at the buffer increases to 0.2 V, then Ksso\_pd(0.2) is calculated. These two modulation factors are used in the reference model calculations to account for gate modulation effects associated with both output transistors.

(1760):Internal Logic that is generally referenced to the power rail is used to set the NMOS MOSFET switch to its “On” state. Internal logic, likewise referenced to ground, is used to set the PMOS device to its “On” state if the PMOS device is present. Thus, the [Voltage Range] settings provide the assumed gate voltages. If the [POWER Clamp Reference] exists, it overrides the [Voltage Range] value. The table entries are actually Vgs values of the NMOS device and Vcc - Vgs values of the PMOS device, if present. The polarity conventions are identical with those used for other tables that are referenced to power rails. Thus, the voltage column can be viewed as a table defining the source voltages Vs according to the convention: Vtable = Vcc - Vs. This convention remains even without the NMOS device.

(1918):Figure 16 illustrates a general configuration from which a [Rising Waveform] or [Falling Waveform] is extracted. The DUT die shows all of the available power and ground pin reference voltage terminals. For many buffers, only one power pin and one common ground pin terminal are used. The absolute GND is the reference for the V\_fixture voltage and the package model equivalent network. It can also serve as a reference for C\_comp, unless C\_comp is optionally split into component attached to the other reference voltages.

(1925):Other Notes: Figure 17 documents some expected internal paths for a useful special case where only one common power pin (VDDQ) and one common ground exists (GND).

(1936):L\_GND - On-die inductance of Ground

(1937):R\_GND - On-die resistance of Ground

(1941):While the [Composite Current] already includes the buffer I\_byp current, some Series model type elements may be used to document an equivalent bypass impedance to improve simulation results. Such an equivalent impedance can be extracted on a per buffer basis, but summed and expressed as a total equivalent impedance between the power and ground pins of the component with the Series model type keywords, including [C Series], [Lc Series], [Rc Series], and [R Series] under a separate [Model]. These elements are connected using the [Series Pin Mapping] keyword. Paths between several voltage rails can be modeled in this manner. The [Pin Mapping] keyword documents what buffers share common and often isolated power rails.

(2120):Usage Rules: Each [GND Pulse Table] and [POWER Pulse Table] keyword introduces a table of voltage vs. time points that describe the shape of an offset voltage from the [GND Clamp Reference] voltage (or default ground) or the [POWER Clamp Reference] voltage (or default [Voltage Range] voltage). Note that these voltage values are inherited from the top-level model.

(2542):7 A\_gcref Voltage reference port for ground clamp structure

(2553):Under the [Model] description, power and ground reference ports are created and connected by IBIS-compliant tools as defined by the [Power Clamp Reference], [GND Clamp Reference], [Pullup Reference], [Pulldown Reference] and/or [Voltage Range] keywords. The A\_signal port is connected to the die pad, to drive or receive an analog signal.

(2567):Figure 21 illustrates the use of [External Circuit]. Buffer A is an instance of [External Circuit] “X”. Similarly, Buffer B is an instance of [External Circuit] “Z”. These instances are created through [Circuit Call]s. [External Circuit] “Y” defines an on-die interconnect circuit. Nodes “a” through “e” and nodes “f” through “j” are specific instances of the ports defined for [External Circuit]s “X” and “Z”. These ports become the internal nodes of the die and must be explicitly declared with the [Node Declarations] keyword. The “On-die Interconnect” [Circuit Call] creates an instance of the [External Circuit] “Y” and connects the instance with the appropriate power, signal, and ground die pads. The “A” and “B” [Circuit Call]s connect the individual ports of each buffer instance to the “On-die Interconnect” [Circuit Call].

(2674):The vlow and vhigh entries accept analog voltage values which must correspond to the digital off and on states, where the vhigh value must be greater than the vlow value. When polarity is Non-Inverting, vlow corresponds to the digital off state '0', vhigh corresponds to the digital on state '1', trise corresponds to the analog edge rate going from the digital off to on state, and tfall corresponds to the analog edge rate going from the digital on to off state. When polarity is Inverting, the analog behavior corresponds to the opposite digital states. For example, a 3.3 V ground-referenced buffer would list vlow as 0 V and vhigh as 3.3 V. For a Non-Inverting D\_to\_A converter, a rising edge in D\_drive would result in a transition from 0 V to 3.3 V, and for an Inverting D\_to\_A converter, a rising edge in D\_drive would result in a transition from 3.3 V to 0 V. The trise and tfall entries are times, must be positive, and define input ramp rise and fall times between 0 and 100 percent.

(3249):The vlow and vhigh entries accept voltage values which correspond to fully-off and fully-on states, where the vhigh value must be greater than the vlow value. When polarity is Non-Inverting, vlow corresponds to the digital off state '0', vhigh corresponds to the digital on state '1', trise corresponds to the analog edge rate going from the digital off to on state, and tfall corresponds to the analog edge rate going from the digital on to off state. When polarity is Inverting, the analog behavior corresponds to the opposite digital states. For example, a 3.3 V ground-referenced buffer would list vlow as 0 V and vhigh as 3.3 V. For a Non-Inverting D\_to\_A converter, a rising edge in D\_drive would result in a transition from 0 V to 3.3 V, and for an Inverting D\_to\_A converter, a rising edge in D\_drive would result in a transition from 3.3 V to 0 V. The trise and tfall entries are times, must be positive and define input ramp rise and fall times between 0 and 100 percent.

(3795):However, if power/ground buses are defined by the [Pin Mapping] keyword of a component, the following rules apply to the power/ground pins. If the name of one or more power/ground pin from the power/ground bus defined by the [Pin Mapping] keyword appears under the [Pin Numbers] keyword, then the model data of those pins which are members of the same bus but are not listed under the [Pin Numbers] keyword are assumed to be merged into the model data of the pin(s) which are listed. Consequently, pins which are not listed under the [Pin Numbers] keyword shall NOT be simulated with their corresponding RLC values from the [Pin] or the [Package] keywords. Instead, all unlisted pins whose corresponding pads are members of the bus defined by the [Pin Mapping] keyword shall be shorted to the first pin of the same bus that is listed under the [Pin Numbers] keyword. This mechanism supports merged power/ground pin package modeling without additional keywords. Since the [Merged Pins] keyword (defined below) provides a mechanism to explicitly and unambiguously define the connectivity of merged pins with greater detail and freedom, the use of the [Merged Pins] keyword is strongly recommended for new models in which merged pin modeling exists.

(3796):If none of the power/ground pins of a bus defined in the [Pin Mapping] keyword appears under the [Pin Numbers] keyword, the EDA tool is expected to use the RLC values from the [Pin] or [Package] keywords according to the hierarchy rules stated under the [Package] keyword.Subparameters:

(3851):Description: When the [Pin Mapping] keyword defines power/ground buses that span over multiple power/ground pins (i.e., pads), the package parasitics of one or more groups of power/ground pins may be merged into one or more single pin representations. The [Merged Pins] keyword declares the package model for the pin whose name follows the [Merged Pin] keyword as a merged package model and lists the names of the pins whose package parasitics have been merged into this merged package model.

(3852):Usage Rules: This keyword may optionally be used when the [Model Data] keyword is present in the [Define Package Model] section. When used, it must be placed after the end of the pin list defined by the [Pin Numbers] keyword and before the [Model Data] keyword. The keyword must be followed by one pin name (the merging pin) on the same line on which the keyword appears, separated by at least one white space. This pin name must be listed under the [Pin Numbers] keyword, it must be listed as a POWER or GND pin under the [Pin] keyword and it must also be a member of a power or ground bus defined by the [Pin Mapping] keyword. This is the pin whose package model contains the merged package model data for a group of power or ground pins.

(3854):Each pin name in the list of merged pins must match the name of a POWER or GND pin in the [Pin] keyword and must also be a member of the same power or ground bus as the merging pin (pin name that follows the [Merged Pins] keyword). Pin names in this list must not be present in the pin list under the [Pin Numbers] keyword. The list must include the names of all those pins which are to be connected to the merging pin that follows the [Merged Pins] keyword due to merged modeling. No pin name may appear more than once under all [Merged Pins] keywords.

(3856):Other Notes: Note that power integrity (PI) analysis including the package parasitics on power and ground nets is not possible with Components which do not contain power/ground bus definitions using the [Pin Mapping] keyword together with the [Define Package Model] keyword, because key pieces of information on how power is distributed between the power and ground pins and the power terminals of buffer [Model]s are not available for the EDA tool. For PI analysis, at least one power/ground pin should be included in [Pin Numbers] from each power/ground bus defined in [Pin Mapping] for a given signal pin’s buffer. If no power/ground pins are defined, ideal power/ground connections based on the [Voltage Range] and/or the [\* Reference] keywords can be assumed. However, there is insufficient information for PI analysis.

(4171):Description: Tells the parser the pin names of the user accessible pins. It also informs the parser which pins are connected to power and ground.

(4173):Usage Rules: Following the [Pin List] keyword are two columns. The first column lists the pin name while the second lists the data book name of the signal connected to that pin. There must be as many pin\_name/signal\_name rows as there are pins given by the preceding [Number Of Pins] keyword. Pin names must be the alphanumeric external pin names of the part. The pin names cannot exceed eight characters in length. Any pin associated with a signal name that begins with “GND” or “POWER” will be interpreted as connecting to the boards ground or power plane. In addition, NC is a legal signal name and indicates that the Pin is a “no connect”. As per the IBIS standard “GND,” “POWER,” and “NC” are case insensitive.

(4204):The Len, L, R, and C subparameters specify the length, the series inductance, resistance, and the capacitance to ground of each section in a path description.

(4207):C The capacitance to ground of a section, in terms of farads/unit length.

(4446):c. A 500 ohm termination to the ground clamp reference voltage for TTgnd extraction and to the power clamp reference voltage for TTpower extraction (to provide a convenient, minimum loading 450 ohm - 50 ohm divider for high-speed sampling equipment observation of the component denoted as the device under test), and

(4452):The TTgnd extraction will be done only if a [GND Clamp] table exists. A high to low transition that produces a positive “glitch,” perhaps several nanoseconds later, indicates a stored charge in the ground clamp circuit. The test circuit is simulated using the complete IBIS model with C\_comp and the Ct model defined under the [TTgnd] and [TTpower] keywords. An effective TTgnd value that produces a “glitch” with the same delay is extracted.

(6819):C\_Heatsink\_Float and C\_Heatsink\_Gnd define the heatsink capacitance and connection conditions. C\_Heatsink\_Float indicates that the heatsink is floating, and C\_Heatsink\_Gnd indicates that the heatsink is grounded.