**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER:** 189.6

**ISSUE TITLE:** *Interconnect Modeling Using IBIS-ISS and Touchstone*

**REQUESTOR:**  Walter Katz, Signal Integrity Software (SiSoft); Radek Biernacki, Keysight Technologies; Justin Butterfield, Micron Technology; Curtis Clark, ANSYS; Mike LaBonte, Signal Integrity Software (SiSoft); Arpad Muranyi, Mentor Graphics; Michael Mirmak, Intel Corp.; Bob Ross, Teraspeed Labs; Randy Wolff, Micron Technology

**DATE SUBMITTED:** January 27, 2017

**DATE REVISED:** March 29, 2017; April 19, 2017; April 26, 2017; June 22, 2017;

 April 25, 2018; May 16, 2018

**DATE ACCEPTED:**

**STATEMENT OF THE ISSUE:**

This BIRD enhances IBIS with interconnect modeling features to support broadband, coupled package, and on-die interconnect using IBIS-ISS and Touchstone data.

The BIRD also adds a keyword for buffer rail mapping, to link to new terminal definitions defined for buffers.

**ANALYSIS PATH/DATA THAT LED TO SPECIFICATION:**

This BIRD has resulted from several years of discussion regarding the need for more flexible description of interconnects in IBIS. It was decided to avoid a keyword-based approach, in favor of a circuit language approach. IBIS-ISS was developed for this purpose, and a means to instantiate IBIS-ISS models from IBIS became the logical next step.

**SOLUTION REQUIREMENTS:**

The IBIS specification must meet these requirements:

Table 1: Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| 1. The model maker must be able to provide interconnect models representing die and package, using a combination of IBIS-ISS and Touchstone formats.
 | Might replace BIRD 125.1 |
| 1. Touchstone models without an IBIS-ISS wrapper circuit must be supported.
 | Might replace BIRD 158.1 |
| 1. An interconnect model may connect buffers to pins directly or separate models may be used for the buffer to pad and pad to pin connections (die and package portions).
 | Die is buffer to pad. Package is pad to pin. |
| 1. An interconnect model may connect one pin or any combination of pins on one [Component].
 | Coupled models are supported. |
| 1. The buffer I/O, pad, and pin terminals associated with I/O pins must be assignable to interconnect model terminals directly by pin name.
 |  |
| 1. The buffer supply, pad, and pin terminals associated with POWER and GND rail pins must be assignable to interconnect model terminals directly by pin name, or indirectly by [Pin] signal\_name or [Pin Mapping] bus\_label.
 |  |
| 1. The model maker must be able to provide alternative interconnect models for any given set of pins.
 | For example for a given pin pair it must be possible to provide both coupled and uncoupled models, high and low bandwidth models, or both IBIS-ISS and Touchstone models. |
| 1. The model maker may use new interconnect models for some pins and legacy package models for other pins.
 | Legacy Package Models are “Package models defined in IBIS 6.1”. |
| 1. The model user must be able, given a pin or set of pins it must analyze, to locate all interconnect models that include the pin(s), if any.
 | Simulation netlisting begins with a list of pins that must be simulated. |
| 1. The model user must be able to determine all of the pins that a given interconnect model includes.
 | Once a model is chosen, it may add more pins to the simulation. |
| 1. The model user must be able to determine how to terminate any terminals of an interconnect model not necessary for a particular analysis.
 | May need to handle s-parameter and circuit models differently. |
| 1. For any pin having an interconnect model, models encompassing the full path from buffer to pin must be present and identifiable by the user.
 | The full path may be described using BIRD 189 Buffer to Pad models and Legacy Pad to Pin Models. |
| 1. The model user must have useful information needed to make the choice between alternative interconnect models that differ only in characteristics other than the model format and the set of pins included.
 | For example: coupled/uncoupled, low/high bandwidth. This will be used to choose which alternative model set to use. |
| 1. The order of precedence for new interconnect models and legacy forms of package models must be specified.
 | Probably will take precedence over [Package Model], [Pin] RLC, and [Package]. |
| 1. The model user must be informed which pins of an interconnect model have been modeled with coupling to other pins, sufficient for the former to represent the victim pins and the latter all of the aggressor pins in a crosstalk simulation.
 | Pins near one “end” of the model will be coupled to pins on one side but probably not enough pins on the other side. |

**BACKGROUND INFORMATION/HISTORY:**

This BIRD was originally submitted to the IBIS Interconnect Task Group by Walter Katz in April, 2014. Subsequent revisions were created and reviewed in the Interconnect Task Group with contributions from Radek Biernacki, Justin Butterfield, Curtis Clark, Mike LaBonte, Arpad Muranyi, Michael Mirmak, Bob Ross, and Randy Wolff.

Parameter is shortened to Param (.param is legal in IBIS-ISS) to differentiate it further from Parameters in the multi-lingual syntax (Parameter has several meanings in IBIS and the Algorithmic Modeling Interface.)

File\_names are not quoted, to be consistent with Corner in the multi-lingual syntax. Multiple file names for corners are not supported here, however.

Entries for strings in Param are surrounded by double quotes to be consistent with string\_literal Parameters in the multi-lingual syntax (or where the AMI string\_literal parameter surrounded by double quotes is passed into the multi-lingual Parameters reference). The EDA tool needs to convert string\_literals into the parameter string syntax in IBIS-ISS.

Interaction of Param entries was not discussed. For example, for a transmission line, TD and Z0 could each have max and min entries, but the EDA tool could make available combinations of min/min, min/max, max/min or max/max for any corner. Due to parameter interactions, some mixing of corner combinations might not be realistic. (E.g., Z0min or Z0max might not correlate with TDmin or TDmax values, where TDmin=sqrt(LminCmin), Z0min=sqrt(Lmin/Cmax), etc.).

How corners of File\_IBIS-ISS and Params are processed might be based on vendor supplied documentation. For example, some, but not all, combinations are shown below:

1. One file\_name for all corners, one .subckt name, and all corner settings controlled by Param settings
2. One file\_name, three .subckts (with internal default .param settings), additional corner settings controlled by Param settings or Param is not used
3. Three file\_names with the same .subckt name, but with distinct default .param settings, additional settings controlled by Param settings or Param is not used
4. Three file\_names with three distinct .subckt name and with distinct default .param settings, additional corner settings controlled by Param settings or Param is not used

No interpretation is given for Param typ, min, and max values. It is possible to independently use typ, min, or max values for any of the Param names that have been defined (e.g., the max value of one parameter may be used with the min value of another parameter).

Some concern has been noted that EDA tools may not be able to clearly define a complete interconnect path from separate Interconnect Models that specify only part of the electrical path. While several methods to do this are possible, an example flow for an EDA tool to assemble a complete interconnect path from separate Interconnect Models is as follows:

The suggested example flow outlined below and sentence following it may no longer be relevant due to some additions and changes in BIRD189:

1. Read in the list of I/O buffers; this must contain:
	1. Pin\_I/O nodes
	2. Buffer\_I/O nodes
	3. Buffer\_Rail nodes; this also defines the respective rail attributes, including:
		1. Signal\_names
		2. Bus\_labels
		3. Rail pin\_names
2. Search models to find the smallest number of models that contain all Buffer\_I/O (this is List A)
	1. If List A contains all Pin\_I/O then
		1. Done with I/O
	2. Else search models to find the smallest number of models that contain the Pad\_I/O and Pin\_I/O that are missing in List A (this is List B)
3. If a power delivery network model is required
	1. If the models in List A and List B have connections to all Buffer\_Rail terminals and pins for each of the signal names in the Buffer\_Rail list, then
		1. Done with PDN
	2. Else search models that contain the Pad\_Rail and Pin\_Rail that are missing in List A and List B (this is List C)
4. Verify that no pin or buffer terminal is connected to two or more models
5. Verify that all pin and buffer I/O terminals are connected to a single interconnect model terminal
6. If a power delivery network is defined, then
	1. Verify that all Buffer\_Rail terminals are connected to a single interconnect model terminal
	2. Verify that there is at least one Pin\_Rail terminal with a signal\_name defined in 3.a

The user may direct the EDA tool to use models from the interconnect model sets in an interconnect model group

BIRD189 was submitted to the IBIS Open Forum January 27, 2017.

BIRD189.1 was created to correct several minor editorial issues, to clarify Unused\_port\_termination rules and the meaning of Aggressor\_Only, to remove a figure, and to update three other figures for clarity.

BIRD189.2 was created to update the list of authors, to correct the capitalization of “Aggressor\_Only”, to selectively change “IO” to “I/O”, and to change “Buf\_I/O” to “Buffer\_I/O” and “Buf\_Rail” to “Buffer\_Rail” (with appropriate re-formatting for the longer strings) to better match usage elsewhere in IBIS. A clarification of the meaning of “I/O” in the context of terminals was also added.

BIRD189.3 was created to correct a Param example, and to change “filename” to “base name” in the .ims file rules, for consistency with BIRD186.

BIRD189.4 was created to update the file name rules for compliance with the new terminology defined in BIRD186.3. Minor editorial corrections were made. A comment line was added under the [Interconnect Model Set Selector] keyword.

BIRD189.5 contains a number of updates based on a review by Arpad Muranyi, sent July 4, 2017, and several Interconnect Task group reviews. The 60 character limit for [Description] is removed for both [Interconnect Model Set] and [Define Package Model].

[Interconnect Model Set Selector] is replaced with [Interconnect Model Group]s. Unused\_port\_termination leaves the termination to EDA tools.

The Unused\_port\_termination subparameter is restored with options Open, Reference, and Resistance. Rigid rules are established related to Unused\_port termination usage.

Terminal\_type A\_gnd is added to connect a terminal to simulator global reference node A\_gnd.

More statements are given to show how bus\_label names can be entered with any or all of the [Pin Mapping], [Pin], [Bus Label] and [Die Supply Pads] keywords

BIRD189.6 adds rail relaxation rules.

**PROPOSED CHANGES:**

**In Page 94 replace:**

|  |  |  |
| --- | --- | --- |
| 11 | A\_gnd | Global reference voltage port |

**with**

|  |  |  |
| --- | --- | --- |
| 11 | A\_gnd | Simulator global reference node  |

**In Page 94 replace:**

A\_gnd is a universal reference node, similar to SPICE ideal node “0.”

**with**

A\_gnd is a simulator global reference node, similar to SPICE ideal node “0.”

The following keyword should be added to Chapter 5, COMPONENT DESCRIPTION, after the [Alternate Package Models] keyword:

*Keyword:* [Interconnect Model Group]

*Required:* No

*Description:*  [Interconnect Model Group] has a single argument, which is the name of the associated Interconnect Model Group. The length of the Interconnect Model Group name shall not exceed 40 characters in length. Blank characters are not allowed. The [Interconnect Model Group]/[End Interconnect Model Group] keyword pair is hierarchically scoped by the [Component~~]~~ keyword. The [Interconnect Model Group] keyword is used to define a list of [Interconnect Model Set]s by name that shall be used together to define Interconnect Models to be used in a simulation. A simulation may contain Interconnect Models from the Interconnect Model Sets listed in only one Group.

*Usage Rules:* [Component] may contain zero or more [Interconnect Model Group] keywords (identified by a name). Each [Interconnect Model Group] must contain at least one [Interconnect Model Set] name. Interconnect Model Sets contain Interconnect Models used to describe pin, die pad or buffer terminal connections to IBIS-ISS subcircuits or Touchstone files.

Interconnect Model Sets that exist for the component shall be listed in one or more Interconnect Model Groups. An Interconnect Model Group is required even if it references only one Interconnect Model Set. If there are no Interconnect Model Sets, the [Interconnect Model Group] keyword is illegal

The section under the [Interconnect Model Group] keyword shall have two entries per line, with each line identifying one Interconnect Model Set associated with the component. The entries shall be separated by at least one white space. The first entry lists the Interconnect Model Set name (up to 40 characters long). The second entry is the file reference of the file containing the Interconnect Model Set and shall have the extension “ims”. This file reference shall conform to the rules given in Section 3, ‘GENERAL SYNTAX RULES AND GUIDELINES’. If the Interconnect Model Set is in the same IBIS file as [Component], then the second entry shall be “NA”.

The files containing the Interconnect Model Sets with the ims extension shall be located in the same directory as the .ibs file or in a specified directory under the .ibs file as determined by the directory path according to the file name rules given in Section 3, ’GENERAL SYNTAX RULES AND GUIDELINES’ (i.e., a file reference containing a relative path to a directory below that of the referencing .ibs file is permitted). An [Interconnect Model Set] with matching name shall be found in the stated location for each Interconnect Model Set named in the [Interconnect Model Group].

Each Interconnect Model Set name and its file\_reference may only appear once under each [Interconnect Model Group] keyword for a given component.

As discussed in Section XXX, three interface locations exist: pin, die pad, and buffer. These interfaces are identified in the terminal lines under the [Interconnect Model] keyword and by their Terminal\_type column entries (shown in Table 41) as follows:

pin: Pin\_I/O, Pin\_Rail, A\_gnd

die pad: Pad\_I/O, Pad\_Rail, A\_gnd

buffer: Buffer\_I/O, Buffer\_Rail, Pullup\_ref, Pulldown\_ref, Power\_clamp\_ref, Gnd\_clamp\_ref, Ext\_ref, A\_gnd

A\_gnd is the simulator global reference node of the Interconnect Model.

Identifiers associated with these Termimal\_type \*\_I/Os are pin\_name entries. In addition, some \*\_I/O terminals may have the optional Aggressor\_Only column. If any \*\_I/O pin is marked as Aggressor\_Only, then all \*\_I/O pins with the same pin\_name entry shall be considered as Aggressor\_Only. Any \*\_I/O Terminal\_type without the Aggressor\_Only column may be considered as an aggressor or a victim.

The remaining terminals are used for POWER or GND and are referred to as “rails”. The rail identifiers are pin\_name, signal\_name, bus\_label (described below) and pad\_name entries (described below) according the allowable association rules summarized in Section XXX (Connecting Pins, Pads and Buffer Terminals) and Table 41.

An Interconnect Model Group contains of a list of Interconnect Model Sets which in turn contains a list of Interconnect Models. There are a number of rules that apply to this combined list of Interconnect Models in an Interconnect Model Group.

* I/O pin\_name rules
	+ I/O terminals use pin\_name identifiers
	+ All \*\_I/O pin\_names may omit the Aggressor\_Only column (may be aggressors or victims)
	+ No I/O pin\_name in a component may appear as a Pin\_I/O terminal without the Aggressor\_Only column in more than one Interconnect Model in the Interconnect Model Group.
	+ No I/O pin\_name in a component may appear as a Buffer\_I/O terminal without the Aggressor\_Only column in more than one Interconnect Model in the Interconnect Model Group.
	+ An I/O pin\_name may appear in Interconnect Models with the following interface combinations:
		- pin to buffer
		- pin to die pad (in one Interconnect Model) and die pad to buffer (in another Interconnect Model)
		- pin to die pad
		- die pad to buffer
	+ A \*\_I/O pin\_name may not appear in Interconnect Models of Interconnect Model Sets that are listed in one Interconnect Model Group with the following interface combinations:
		- pin to buffer (in one Interconnect Model) and pin to die pad (in another Interconnect Model)
		- pin to buffer (in one Interconnect Model) and die pad to buffer (in another Interconnect Model)
		- pin to buffer and pin to die pad and die pad to buffer in three separate Interconnect Models
* General description of rail terminals
	+ At the pin interface, a terminal whose Terminal\_type is Pin\_Rail can be identified by a pin\_name, signal\_name or bus\_label entry. A pin\_name maps directly into a Pin\_Rail pin\_name entry or the pin\_name can be mapped into a bus\_label or a signal\_name with the information given in the [Pin] keyword or by the [Pin Mapping], [Bus Label], or [Die Supply Pads] keywords described later in this section.
		- Note that a terminal whose Terminal\_type is Pin\_Rail may be associated with one pin\_name or a list of pin\_names on a rail that is associated with a signal\_name or bus\_label. If the terminal is associated with more than one pin\_name then these pin\_names are shorted together.
	+ At a die pad interface, a terminal whose Terminal\_type is Pad\_Rail can be identified by a pad\_name, signal\_name or bus\_label entry. Connections between die pad interfaces in different Interconnect models can be made by using identical pad\_names or identifying a common bus\_label or signal\_name that is available in the [Pin], [Pin Mapping], [Die Supply Pads], or [Bus Label] keywords.
		- Note that a terminal whose Terminal\_type is Pad\_Rail may be associated with one pad\_name or a list of pad\_names on a rail that is associated with a single signal\_name or bus\_label. If the terminal is associated with more than one pad\_name then these pad\_names are shorted together.
	+ At the buffer interface, a terminal whose Terminal\_type is Pullup\_ref, Pulldown\_ref, Power\_clamp\_ref, Gnd\_clamp\_ref, Ext\_ref or Buffer\_Rail can be identified by a signal\_name or bus\_label entry, or directly by the \*\_ref entries that are associated with Buffer\_I/O pin\_names.
		- Note that a terminal whose Terminal\_type is Pullup\_ref, Pulldown\_ref, Power\_clamp\_ref, Gnd\_clamp\_ref, Ext\_ref or Buffer\_Rail may be associated with one buffer terminal or a list of buffer terminals on a rail that is associated with a single signal\_name or bus\_label. If it is associated with more than one buffer terminals then these buffer terminals are shorted together.
	+ A Power Delivery Network (PDN) has one or more connections of rail terminals between Pin and Buffer, Pin and Pad or Pad and Buffer.
	+ An Interconnect Model with only rail terminals and two interfaces (no I/O terminals) can be used for a PDN.
	+ An Interconnect Model with only rail terminals (no I/O terminals) and only one interface is permitted for applications such as for modeling rail decoupling circuits.
	+ A PDN structure can also exist in an Interconnect Model with I/O terminals.
	+ Also, rail terminals or A\_gnd can be used in Interconnect Models to provide a reference node for the electrical interconnections associated with \*\_I/O terminals.
* Rail terminal rules
	+ At the pin interface, a rail pin\_name may appear on a terminal line whose Terminal\_type is Pin\_Rail in multiple Interconnect Models in the Interconnect Model Group.
	+ At the buffer interface, a rail pin\_name may appear on a terminal line whose Terminal\_type is Pullup\_ref, Pulldown\_ref, Power\_clamp\_ref, Gnd\_clamp\_ref, Ext\_ref or as a Buffer\_Rail in more than one power delivery Interconnect Model in the Interconnect Model Group.
	+ A rail terminal may be in Interconnect Models with the following interface combinations:
		- pin to buffer
		- pin to die pad (in one Interconnect Model) and die pad to buffer (in another Interconnect Model)
		- pin to die pad
		- die pad to buffer
		- pin only
		- die pad only
		- buffer only
	+ A rail terminal may not be in Interconnect Models with the following interface combinations:
		- pin to buffer (in one Interconnect Model) and pin to die pad (in another Interconnect Model)
		- pin to buffer (in one Interconnect Model) and die pad to buffer (in another Interconnect Model)
		- pin to buffer, pin to die pad, and die pad to buffer in three separate Interconnect Models

Note that these rules apply to the complete list of Interconnect Models that are included in each Interconnect Model Group, regardless of which Interconnect Model Sets contain the Interconnect Models.

All Interconnect Models without I/O terminals, but with only rail terminals are available for simulations.

If an \*\_I/O pin\_name appears on terminal lines of Interconnect Model(s) in the Interconnect Model Group with the interface combinations: pin to buffer, or pin to die pad and die pad to buffer, then the Interconnect Model(s) in the Interconnect Model Group define the full interconnect electrical path between the pin and buffer interfaces. If this is not the case then:

* If an \*\_I/O pin\_name appears only in a pin to die pad Interconnect Model in the Interconnect Model Group, then the \*\_I/O pin\_name electrical path from the die pad to buffer shall be shorted.
* If an \*\_I/O pin\_name appears only in a buffer to die pad Interconnect Model in the Interconnect Model Group, then the \*\_I/O pin\_name electrical path from die pad to buffer shall be connected using any other existing package model in this document including those under [Package] R\_pkg, L\_pkg, and C\_pkg entries; [Pin] R\_pin, L\_pin, and C\_pin entries in this section; or entries under the [Define Package Model] keyword described in Section 7. Note, if several [Define Package Model] keywords exist, the EDA tool may have to select which on one to use. EDA tools may provide the option to ignore any of the other package model formats and to use shorted paths instead.
* If an \*\_I/O pin\_name does not appear on a terminal line in any Interconnect Model in an Interconnect Model Group, then the EDA tool should use any other existing package model in this document.

If a PDN structure has terminals in an Interconnect Model(s) in the Interconnect Model Group with the interface combinations: pin to buffer, or pin to die pad and die pad to buffer, then the Interconnect Model(s) in the Interconnect Model Group define the full PDN electrical path between the pin and buffer interfaces. If this is not the case then:

* If rail terminals describe a PDN structure with only a pin to die pad Interconnect Model in the Interconnect Model Group, then the rail electrical path from the die pad to buffer shall be shorted. Note, the shorted connections from the die pad terminal names to the buffer interface rail terminal names might require using the information under the [Pin], [Pin Mapping], [Die Supply Pads] or [Bus Label] keywords in this section.
* If rail terminals describe a PDN structure with only a buffer to die pad Interconnect Model in the Interconnect Model Group, then the rail electrical path from die pad to Pin\_Rail pin\_name entry shall be connected using any other existing package model in this document including those with [Package] R\_pkg, L\_pkg, and C\_pkg entries or [Pin] R\_pin, L\_pin, and C\_pin entries in this section; or entries under the [Define Package Model] keyword described in Section 7. Note, if several [Define Package Model] keywords exist, the EDA tool may have to select which on one to use. Also note, the Pad\_Rail terminals have pad\_name bus\_label, or signal\_name entries that may short the electrical connections at the die pad interface based on the information under the [Pin], [Pin Mapping], [Die Supply Pads] or [Bus Label] keywords in this section. If there are more rail pad\_names than Pin\_Rail pin\_names, the EDA tool will have to short some pad\_names to support existing package model formats.
* If there are no rail terminal names on a terminal line in any Interconnect Model in an Interconnect Model Group, then the EDA tool should use any other existing package model in this document, or ideal sources if the simulation does not need to include PDN effects.

*Examples:*

| Some [Interconnect Model Set] names used in Examples from Section 12 are

| referenced below:

|

| Example 1

|

[Interconnect Model Group] Full\_ISS\_PDN\_1

| Interconnect Model Set file\_reference

Full\_ISS\_PDN\_1 NA | The [Interconnect Model Set] is

 | present in the .ibs file for

 | all pins

[End Interconnect Model Group]

|

| Example 2

|

[Interconnect Model Group] Full\_ISS\_PDN\_sn\_2

| Interconnect Model Set file\_reference

Full\_ISS\_PDN\_sn\_2 NA | The [Interconnect Model Set] is

 | present in the .ibs file for

 | all I/O pins and PDN described

 | by signal\_names (sn)

[End Interconnect Model Group]

|

| Example 3

|

[Interconnect Model Group] A1\_TS

| Interconnect Model Set file\_reference

A1\_TS touchstone/ts\_sets.ims | [Interconnect Model Set] is

 | in ts\_sets.ims under the

 | touchstone directory for A1

[End Interconnect Model Group]

|

| Example 4

|

[Interconnect Model Group] A1\_ISS\_buf\_pad\_TS\_pad\_pin

| Interconnect Model Set file\_reference

A1\_ISS\_buf\_pad NA | Interconnect Model Sets combined from

A1\_TS\_pad\_pin NA | buffer to pad and pad to pin Sets with

 | different file formats for A1

[End Interconnect Model Group]

|

| Example 5

|

[Interconnect Model Group] Full\_ISS\_split\_IO\_PDN\_3

| Interconnect Model Set file\_reference

Full\_ISS\_buf\_pin\_IO\_1 NA | IO paths with common sn reference

Full\_ISS\_buf\_pin\_PDN\_1 NA | Detailed (by pin) PDN paths

 | PDN terminals G1-G4 get shorted

[End Interconnect Model Group]

 \*\*\*\*\* ALL OTHER EXAMPLES NEED CAREFUL REVIEW FOR REFERENCING \*\*\*\*\*

*Keyword:* [**End Interconnect Model Group**]

*Required:* Yes, for each instance of the [Interconnect Model Group] keyword

*Description:* Indicates the end of the data for one [Interconnect Model Group].

*Example:*

[End Interconnect Model Group]

The following keywords should be placed in section 5, COMPONENT DESCRIPTION, after the [Pin Mapping] keyword.

Keyword: [Bus Label]

*Required:* No

*Description:* Defines bus\_label names and associates a POWER or GND signal\_name with one or more bus\_label names within a Component. The bus\_label names can be used to define connection points for Interconnect Model terminals.

*Sub-Params:* signal\_name

*Usage Rules:* The first column shall contain a bus\_label. The second column, signal\_name, shall be a corresponding signal\_name entry for a pin under the [Pin] keyword that uses the model\_name POWER or GND.

The [Bus Label] keyword shall be followed by the string “signal\_name” as a column heading.

Duplicate bus\_labels are not permitted. A bus\_label may be defined also by the [Pin Mapping] keyword, by a signal\_name under the [Pin] keyword, and/or by the [Die Supply Pads] keyword below.

Column length limits are:

[Bus Label] 15 characters max

signal\_name 40 characters max

*Example:*

[Bus Label] signal\_name

VDD1 VDD

VDD2 VDD

VDD3 VDD

VSS1 VSS

VSS2 VSS

*Keyword:* **[Die Supply Pads]**

*Required:* No

*Description:* Defines supply rail die pads and associates signal\_names and bus\_labels with those die pads.

*Sub-Params:* signal\_name, bus\_label

*Usage Rules:*  Only die pads with signal\_names that occur on POWER or GND pins are allowed. Each line shall contain either two or three columns. The first column shall contain the supply die pad name (the column entry is also referred to as “pad\_name” elsewhere in this document). The second column, signal\_name, shall contain the signal name as given under the [Pin] keyword. The third column is optional. If it exists, it is a bus\_label. If the third column does not exist, then the bus\_label shall be the signal\_name.

The [Die Supply Pads] keyword shall be followed by the strings “signal\_name” and “bus\_label” as column headings.

*Other Notes:* The data in this section consists of a list of pad\_names and their corresponding signal\_names and bus\_labels, which can be used to mate package and on-die power delivery networks.

The keywords described above ([Pin Mapping], [Pin], [Bus Label], and [Die Supply Pads]) describe several ways to name the bus\_label entries. Briefly, they are listed here:

[Pin Mapping] associates each rail pin\_name with a bus\_label for all rail pin\_names. For the listed buffer I/O pin\_names (in the first column), the bus\_label entries are listed under the pulldown\_ref, pullup\_ref, gnd\_clamp\_ref, power\_clamp\_ref, and ext\_ref columns of [Pin Mapping]. This listing of any or all POWER and/or GND pin\_names (also referred to as rails) is optional.

[Pin] associates each pin\_name with a signal\_name. The signal\_name can be used as a bus\_label for rail pin\_names that are not listed under [Pin Mapping] or not described by the [Bus Label] and [Die Supply Pads] keywords.

[Bus Label] also associates signal\_names with bus\_labels.

[Die Supply Pads] is used to define rail pad\_names and to associate them with signal\_name, but the second and third columns can provide another way to associate signal\_names with bus\_labels in a manner that may not be covered above.

Such entries can be used as terminals at designated locations in [Interconnect Model] terminal lines described later in Section XXX. The keywords can also be used to describe how different Terminal\_type\_qualifiers (described later) can be associated with each other. For example, a POWER or GND pin\_name with a bus\_label entry in [Pin Mapping] would find its corresponding signal\_name from the [Pin] keyword for the same pin\_name.

With these four keywords, it is possible to create bus\_label names for rails in four different ways, and any or all of the four ways can be used at once.

These keywords also support using each rail terminal individually or for creating a single terminal that connects terminals that connects rails with the same bus\_label or signal\_name, or to designate rail pad\_names that might be different than rail pin\_names. With these keywords, the number of rail nets can be reduced. Also, a different number of rail terminals can be entered at each boundary to support few-to-many or many-to-few connection terminals.

*Example:*

[Die Supply Pads] signal\_name bus\_label

VDDQ VDDQ

VDD1 VDD VDDa

VDD2 VDD VDDa

VDD3 VDD VDDb

VSS1 VSS

VSS2 VSS

The following text should be added at the beginning of Chapter 7, PACKAGE MODELING, after the chapter title.

**7.1 INTRODUCTION**

Several package modeling formats are available in IBIS. These include:

1. Lumped [Component]-level models for the entire [Component], using the [Package] keyword.
2. Lumped [Component]-level modeling per-pin, using the [Pin] keyword.
3. [Package Model] (including [Alternate Package Models] and [Define Package Model]).
4. [Interconnect Model Group] and the keywords associated with it.

The lumped formats are described in the [Package] and [Pin] keyword definitions in Chapter 5. Keywords for use with the [Package Model] format are described in this chapter, while keywords for use with [Interconnect Model Group] are described in Chapter 12.

**7.2 RULES OF PRECEDENCE**

The order of precedence for package model data to be used by EDA tools in simulation is defined below, in ascending order. If a package data format at a numerically higher position on the list is available in an IBIS or related file, that data shall be considered by the EDA tool to be more detailed and is therefore preferred.

1. [Component]/[Package]
2. [Component]/[Pin]
3. [Package Model] (including [Alternate Package Models] and [Define Package Model])
4. [Interconnect Model Group]

Note that [External Circuit] and [Node Declarations] are mutually exclusive with [Interconnect Model Group] within the same [Component]. [Package Model] and [Interconnect Model Group] may both be present for the same [Component] but should not both be used at the same time.

**7.3 KEYWORDS FOR USE WITH [PACKAGE MODEL]**

< Insert Existing Text Here>

Page 141 for the [Description] keyword, Replace:

*Usage Rules:* The description must be less than 60 characters in length, must fit on a single line, and may contain spaces.

With:

*Usage Rules:* The description shall fit on a single line, and may contain spaces.

The following new Chapter 12 should be added after Chapter 11.

**12 INTERCONNECT MODELING**

**12.1 INTRODUCTION**

IBIS supports broadband interconnect models describing connections between the pins of a component and its I/O buffers. These interconnect models may include descriptions of frequency-dependent losses, interconnect coupling and/or complex supply rail distributions.

Interconnect is defined between up to three interface locations:

* pin, where a component connects to a printed circuit board
* die pad, where a component die connects to the routing on a package substrate
* buffer, where the buffer itself connects to the die substrate and routing

The relationship between the terminals at the buffer, die pad, and pin interfaces is shown in the figure below.



Figure 47 – Example Interconnect Model Structure

The connection between the pin and die pad is generally called “package interconnect”, while the connection between the die pad and the buffer is generally called “on-die interconnect.” The die pad is distinct from the buffer terminal; the buffer includes the circuitry that would be described through the [Model] keyword and related keywords, and would not include transmission line behavior.

Interconnect models may be supplied separately for on-die interconnect and package interconnect, or may be supplied as a single model for the entire connection between the package pins and buffers.

The electrical behavior of an interconnect is described through either IBIS-ISS subcircuits or Touchstone network parameters. An Interconnect Model defines the connections to either an IBIS-ISS subcircuit or a Touchstone file. An Interconnect Model may describe the connection between the I/O pins of the package and the buffers, the pins of the package and the die pads, or the die pads and buffers. Rail (supply) terminals related to GND and POWER pins can be described in a similar manner, but can also exist on only one interface for serving as reference terminals or for supporting, for example, decoupling circuitry.

Interconnect Models are organized into Interconnect Model Sets. An [Interconnect Model Set] keyword consists of one or more [Interconnect Model] keywords. One Interconnect Model Set may contain groups of similar interconnect models or different interconnect models to describe the complete connections from the buffer to pin interface.

Each I/O pin is associated with one I/O buffer terminal and optionally one I/O die pad. By contrast, there is no required one-to-one relationship between rail pins, (optional) rail die pads, and buffer rail terminals.

Figure 48 below shows the [Interconnect Model] terminals for an I/O path on both package and on-die substrates.



Figure 48 – Package Substrate I/O Paths

The figure also shows on-die interconnect routes that may experience crosstalk effects. This example assumes that only a few routes out of a larger bus are shown. In such a model, the crosstalk on any one route *in the model* could only be caused by its nearest neighbors.

While each of the inner two routes in the figure may have all potential crosstalk represented in the model, the outer signals would not. The model maker would therefore indicate that connections to the outer routes’ terminals do not include all of their aggressors by adding the optional argument “Aggressor\_Only” to their terminals. The descriptions of the associated terminals would not use the “Aggressor\_Only” designation for the inner routes. The EDA tool may therefore assume in simulation that the inner routes have all (or more practically most of) the coupling to their aggressor connections represented in the model.

Crosstalk simulations require Interconnect Models to have connections to multiple I/O pin\_names.

Figure 49 of a package and die shows graphically the potential [Interconnect Model] terminals for a rail connection. A single pin terminal for a supply rail connects to multiple die pads. Note that these terminals may be collapsed to a single terminal at the pin (as shown), or alternately at the die pad interface and/or the buffer rail terminals.



Figure 49 – Package Substrate Rail Terminals

The terminal section of an [Interconnect Model] describes how the terminals of an Interconnect Model subcircuit or Touchstone file instance are connected at a buffer terminal, die pad interface or pin/board interface.

**12.2 GENERAL INTERCONNECT SYNTAX REQUIREMENTS**

Terminal lines under the [Interconnect Model] keyword describe connections.

I/O terminals shall be connected using only the pin\_name qualifier at these locations:

* pins: I/O pin\_name
* die pads: I/O pin\_name
* buffer: I/O pin\_name

Rail terminal connections have more options to support direct connections to terminals or to groups of terminals using signal\_name, bus\_label, or pad\_name entries at the pin, die pad or buffer locations. For the following locations the rail terminal can connect to:

* pins
* a specific rail pin\_name
* all of the pins of a rail signal\_name
* all of the pins of a bus\_label
* die pads
* all of the die pads with a rail signal\_name
* all of the die pads with a rail bus\_label
* a specific die pad pad\_name
* buffer rail terminals
* all of the buffer rail terminals of a rail signal\_name
* all of the buffer rail terminals of a bus\_label
* a specific buffer rail terminal for an I/O buffer pin\_name

One or more Interconnect Model Sets may be included in a separate Interconnect Model Set file, using a file name with the extension “ims”, or within the .ibs file where [Interconnect Model Group] is used. The [Interconnect Model Set] keyword can contain the optional [Manufacturer] and [Description] keywords and one or more [Interconnect Model] keywords and the [Interconnect Model] associated subparameters, as is listed in Table 40.

Table 40 – Interconnect Modeling Keywords and Subparameters

| **Keyword or Subparameter** | **Notes** |
| --- | --- |
| [Interconnect Model Set] |  |
| [Manufacturer] | (note 1) |
| [Description] | (note 1) |
| [Interconnect Model] | (note 2) |
| Param |  |
| File\_TS | (note 3) |
| File\_IBIS-ISS | (note 3) |
| Unused\_port\_termination | (note 4) |
| Number\_of\_terminals | (note 5) |
| <terminal line> | (note 6) |
| [End Interconnect Model] | (note 7) |
| [End Interconnect Model Set] | (note 8) |
| Note 1 [Manufacturer] and [Description] are each optional keywords within any [Interconnect Model Set].Note 2 At least one [Interconnect Model] is required for each [Interconnect Model Set].Note 3 One of either the File\_TS or File\_IBIS-ISS subparameters is required.Note 4 Required for Touchstone files where ports are unused, illegal if there are no unused ports or for IBIS-ISS fileNote 5 This subparameter shall be followed by the “=” character and an integer value, with both optionally surrounded by whitespace.Note 6 See text below.Note 7 Required when the [Interconnect Model] keyword is usedNote 8 Required when the [Interconnect Model Set] keyword is used |

When Interconnect Model Set definitions occur within a .ibs file, their scope is “local”— they are known only within that .ibs file and no other .ibs file. In addition, within that .ibs file, they override any interconnect package models defined using the [Package], [Pin], or [Define Package Model] keywords. Interconnect Models in separate .ims files referenced by the [Interconnect Model Group] keyword in a .ibs file also override any interconnect package models defined in the same .ibs file using the [Package], [Pin], or [Define Package Model] keywords.

Usage Rules for the .ims file:

Interconnect models are stored in a file whose file name uses the format:

<stem>.ims

The <stem> provided shall adhere to the rules given for the [File Name] keyword. Use the “ims” extension to identify files containing Interconnect Models. The .ims file shall contain the [IBIS Ver], [File Name], [File Rev], and the [End] keywords. Optional elements include the [Date], [Source], [Notes], [Disclaimer], [Copyright], and [Comment Char] keywords. All of these keywords and associated subparameters follow the same rules as those for a normal .ibs file.

Note that the [Component] and [Model] keywords are not allowed in the .ims file. The .ims file is for Interconnect Models only.

*Keyword:* [Interconnect Model Set]

*Required:* No

*Description:* Used to contain Interconnect Models

*Usage Rules:* [Interconnect Model Set] has a single argument, which is the name of the Interconnect Model Set. The length of the Interconnect Model Set name shall not exceed 40 characters in length. Blank characters are not allowed. The [Interconnect Model Set]/[End Interconnect Model Set] keyword pair is hierarchically equivalent in scope to [Component] and [Model].

The section under the [Interconnect Model Set] keyword may contain a [Manufacturer] keyword section and [Description] keyword section and shall contain one or more Interconnect Models. See the section [Interconnect Model] for a description of the content of each Interconnect Model.

An [Interconnect Model Set] contains a list of [Interconnect Model]s that have a logical association such as:

* All models in a bus (e.g.. DDR4, or PCIeG3)
* Full PDN structure from buffer to pin
* On-die PDN structure from buffers to die pads
* Package only PDN structure from die pads to pins
* All I/O models between die pad and pin
* All I/O models between buffer and die pad
* All I/O models between buffer and pin
* Combined I/O and PDN models
* All uncoupled models
* Coupled models
* Touchstone electrical models
* Decoupling capacitor models
* IBIS-ISS electrical models

*Example:*

[Interconnect Model Set] Signal\_Integrity

[Manufacturer] Acme Packaging, Inc.

[Description] This set contains one model for each I/O buffer

[Interconnect Model] DQ1

…

[End Interconnect Model]

[Interconnect Model] DQ2

…

[End Interconnect Model]

[Interconnect Model] DQS

…

[End Interconnect Model]

[End Interconnect Model Set]

*Keyword:* [Manufacturer]

*Required:* No

*Description:* Specifies the name of the [Interconnect Model Set] manufacturer.

*Usage Rules:* The length of the manufacturer’s name shall not exceed 40 characters (blank characters are allowed, e.g., Oklahoma Instruments).

*Example:*

[Manufacturer] NoName Corp.

*Keyword:* [Description]

*Required:* No

*Description:* Provides a concise yet easily human-readable description of what kind of interconnect the [Interconnect Model Set] represents.

*Usage Rules:* The description shall fit on a single line, and may contain spaces.

*Example:*

[Description] 220-Pin Quad Ceramic Flat Pack

*Keyword:* [**End Interconnect Model Set**]

*Required:* Yes, for each instance of the [Interconnect Model Set] keyword.

*Description:* Indicates the end of the Interconnect Model Set data.

*Example:*

[End Interconnect Model Set]

*Keyword:* [Interconnect Model]

*Required:* No

*Description:* Marks the beginning of an Interconnect Model description that is used to define the interfaces to IBIS-ISS subcircuit or Touchstone files.

*Sub-Params:* Param, File\_TS, File\_IBIS-ISS, Number\_of\_terminals

*Usage Rules:* [Interconnect Model] has a single argument, which is the name of the associated Interconnect Model. The length of the Interconnect Model name shall not exceed 40 characters in length. Blank characters are not allowed. The [Interconnect Model]/[End Interconnect Model] keyword pair is hierarchically scoped by the [Interconnect Model Set]/[End Interconnect Model Set] keywords.

The [Interconnect Model]/[End Interconnect Model] section defines both the association between a Touchstone file or IBIS-ISS subcircuit and an Interconnect Model, as well as defining the terminals and terminal usage for the Interconnect Model in the context of the given [Component].

An [Interconnect Model] shall contain one and only one of the following combinations:

* pins and buffer terminals (full package model)
* pins and die pads (package only model)
* die pads and buffer terminals (on-die interconnect model)
* rail terminals at only one interface and no I/O terminals

*Other Notes:* If a full package model contains an I/O pin terminal for a pin\_name then it shall also contain an I/O buffer terminal for the same pin\_name. If a package only model contains an I/O pin terminal for a pin\_name then it shall also contain an I/O die pad for the same pin\_name. If an on-die interconnect model contains an I/O buffer terminal for a pin\_name then it shall also contain an I/O die pad for the same pin\_name.

An [Interconnect Model] may contain:

* only power rail models
* one or more I/O signal models
* both power rail models and one or more I/O signal models
* pin rails only
* die pad rails only
* buffer rails only

Each terminal of an Interconnect Model is connected to a node and has a “voltage”. This, as stated, is imprecise. Voltage, by definition, is a potential difference between two points. It is common to probe and plot the potential difference between simulator nodes at a terminal and a simulator global reference node (e.g., SPICE ideal node “0”), the latter of which is often assumed and/or unstated. This is valid for non-power-aware simulations when the local reference (or return path) node is forced to a global reference by the simulator, or for “ground-referenced” power aware simulations that lump the effects of all rail interconnects together. However, this is not valid when the local reference nodes are “floating”. In this case it is important that the actual reference node for measurements at the I/O buffer is included as a terminal in the Interconnect Model. If this is not done, then the Interconnect Model will not correctly account for all return currents, particularly from capacitive elements. If an Interconnect Model does not contain a reference terminal, then the user of these models should be aware that using these models in power-aware simulations can potentially introduce errors in simulations.

The following subparameters are defined:

Param

File\_IBIS-ISS

File\_TS

Unused\_port\_termination

Number\_of\_terminals = <value>

In addition to these subparameters, the [Interconnect Model]/[End Interconnect Model] section may contain lines describing terminals and their connections. No specific subparameter name or other string is used to identify terminal lines.

Unless noted below, no Interconnect Model subparameter requires the presence of any other subparameter.

Param rules:

The subparameter Param is optional and only legal with the File\_IBIS-ISS subparameter documented below. Param is illegal with the File\_TS subparameter documented below. Param shall be followed by three arguments: an unquoted string argument giving the name of the parameter to be passed into the IBIS-ISS subcircuit, a reserved word for the parameter format, and one numerical value or one string value (surrounded by double quotes) for the parameter value to be passed into the IBIS-ISS subcircuit.

The numerical value rules follow the scaling conventions in Section 3.2, “SYNTAX RULES”. The EDA tool is responsible for translating IBIS specified parameters into IBIS-ISS parameters. For example, 1 megaohm, would be represented as 1M in Param value according to the Section 3 rules, but would be converted by the EDA tool to case-insensitive 1meg (1X is not recommended) or 1E6 for IBIS-ISS use. Quoted string parameters in IBIS are converted to the string parameter syntax in IBIS-ISS subcircuits. For example, the Param value "typ.s2p" would be converted to str('typ.s2p') in IBIS-ISS subcircuits.

*Examples:*

| Param name format value

Param abc Value 2m | 2E-3 in IBIS

Param def Value 4k | 4E3 in IBIS

Param ts\_file Value "typ.s2p" | file name string passed

 | into IBIS-ISS

File\_IBIS-ISS rules:

Either File\_IBIS-ISS or File\_TS is required for a [Interconnect Model]/[End Interconnect Model] group*.* The File\_IBIS-ISS subparameter is followed by two unquoted string arguments consisting of the file\_reference and circuit\_name (.subckt name) for an IBIS-ISS file. The IBIS-ISS file under file\_reference shall be located in the same directory as the referencing .ibs file or .ims file or in a specified directory under the referencing file as determined by the directory path (i.e., a file reference containing a relative path to a directory below that of the referencing .ibs or .ims file is permitted).

*Example:*

| file\_type file\_reference circuit\_name(.subckt name)

File\_IBIS-ISS net.iss netlist\_typ

File\_TS rules:

Either File\_TS or File\_IBIS-ISS is required for a [Interconnect Model]/[End Interconnect Model] group.File\_TS is followed by one unquoted string argument, which is the file\_reference for a Touchstone file. The Touchstone file under file\_reference shall be located in the same directory as the referencing .ibs file or .ims file or in a specified directory under the referencing file as determined by the directory path (i.e., a file reference containing a relative path to a directory below that of the referencing .ibs or .ims file is permitted).

*Example:*

| file\_type file\_reference

File\_TS typ.s8p

Unused\_port\_termination rules:

The Unused\_port\_termination subparameter is required under this condition:

File\_TS is used and the number of terminal lines (described below) is less than N+1 (where N is the number of ports in the Touchstone file)

Unused\_port\_termination is illegal under these conditions:

File\_IBIS-ISS is used.

File\_TS is used and the number of terminal lines is N+1

If required, only one Unused\_port\_termination subparameter may appear for a given [Interconnect Model] keyword.

The Unused\_port\_termination subparameter is followed by white space and one of these arguments:

Open

Reference

Resistance

“Open” declares that the unused ports remain unterminated (open-circuited).

“Reference” declares that the EDA tool terminates all unused ports with resistors whose resistance values are equal to the reference impedances provided in the Touchstone file for the respective unused ports, and all connected to the model’s reference terminal.

“Resistance” declares that the EDA tool terminates all unused ports with resistors, all having the same value, and all connected to the model’s reference terminal. The “Resistance” entry is followed by a third column entry with the (non-negative) numerical resistance value.

*Examples:*

Unused\_port\_termination Open

Unused\_port\_termination Reference

Unused\_port\_termination Resistance 43.5

Number\_of\_terminals rules:

The Number\_of\_terminals subparameter is required and defines the number of terminals associated with the Interconnect Model. The subparameter name shall be followed by a single integer argument on the same line. The argument shall be separated from the subparameter name by the “=” character. The subparameter name, “=” character, and argument may optionally be separated by whitespace.

Only one Number\_of\_terminals subparameter may appear for a given [Interconnect Model] keyword. The Number\_of\_terminals subparameter shall appear before any terminal lines and after all other subparameters for a given Interconnect Model.

For File\_IBIS-ISS, the Number\_of\_terminals value shall be equal to the number of subcircuit terminals for an IBIS-ISS subcircuit. Because an IBIS-ISS subcircuit requires at least one terminal the Number\_of\_terminals value shall be 1 or greater. The IBIS-ISS subcircuit terminals shall not contain an ideal reference node (SPICE node 0 or its synonyms).

For File\_TS, the Number\_of\_terminals value shall be a value equal to N+1 (where N is the number of ports in the Touchstone file). Because a Touchstone file requires at least one port, the Number\_of\_terminals value shall be 2 or greater.

*Example:*

Number\_of\_terminals = 3

Terminal line rules:

The terminal lines shall appear after the Number\_of\_terminals subparameter and before the [End Interconnect Model] keyword.

Terminal lines are of the following form, with each identifier separated by whitespace:

 <Terminal\_number> <Terminal\_type> <Terminal\_type\_qualifier> <Qualifier\_entry> [Aggressor\_Only]

Terminal\_number

The Terminal\_number is the identifier for a specific terminal. The value shall be 1 or greater and less than or equal to the Number\_of\_terminals. The same Terminal\_number shall not appear more than once for a given Interconnect Model.

For File\_IBIS-ISS, the Terminal\_number entry shall match the IBIS-ISS terminal (node) position. The Terminal\_number entries may be listed in any order as long as there are no duplicate entries. Each IBIS-ISS terminal shall have terminal line entry.

For File\_TS, the Terminal\_number entry shall match the Touchstone file port number or reference terminal line, as shown below. The Terminal\_number entries may be listed in any order as long as there are no duplicate entries. The terminal line for Terminal\_number N+1 is required as a reference terminal for each port and shall be connected to a rail terminal or A\_gnd in the Interconnect Model. At least one other terminal line entry is required.

* Terminal\_number Port
* 1                     1
* 2                          2
* …
* N                        N
* N+1 Reference terminal for the Touchstone file

For Touchstone files, each unused port and its corresponding Terminal\_number shall be terminated in simulation with a resistor whose value corresponds to the Unused\_port\_termination subparameter entry. The resistor is connected to the model’s reference terminal.

Terminal\_type
The Terminal\_type is a string that identifies whether the terminal is a reference, supply or I/O terminal and whether the terminal is connected at the buffer, die pad, or pin level. (Note that “I/O” in this context is a synonym for “signal”, as opposed to “supply” or “rail”; it is not intended to imply model type as used in the “Model\_type” subparameter). Furthermore, if the terminal is connected to a buffer supply rail, the Terminal\_type identifies to which specific buffer rail the terminal is connected. The Terminal\_type shall be one of the following:

* Pin\_I/O
* Pad\_I/O
* Buffer\_I/O
* Pin\_Rail
* Pad\_Rail
* Buffer\_Rail
* Pullup\_ref
* Pulldown\_ref
* Power\_clamp\_ref
* Gnd\_clamp\_ref
* Ext\_ref
* A\_gnd

Buffer\_I/O, Pullup\_ref, Pulldown\_ref, Power\_clamp\_ref, Gnd\_clamp\_ref, Ext\_ref and Buffer\_Rail are terminals of an Interconnect Model that connect directly to I/O buffers.

Pad\_I/O and Pad\_Rail are terminals that are at the die pad interface.

Pin\_I/O and Pin\_Rail are terminals that are at the pin interface that can connect the package to the PCB.

The Terminal\_types Buffer\_I/O, Pad\_I/O and Pin\_I/O are used only for any single terminal of a buffer described by the [Model] keyword and for any Model\_type subparameter listed in Section 5, Table 1. The Model\_types Series and \*\_diff are used for two-terminal configurations, and their terminals require two separate Buffer\_I/O, Pad\_I/O or Pin\_I/O Terminal\_type lines.

Terminal\_type A\_gnd defines a connection to the simulator global reference node. The A\_gnd node can be used at any interface.

Terminal\_type A\_gnd is not required under File\_TS or File\_IBIS-ISS.

If present under File\_TS, Terminal\_type A\_gnd may be used only once on the N+1th terminal line.

If present under File\_IBIS-ISS, Terminal\_type A\_gnd may be used any number of times on any of the terminal lines.

Terminal\_type\_qualifier
The Terminal\_type\_qualifier is a string that identifies the association between a terminal and a specific pin\_name, signal\_name, bus\_label, or pad\_name. Only certain Terminal\_types may be used with pad\_names, pin\_names, signal\_names, or bus\_labels respectively, as outlined in the Connecting Pins, Pads, and Buffer Terminals section below and summarized in Table 41.

Qualifier\_entry
The <Qualifier\_entry>, shown in angle brackets, is the name required for the following Terminal\_type\_qualifiers:

pin\_name <pin\_name\_entry>

signal\_name <signal\_name\_entry>

bus\_label <bus\_label\_entry>

pad\_name <pad\_name\_entry>

Aggressor\_Only

The Aggressor\_Only entry is optional and is indicated by the string “Aggressor\_Only” without the quotation marks.

Multi-line Interconnect Models may describe only a subset of a coupled structure (e.g., a 64-line bus may be described by a four-line Interconnect Model). As a result, while the interconnects at the edges of the Interconnect Model may induce crosstalk onto other interconnects nearby, being on the edge of the Interconnect Model, they may not themselves experience the full crosstalk impact that the corresponding interconnect experiences in the real, full structure.

Figure xx1 shows examples of Interconnect Models having full coupling for some pins and partial coupling for other pins of an example part package, and the corresponding Aggressor\_Only entries. The Aggressor\_Only column entry is allowed on all terminal locations for I/O terminals to indicate such incomplete coupling. Terminals that include the Aggressor\_Only entry may not be suitable to be simulated as victims, as they do not experience the full coupling present in the real physical structure. If an I/O terminal is not identified as Aggressor\_Only, then the interconnect to that I/O terminal includes coupling to all interconnections deemed necessary for coupled signal analysis. Within any Interconnect Model, if a terminal line is identified as Aggressor\_Only, then the corresponding terminal line associated with the same pin\_name shall also be identified as Aggressor\_Only.



Figure XX1 – Aggressor\_Only examples

Figure XX2 illustrates a special situation when a pin (pin 4 in this case) is associated with more than one Interconnect Model within the same Interconnect Model Group in one or more Interconnect Model Sets, and all of the terminal lines associated with that pin are marked as Aggressor\_Only. The first Interconnect Model in this example is associated with pins 2-4 and is shown in green. The second Interconnect Model is associated with pins 4-6 and is shown in red. Note that pin 4 is marked as Aggressor\_Only in both Interconnect Models, and there are no other Interconnect Models referenced through Interconnect Model Set(s) in this Interconnect Model Group with a terminal line for pin 4 without the Aggressor\_Only marking. Since EDA tools are not expected to provide a selection user interface for Interconnect Models in Interconnect Model Sets, this case would present an ambiguity if the user wanted to run a simulation with pin 4.



Figure XX2 – A special case with Aggressor\_Only

Connecting Pins, Pads and Buffer Terminals

Terminal lines describe the IBIS-ISS node or Touchstone port that each terminal should be connected to. Terminals may be at pins, die pads or the buffer. The arrangement of the terminal line entries (columns) is described below.

* The first column, Terminal\_number, contains an integer between 1 and the Number\_of\_terminals that describes the ordinal (positional) number of the IBIS-ISS node in the [Interconnect Model] subcircuit or Touchstone file port. The second column is Terminal\_type, the third column is Terminal\_type\_qualifier, the fourth column is Qualifier\_entry and there is an optional fifth column “Aggressor\_Only”
* The second column, Terminal\_type, determines if the terminal is at a pin, die pad or buffer.
	+ For I/O connections
		- At pins, die pads or buffers
			* Terminal\_type can be Pin\_I/O, Pad\_I/O and Buffer\_I/O
			* Terminal\_type\_qualifier shall be pin\_name.
			* Qualifier\_entry shall be the pin\_name of an I/O pin.
	+ For rail connections
		- At pins
			* Terminal\_type shall be Pin\_Rail
			* Terminal\_type\_qualifier shall be one of the following
				+ pin\_name

Qualifier\_entry shall be a rail pin\_name

* + - * + signal\_name

Qualifier\_entry shall be a rail signal\_name

* + - * + bus\_label

Qualifier\_entry shall be a bus\_label

* + - At die pads
			* Terminal\_type shall be Pad\_Rail
			* Terminal\_type\_qualifier shall be
				+ signal\_name

Qualifier\_entry shall be a rail signal\_name

* + - * + bus\_label

Qualifier\_entry shall be a bus\_label

* + - * + pad\_name

Qualifier\_entry shall be the pad\_name of a rail pad

* + - At buffers
			* Terminal\_type shall be Buffer\_Rail or any of the five \*\_ref terminals associated with an I/O buffer below
			* Buffer\_Rail Terminal\_type\_qualifier shall be
				+ signal\_name

Qualifier\_entry shall be a rail signal\_name

* + - * + bus\_label

Qualifier\_entry shall be a bus\_label

* + - * Pullup\_ref, Pulldown\_ref, Power\_clamp\_ref, Gnd\_clamp\_ref or Ext\_ref Terminal\_type\_qualifiers shall be
				+ pin\_name

Qualifier\_entry shall be the I/O buffer pin\_name

* + - At any interface
			* Terminal\_type A\_gnd is available at any interface and without any Terminal\_type qualifier

Table 41 summarizes the rules described above.

Table 41 – Allowed Terminal\_type Associations1

| **Terminal\_type** | **Terminal\_type\_qualifier** | **Aggressor\_Only** |
| --- | --- | --- |
| **pin\_name** | **signal\_name** | **bus\_label** | **pad\_name** |
| Pin\_I/O | X |  |  |  | A |
| Pad\_I/O | X |  |  |  | A |
| Buffer\_I/O | X |  |  |  | A |
| Pin\_Rail | Y | Y | Y |  |  |
| Pad\_Rail |  | Y | Y | Z |  |
| Buffer\_Rail |  | Y | Y |  |  |
| Pullup\_ref | X |  |  |  |  |
| Pulldown\_ref | X |  |  |  |  |
| Power\_clamp\_ref | X |  |  |  |  |
| Gnd\_clamp\_ref | X |  |  |  |  |
| Ext\_ref | X |  |  |  |  |
| A\_gnd |  |  |  |  |  |

Notes

1. In the table, “X” refers to I/O pin names. “Y” and “Z” are POWER and GND names. The letter “A” designates "Aggressor\_Only".

Each terminal of an interface represents either 1) a list of pins at the pin interface, 2) a list of die pads at the die pad interface, or 3) a list of buffer model terminals. It is illegal in one interface, in one model, for 1) a pin to appear in two terminals, 2) a die pad to appear in two terminals, or 3) a buffer model terminal to appear in two terminals.

For I/O terminals, the pin\_name value shall not be repeated at any one interface. For rail terminals, the rail terminal name shall not be repeated at any one interface. Also, a rail terminal name that overlaps with another rail terminal name (expressed as pin\_name, pad\_name, bus\_label, signal\_name) shall not be entered at any one interface. For example, if the [Pin] keyword contains the following row:

[Pin]

…

10  VDD POWER

…

then signal\_name VDD overlaps with pin\_name 10.  So, Terminal\_type lines “Pin\_Rail signal\_name VDD” and “Pin\_Rail pin\_name 10” shall not both be entered in a single Interconnect Model.

For Interconnect Model Sets containing several Interconnect Models, the Terminal\_types at the same interface are considered connected if the terminal names match. I/O terminals assigned to the same pin\_name at the die pad interface in two Interconnect Models are connected. For rail terminals, identical names are connected and rail terminal names that overlap with another rail terminal name are connected. An excepton exists if the Interconnect Models are not to be used together because of different Aggressor\_Only entries, as illustrated in Figures XX1 and XX2 above. In these cases, overlapping I/O pin\_names are permitted because the Interconnect Models are not to be used together in simulations. The rails connections and paths in the unused Interconnect Models are also not used.

When an Interconnect Model Group references several Interconnect Model Sets as shown under the [Interconnect Model Group] keyword, the same connection rules apply for all Interconnect Models in the Interconnect Model Sets that are used in the simulation.

In the examples below, the Interconnect Models have unique Terminal\_type names at each interface. Some examples illustrate several Interconect Models within an Interconnect Model Set with identical or overlapping Terminal\_type names. During simulations, the EDA tool should connect these terminals.

*Examples:*

| All examples show a [Interconnect Model Set] for grouping of the

| [Interconnect Model] descriptions that can be referenced

|

| Naming convention for [Interconnect Model Set] examples is below

| ([Interconnect Model] may show additional details)

|

| Full – Includes all I/O pins

| A1 or A1\_A3 – Designated pin or pins

| TS - Touchstone representation

| ISS - IBIS-ISS representation

| PDN - Includes power delivery network, can also be PU and PD

| IO - Only if modified differently than PDN below for buf\_pad\_pin

| buf\_pad\_pin – Includes models for buf\_pad, pad\_pin; if missing, buf\_pad

| sn - Uses signal\_name; if missing assumes pin\_name

| bl - Uses bus\_label; if missing assumes pin\_name

| pn - Uses pad\_name; if missing assumes pin\_name

| XTALK - Cross talk analysis (coupled nets may include Aggressor\_Only)

| Examples 1 – 11 apply to the configuration below:

[Pin] signal\_name model\_name      R\_pin   L\_pin   C\_pin

A1    DQ1         DQ

A2    DQ2         DQ

A3    DQ3         DQ

D1    DQS+        DQS

D2    DQS-        DQS

P1    VDD         POWER

P2    VDD         POWER

P3    VDD         POWER

P4    VDD         POWER

P5    VDD         POWER

G1    VSS         GND

G2    VSS         GND

G3    VSS         GND

G4    VSS         GND

[Diff Pin] inv\_pin  vdiff  tdelay\_typ tdelay\_min tdelay\_max

D1         D2       NA     NA         NA         NA

[Die Supply Pads]  signal\_name bus\_label

VDD1 VDD

VDD2 VDD

VDD3 VDD

VSS1 VSS

VSS2 VSS

[Pin Mapping] pulldown\_ref pullup\_ref gnd\_clamp\_ref power\_clamp\_ref ext\_ref

A1            VSS          VDD        NC            NC              NC

A2            VSS          VDD        NC            NC              NC

A3            VSS          VDD        NC            NC              NC

D1            VSS          VDD        NC            NC              NC

D2            VSS          VDD        NC            NC              NC

| Pins below are optional per [Pin Mapping] rules

P1 NC VDD

P2 NC VDD

P3 NC VDD

P4 NC VDD

P5 NC VDD

G1 VSS NC

G2 VSS NC

G3 VSS NC

G4 VSS NC

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 1: Terminals for full IBIS-ISS component with PDN, as depicted below.

|

[Interconnect Model Set] Full\_ISS\_PDN\_1

|-----

[Interconnect Model] Full\_ISS\_buf\_pin\_1

File\_IBIS-ISS full\_buf\_pin\_1.iss full\_buf\_pin\_typ

Number\_of\_terminals = 29

1  Pin\_I/O      pin\_name A1  |  DQ1         DQ

2  Pin\_I/O      pin\_name A2  |  DQ2         DQ

3  Pin\_I/O      pin\_name A3  |  DQ3         DQ

4  Pin\_I/O      pin\_name D1  |  DQS+        DQS

5  Pin\_I/O      pin\_name D2  |  DQS-        DQS

6  Pin\_Rail     pin\_name P1  |  VDD         POWER

7  Pin\_Rail     pin\_name P2  |  VDD         POWER

8  Pin\_Rail     pin\_name P3  |  VDD         POWER

9  Pin\_Rail     pin\_name P4  |  VDD         POWER

10 Pin\_Rail     pin\_name P5  |  VDD         POWER

11 Pin\_Rail    pin\_name G1  |  VSS         GND

12 Pin\_Rail     pin\_name G2  |  VSS         GND

13 Pin\_Rail     pin\_name G3  |  VSS         GND

14 Pin\_Rail     pin\_name G4  |  VSS         GND

15 Buffer\_I/O pin\_name A1  |  DQ1         DQ

16 Buffer\_I/O pin\_name A2  |  DQ2         DQ

17 Buffer\_I/O pin\_name A3  |  DQ3         DQ

18 Buffer\_I/O pin\_name D1  |  DQS+        DQS

19 Buffer\_I/O pin\_name D2  |  DQS-        DQS

20 Pullup\_ref pin\_name A1  |  DQ1         DQ

21 Pullup\_ref pin\_name A2  |  DQ2         DQ

22 Pullup\_ref pin\_name A3  |  DQ3         DQ

23 Pullup\_ref pin\_name D1  |  DQS+        DQS

24 Pullup\_ref pin\_name D2  |  DQS-        DQS

25 Pulldown\_ref pin\_name A1  |  DQ1         DQ

26 Pulldown\_ref pin\_name A2  |  DQ2         DQ

27 Pulldown\_ref pin\_name A3  |  DQ3         DQ

28 Pulldown\_ref pin\_name D1  |  DQS+        DQS

29 Pulldown\_ref pin\_name D2 |  DQS+        DQS

[End Interconnect Model]

[End Interconnect Model Set]



Figure 51 – Electrical Connections for Full Buffer Pin Model with Power Routing



Figure 52 – Electrical Terminals for Full Buffer Pin Model with Power Routing

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 2: Same as Example 1 except the PDN networks are simplified with

| signal\_name qualifiers to create a pair of POWER terminals and a pair

| of GND terminals

[Interconnect Model Set] Full\_ISS\_PDN\_sn\_2

|-----

[Interconnect Model] Full\_ISS\_buf\_pin\_2

File\_IBIS-ISS full\_buf\_pin.iss full\_buf\_pin\_2\_typ

Number\_of\_terminals = 14

1  Pin\_I/O      pin\_name A1    |  DQ1         DQ

2  Pin\_I/O      pin\_name A2    |  DQ2         DQ

3  Pin\_I/O      pin\_name A3    |  DQ3         DQ

4  Pin\_I/O     pin\_name D1    |  DQS+        DQS

5  Pin\_I/O     pin\_name D2    |  DQS-        DQS

|

| POWER and GND terminals with signal\_names

|

6  Pin\_Rail    signal\_name  VDD   |  VDD         POWER

7  Pin\_Rail     signal\_name   VSS   |  VSS         GND

|

8  Buffer\_I/O pin\_name A1    |  DQ1         DQ

9  Buffer\_I/O pin\_name A2    |  DQ2         DQ

10 Buffer\_I/O pin\_name A3    |  DQ3         DQ

11 Buffer\_I/O pin\_name D1    |  DQS+        DQS

12 Buffer\_I/O pin\_name D2    |  DQS-        DQS

|

| POWER and GND terminals with signal\_names

|

13 Buffer\_Rail signal\_name   VDD   |  VDD         POWER

14 Buffer\_Rail signal\_name   VSS   |  VSS         GND

|

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 3: Single I/O Touchstone connection with one extra terminal for the

| N+1 .s2p reference connection terminal; [Interconnect Model Set] keyword

| stored in touchstone/ts\_sets.ims

[Interconnect Model Set] A1\_TS

|-----

[Interconnect Model] A1\_TS\_buf\_pin

File\_TS dq\_ts\_buf\_pin.s2p

Number\_of\_terminals = 3

1 Pin\_I/O      pin\_name A1

2 Buffer\_I/O pin\_name A1

3 Pulldown\_ref pin\_name A1 | VSS reference for .s2p file

 | Rail connections to Buffer\_I/O through

 | [Pin Mapping] or a [Model] reference

 | voltage used if no external rails

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 4: Single I/O pin documenting both IBIS-ISS and Touchstone files and

| showing that the File\_TS Touchstone N+1 reference connection is to the VSS

| rail

[Interconnect Model Set] A1\_TS\_pad\_pin

|-----

[Interconnect Model] A1\_TS\_pad\_pin

File\_TS dq\_ts\_pad\_pin.s2p

Number\_of\_terminals = 3

1 Pin\_I/O     pin\_name A1

2 Pad\_I/O     pin\_name A1

3 Pin\_Rail signal\_name VSS | VSS is reference for .s2p file

| | Requires Pin\_Rail VSS connection

[End Interconnect Model]

[End Interconnect Model Set]

[Interconnect Model Set] A1\_ISS\_buf\_pad

|-----

[Interconnect Model] A1\_ISS\_buf\_pad

File\_IBIS-ISS dq\_iss\_buf\_pad.iss DQ\_buf\_pad\_typ

Number\_of\_terminals = 3

1 Pad\_I/O      pin\_name A1

2 Buffer\_I/O pin\_name A1

3 Pulldown\_ref pin\_name A1

|

| [Pin Mapping] connections used to connect external rails; or default

| internal [Model] rails used if no external rails

|

[End Interconnect Model]

[End Interconnect Model Set]

| As an alternative formulation, the [Interconnect Model]s in two

| Interconnect Model Set]s could be combined into one [Interconnect Model

| Set] describing the full connection of A1 from buffer to pin

|

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 5: Full I/O IBIS-ISS configuration with PDN terminals in a separate

| [Interconnect Model Set]; when connected the individual Pin\_Rail

| terminals G1-G4 become shorted together with common VSS reference

[Interconnect Model Set] Full\_ISS\_buf\_pin\_IO\_1

|-----

[Interconnect Model] Full\_ISS\_buf\_pin\_IO

File\_IBIS-ISS full\_buf\_pin.iss full\_buf\_pin\_typ

Number\_of\_terminals = 13

1  Pin\_I/O      pin\_name A1  |  DQ1         DQ

2  Pin\_I/O      pin\_name A2  |  DQ2         DQ

3  Pin\_I/O      pin\_name A3  |  DQ3         DQ

4  Pin\_I/O      pin\_name D1  |  DQS+        DQS

5  Pin\_I/O      pin\_name D2  |  DQS-        DQS

6 Buffer\_I/O  pin\_name A1  |  DQ1         DQ

7 Buffer\_I/O  pin\_name A2  |  DQ2         DQ

8 Buffer\_I/O  pin\_name A3  |  DQ3         DQ

9 Buffer\_I/O  pin\_name D1  |  DQS+        DQS

10 Buffer\_I/O  pin\_name D2  |  DQS-        DQS

11 Pin\_Rail    signal\_name VSS | VSS         GND

[End Interconnect Model]

[End Interconnect Model Set]

[Interconnect Model Set] Full\_ISS\_buf\_pin\_PDN\_1

|-----

[Interconnect Model] Full\_ISS\_buf\_pin\_PDN\_1

File\_IBIS-ISS full\_ISS\_buf\_pin\_pdn.iss full\_buf\_pin\_PDN\_typ

Number\_of\_terminals = 19

1  Pin\_Rail    pin\_name P1  |  VDD         POWER

2 Pin\_Rail    pin\_name P2  |  VDD         POWER

3  Pin\_Rail    pin\_name P3  |  VDD         POWER

4  Pin\_Rail    pin\_name P4  |  VDD         POWER

5 Pin\_Rail    pin\_name P5  |  VDD         POWER

6 Pullup\_ref  pin\_name A1  |  DQ1         DQ

7 Pullup\_ref  pin\_name A2  |  DQ2         DQ

8 Pullup\_ref  pin\_name A3  |  DQ3         DQ

9 Pullup\_ref  pin\_name D1  |  DQS+        DQS

10 Pullup\_ref  pin\_name D2  |  DQS-        DQS

11 Pin\_Rail    pin\_name G1  |  VSS         GND

12 Pin\_Rail   pin\_name G2  |  VSS         GND

13 Pin\_Rail   pin\_name G3  |  VSS         GND

14 Pin\_Rail   pin\_name G4  |  VSS         GND

15 Pulldown\_ref pin\_name A1  |  DQ1         DQ

16 Pulldown\_ref pin\_name A2  |  DQ2         DQ

17 Pulldown\_ref pin\_name A3  |  DQ3         DQ

18 Pulldown\_ref pin\_name D1  |  DQS+        DQS

19 Pulldown\_ref pin\_name D2  |  DQS-        DQS

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 6: Full IBIS-ISS IOs and separate PDNs, all with buf\_pad and

| pad\_pin [Interconnect Model]s in separate [Interconnect Model]s

[Interconnect Model Set] Full\_ISS\_buf\_pad\_pin\_PDN\_4

|-----

[Interconnect Model] Full\_ISS\_pad\_pin\_IO

File\_IBIS-ISS full\_pad\_pin\_io.iss full\_pad\_pin\_IO\_typ

Number\_of\_terminals = 11

1  Pin\_I/O      pin\_name A1  |  DQ1         DQ

2  Pin\_I/O     pin\_name A2  |  DQ2         DQ

3  Pin\_I/O     pin\_name A3  |  DQ3         DQ

4  Pin\_I/O     pin\_name D1  |  DQS+        DQS

5  Pin\_I/O     pin\_name D2  |  DQS-        DQS

|

6 Pad\_I/O  pin\_name A1  |  DQ1         DQ

7 Pad\_I/O  pin\_name A2  |  DQ2         DQ

8 Pad\_I/O  pin\_name A3  |  DQ3         DQ

9 Pad\_I/O  pin\_name D1  |  DQS+        DQS

10 Pad\_I/O  pin\_name D2  |  DQS-        DQS

11 Pin\_Rail signal\_name VSS

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pad\_IO

File\_IBIS-ISS full\_buf\_pad\_io.iss full\_buf\_pad\_IO\_typ

Number\_of\_terminals = 11

1  Pad\_I/O      pin\_name A1  |  DQ1         DQ

2  Pad\_I/O      pin\_name A2  |  DQ2         DQ

3  Pad\_I/O      pin\_name A3  |  DQ3         DQ

4  Pad\_I/O     pin\_name D1  |  DQS+        DQS

5  Pad\_I/O      pin\_name D2  |  DQS-        DQS

|

6 Buffer\_I/O  pin\_name A1  |  DQ1         DQ

7 Buffer\_I/O  pin\_name A2  |  DQ2         DQ

8 Buffer\_I/O  pin\_name A3  |  DQ3         DQ

9 Buffer\_I/O  pin\_name D1  |  DQS+        DQS

10 Buffer\_I/O  pin\_name D2  |  DQS-        DQS

11 Buffer\_Rail signal\_name VSS

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_pad\_pin\_PDN

File\_IBIS-ISS full\_iss\_pad\_pin\_pdn.iss full\_iss\_pad\_pin\_PDN\_typ

Number\_of\_terminals = 14

1  Pin\_Rail pin\_name P1    |  VDD         POWER

2 Pin\_Rail pin\_name P2    |  VDD         POWER

3  Pin\_Rail pin\_name P3    |  VDD         POWER

4  Pin\_Rail pin\_name P4    |  VDD         POWER

5 Pin\_Rail pin\_name P5    |  VDD         POWER

|

6 Pad\_Rail pad\_name VDD1 |  VDD         POWER

7 Pad\_Rail pad\_name VDD2 |  VDD         POWER

8 Pad\_Rail pad\_name VDD3 |  VDD         POWER

|

9  Pin\_Rail pin\_name G1   |  VSS         GND

10 Pin\_Rail pin\_name G2   |  VSS         GND

11 Pin\_Rail pin\_name G3   |  VSS         GND

12 Pin\_Rail pin\_name G4   |  VSS         GND

|

13 Pad\_Rail pad\_name VSS1 |  VSS         GND

14 Pad\_Rail pad\_name VSS2 |  VSS         GND

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pad\_PDN

File\_IBIS-ISS full\_iss\_buf\_pad\_pdn.iss full\_iss\_buf\_pad\_PDN\_typ

Number\_of\_terminals = 15

1 Pad\_Rail pad\_name VDD1 |  VDD         POWER

2 Pad\_Rail pad\_name VDD2 |  VDD         POWER

3 Pad\_Rail pad\_name VDD3 |  VDD         POWER

|

4 Pullup\_ref  pin\_name A1   |  DQ1         DQ

5 Pullup\_ref  pin\_name A2   |  DQ2         DQ

6 Pullup\_ref  pin\_name A3   |  DQ3         DQ

7 Pullup\_ref  pin\_name D1   |  DQS+        DQS

8 Pullup\_ref  pin\_name D2   |  DQS-        DQS

|

9 Pad\_Rail pad\_name VSS1 |  VSS         GND

10 Pad\_Rail pad\_name VSS2 |  VSS         GND

|

11 Pulldown\_ref pin\_name A1   |  DQ1         DQ

12 Pulldown\_ref pin\_name A2   |  DQ2         DQ

13 Pulldown\_ref pin\_name A3   |  DQ3         DQ

14 Pulldown\_ref pin\_name D1    |  DQS+        DQS

15 Pulldown\_ref pin\_name D2    |  DQS-        DQS

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 7: Full IBIS-ISS model with I/O only [Interconnect Model] and a

| separate PDN [Interconnect Model] with signal\_name qualifiers

[Interconnect Model Set] Full\_ISS\_PDN\_sn\_5

|-----

[Interconnect Model] Full\_ISS\_buf\_pin\_IO

File\_IBIS-ISS full\_buf\_pin.iss full\_buf\_pin\_typ

Number\_of\_terminals = 11

1 Pin\_I/O pin\_name A1 | DQ1 DQ

2 Pin\_I/O pin\_name A2 | DQ2 DQ

3 Pin\_I/O pin\_name A3 | DQ3 DQ

4 Pin\_I/O pin\_name D1 | DQS+ DQS

5 Pin\_I/O pin\_name D2 | DQS- DQS

6 Buffer\_I/O pin\_name A1 | DQ1 DQ

7 Buffer\_I/O pin\_name A2 | DQ2 DQ

8 Buffer\_I/O pin\_name A3 | DQ3 DQ

9 Buffer\_I/O pin\_name D1 | DQS+ DQS

10 Buffer\_I/O pin\_name D2 | DQS- DQS

11 Pin\_Rail signal\_name VSS

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pin\_PDN\_2

File\_IBIS-ISS full\_iss\_buf\_pin\_pdn\_2.iss full\_iss\_buf\_pad\_PDN\_2

Number\_of\_terminals = 4

1  Pin\_Rail     signal\_name VDD  |  VDD         POWER

2 Buffer\_Rail signal\_name VDD  | VDD         POWER

3  Pin\_Rail     signal\_name VSS  |  VSS         GND

4 Buffer\_Rail signal\_name VSS  |  VSS         GND

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 8: Same full IBIS-ISS model with PDN as in Example 7, but with the

| [Interconnect Model]s describing buf\_pad and pad\_pin connections

| separately

[Interconnect Model Set] Full\_ISS\_buf\_pad\_pin\_PDN\_sn\_6

|-----

[Interconnect Model] Full\_ISS\_pad\_pin\_IO

File\_IBIS-ISS full\_pad\_pin\_io.iss full\_pad\_pin\_IO\_typ

Number\_of\_terminals = 11

1 Pin\_I/O pin\_name A1 | DQ1 DQ

2 Pin\_I/O pin\_name A2 | DQ2 DQ

3 Pin\_I/O pin\_name A3 | DQ3 DQ

4 Pin\_I/O pin\_name D1 | DQS+ DQS

5 Pin\_I/O pin\_name D2 | DQS- DQS

|

6 Pad\_I/O pin\_name A1 | DQ1 DQ

7 Pad\_I/O pin\_name A2 | DQ2 DQ

8 Pad\_I/O pin\_name A3 | DQ3 DQ

9 Pad\_I/O pin\_name D1 | DQS+ DQS

10 Pad\_I/O pin\_name D2 | DQS- DQS

11 Buffer\_Rail signal\_name VSS

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pad\_IO

File\_IBIS-ISS full\_buf\_pad\_io.iss full\_buf\_pad\_IO\_typ

Number\_of\_terminals = 11

1 Pad\_I/O pin\_name A1 | DQ1 DQ

2 Pad\_I/O pin\_name A2 | DQ2 DQ

3 Pad\_I/O pin\_name A3 | DQ3 DQ

4 Pad\_I/O pin\_name D1 | DQS+ DQS

5 Pad\_I/O pin\_name D2 | DQS- DQS

|

6 Buffer\_I/O pin\_name A1 | DQ1 DQ

7 Buffer\_I/O pin\_name A2 | DQ2 DQ

8 Buffer\_I/O pin\_name A3 | DQ3 DQ

9 Buffer\_I/O pin\_name D1 | DQS+ DQS

10 Buffer\_I/O pin\_name D2 | DQS- DQS

11 Pin\_Rail signal\_name VSS

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_pad\_pin\_PDN\_3

File\_IBIS-ISS full\_iss\_pad\_pin\_pdn\_3.iss full\_iss\_pad\_pin\_pdn\_3

Number\_of\_terminals = 4

1  Pin\_Rail     signal\_name VDD  |  VDD         POWER

2 Pad\_Rail     signal\_name VDD  |  VDD         POWER

3  Pin\_Rail     signal\_name VSS  |  VSS         GND

4 Pad\_Rail     signal\_name VSS  |  VSS         GND

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pad\_PDN\_3

File\_IBIS-ISS full\_iss\_buf\_pad\_pdn\_3.iss full\_iss\_buf\_pad\_pdn\_3

Number\_of\_terminals = 4

1  Buffer\_Rail  signal\_name VDD  |  VDD         POWER

2 Pad\_Rail     signal\_name VDD  |  VDD         POWER

3  Buffer\_Rail  signal\_name VSS  |  VSS         GND

4 Pad\_Rail     signal\_name VSS  |  VSS         GND

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 9: Same full IBIS-ISS configuration with PDN as in Example 8, except

| that I/O connections are direct from buf\_pin while the PDN connections are

| from buf\_pad and pad\_pin using the signal\_name qualifier

[Interconnect Model Set] Full\_ISS\_IO\_buf\_pad\_pin\_PDN\_sn\_7

|-----

[Interconnect Model] Full\_ISS\_buf\_pin\_IO

File\_IBIS-ISS full\_buf\_pin.iss full\_buf\_pin\_typ

Number\_of\_terminals = 11

1 Pin\_I/O pin\_name A1 | DQ1 DQ

2 Pin\_I/O pin\_name A2 | DQ2 DQ

3 Pin\_I/O pin\_name A3 | DQ3 DQ

4 Pin\_I/O pin\_name D1 | DQS+ DQS

5 Pin\_I/O pin\_name D2 | DQS- DQS

6 Buffer\_I/O pin\_name A1 | DQ1 DQ

7 Buffer\_I/O pin\_name A2 | DQ2 DQ

8 Buffer\_I/O pin\_name A3 | DQ3 DQ

9 Buffer\_I/O pin\_name D1 | DQS+ DQS

10 Buffer\_I/O pin\_name D2 | DQS- DQS

11 Pin\_Rail signal\_name VSS

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_pad\_pin\_PDN\_3

File\_IBIS-ISS full\_iss\_pad\_pin\_pdn\_3.iss full\_iss\_pad\_pin\_pdn\_3

Number\_of\_terminals = 4

1 Pin\_Rail signal\_name VDD | VDD POWER

2 Pad\_Rail signal\_name VDD | VDD POWER

3 Pin\_Rail signal\_name VSS | VSS GND

4 Pad\_Rail signal\_name VSS | VSS GND

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pad\_PDN\_3

File\_IBIS-ISS full\_iss\_buf\_pad\_pdn\_3.iss full\_iss\_buf\_pad\_pdn\_3

Number\_of\_terminals = 4

1 Buffer\_Rail signal\_name VDD | VDD POWER

2 Pad\_Rail signal\_name VDD | VDD POWER

3 Buffer\_Rail signal\_name VSS | VSS GND

4 Pad\_Rail signal\_name VSS | VSS GND

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 10: Terminals A1\_A3 set up for and IBIS-ISS connections with coupling

| for cross-talk analysis – Aggressor\_Only terminals at the Buffer are

| designated

[Interconnect Model Set] A1\_A3\_DQ\_TS\_XTALK

|-----

[Interconnect Model] A1\_A3\_DQ\_TS\_buf\_pin\_XTALK

File\_TS dq\_buf\_pin\_xtalk.s6p

Number\_of\_terminals = 7

1 Pin\_I/O     pin\_name A1 Aggressor\_Only

2 Buffer\_I/O pin\_name A1 Aggressor\_Only

3 Pin\_I/O     pin\_name A2

4 Buffer\_I/O pin\_name A2

5 Pin\_I/O     pin\_name A3 Aggressor\_Only

6 Buffer\_I/O pin\_name A3 Aggressor\_Only

7 Pulldown\_ref pin\_name A1

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 11: Same as Example 10, but with a PDN network added

[Interconnect Model Set] A1\_A3\_DQ\_TS\_XTALK\_ISS\_PDN

|-----

[Interconnect Model] A1\_A3\_DQ\_TS\_buf\_pin\_XTALK

File\_TS dq\_buf\_pin\_xtalk.s6p

Number\_of\_terminals = 7

1 Pin\_I/O pin\_name A1 Aggressor\_Only

2 Buffer\_I/O pin\_name A1 Aggressor\_Only

3 Pin\_I/O pin\_name A2

4 Buffer\_I/O pin\_name A2

5 Pin\_I/O pin\_name A3 Aggressor\_Only

6 Buffer\_I/O pin\_name A3 Aggressor\_Only

7 Pulldown\_ref pin\_name A1

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pin\_PDN\_2

File\_IBIS-ISS full\_iss\_buf\_pin\_pdn\_2.iss full\_iss\_buf\_pad\_PDN\_2

Number\_of\_terminals = 4

1 Pin\_Rail signal\_name VDD | VDD POWER

2 Buffer\_Rail signal\_name VDD | VDD POWER

3 Pin\_Rail signal\_name VSS | VSS GND

4 Buffer\_Rail signal\_name VSS | VSS GND

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Examples 12 and 13 apply to the configuration below

[Pin] signal\_name model\_name      R\_pin   L\_pin   C\_pin

A1    DQ1         DQ

A2    DQ2         DQ

A3    DQ3         DQ

A4    DQ4         DQ

P1    VDD         POWER

P2    VDD         POWER

G1    VSS         GND

G2    VSS         GND

[Bus Label] signal\_name

VDD1 VDD

VDD2 VDD

[Pin Mapping] pulldown\_ref pullup\_ref gnd\_clamp\_ref power\_clamp\_ref ext\_ref

A1            VSS           VDD1        NC            NC              NC

A2            VSS           VDD1        NC            NC              NC

A3            VSS           VDD2        NC            NC              NC

A4            VSS           VDD2        NC            NC              NC

| Entries below may optionally be deleted and replaced with [Bus Label] per

| [Bus Label] and [Pin Mapping] rules

P1            NC           VDD1        NC            NC              NC

P2            NC           VDD2        NC            NC              NC

G1            VSS           NC         NC            NC              NC

G2            VSS           NC         NC            NC              NC

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 12: Full IBIS-ISS configuration with PDN described using both

| bus\_label and signal\_name qualifiers for the Rails

[Interconnect Model Set] Full\_ISS\_IO\_PDN\_bl\_sn\_6

|-----

[Interconnect Model] Full\_ISS\_buf\_pin\_IO\_4

File\_IBIS-ISS full\_iss\_buf\_pin\_io\_4.iss full\_iss\_buf\_pin\_IO\_4\_typ

Number\_of\_terminals = 9

1  Pin\_I/O     pin\_name A1  |  DQ1         DQ

2  Pin\_I/O      pin\_name A2  |  DQ2         DQ

3  Pin\_I/O     pin\_name A3  |  DQ3         DQ

4  Pin\_I/O     pin\_name A4  |  DQ4         DQ

5 Buffer\_I/O pin\_name A1  |  DQ1         DQ

6 Buffer\_I/O pin\_name A2  |  DQ2         DQ

7 Buffer\_I/O pin\_name A3  |  DQ3         DQ

8 Buffer\_I/O pin\_name A4  |  DQ4         DQ

9 Pin\_Rail signal\_name VSS

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_PDN\_bl\_sn

File\_IBIS-ISS buf\_pin\_pdn.iss buf\_pin\_PDN\_typ

Number\_of\_terminals = 5

1  Pin\_Rail     signal\_name VDD  |  VDD         POWER

2  Pin\_Rail     signal\_name VSS  |  VSS         GND

|

3 Buffer\_Rail bus\_label VDD1  |  VDD         POWER

4 Buffer\_Rail bus\_label VDD2  |  VDD         POWER

5 Buffer\_Rail signal\_name VSS  |  VSS         GND

[End Interconnect Model]

[End Interconnect Model Set]

| The EDA tool connects the terminals and pins as follows:

|

| 1 Pins P1 and P2

| 2 Pins G1 and G2

| 3 Pullup\_ref of buffers A1 and A2

| 4 Pullup\_ref of buffers A3 and A4

| 5 Pulldown\_ref of buffers A1, A2, A3 and A4

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 13: Same as Example 12, but adds decoupling capacitors at the buffer

| interface in separate Interconnect Models to show how single-interface

| Interconnect Models with rail-only terminals can be used

[Interconnect Model Set] Full\_ISS\_IO\_PDN\_bl\_sn\_7

|-----

[Interconnect Model] Full\_ISS\_buf\_pin\_IO\_4

File\_IBIS-ISS full\_iss\_buf\_pin\_io\_4.iss full\_iss\_buf\_pin\_IO\_4\_typ

Number\_of\_terminals = 9

1  Pin\_I/O     pin\_name A1  |  DQ1         DQ

2  Pin\_I/O      pin\_name A2  |  DQ2         DQ

3  Pin\_I/O     pin\_name A3  |  DQ3         DQ

4  Pin\_I/O     pin\_name A4  |  DQ4         DQ

5 Buffer\_I/O pin\_name A1  |  DQ1         DQ

6 Buffer\_I/O pin\_name A2  |  DQ2         DQ

7 Buffer\_I/O pin\_name A3  |  DQ3         DQ

8 Buffer\_I/O pin\_name A4  |  DQ4         DQ

9 Pin\_Rail signal\_name VSS

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_PDN\_bl\_sn

File\_IBIS-ISS buf\_pin\_pdn.iss buf\_pin\_PDN\_typ

Number\_of\_terminals = 5

1  Pin\_Rail     signal\_name VDD  |  VDD         POWER

2  Pin\_Rail     signal\_name VSS  |  VSS         GND

|

3 Buffer\_Rail bus\_label VDD1  |  VDD         POWER

4 Buffer\_Rail bus\_label VDD2  |  VDD         POWER

5 Buffer\_Rail signal\_name VSS  |  VSS         GND

[End Interconnect Model]

[Interconnect Model] Decap1

File\_IBIS-ISS buf\_pin\_pdn.iss single\_decoupling\_cap\_model

Number\_of\_terminals = 2

1 Buffer\_Rail bus\_label VDD1  |  VDD         POWER

2 Buffer\_Rail signal\_name VSS  |  VSS         GND

[End Interconnect Model]

[Interconnect Model] Decap2

File\_IBIS-ISS buf\_pin\_pdn.iss single\_decoupling\_cap\_model

Number\_of\_terminals = 2

1 Buffer\_Rail bus\_label VDD2  |  VDD         POWER

2 Buffer\_Rail signal\_name VSS  |  VSS         GND

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 14: Full IBIS-ISS configuration with I/Os (and no PDN) and using

| A\_gnd to connect some I/O terminals and the VSS terminal to the simulator

| global reference node.

|

| A\_gnd is used to connect the VSS subcircuit terminal located as its

| first terminal to the simulator global reference, and A\_gnd is also used to

| connect some I/O terminals (3 and 7) to the simulator global reference.

[Interconnect Model Set] Full\_ISS\_IO\_with\_A\_gnd

|-----

[Interconnect Model] Full\_ISS\_IO\_A\_gnd

File\_IBIS-ISS full\_iss\_buf\_pin\_io\_4.iss full\_iss\_buf\_pin\_IO\_4\_A\_gnd\_typ

Number\_of\_terminals = 9

1 A\_gnd | VSS terminal connected to simulator

| global reference

2 Pin\_I/O pin\_name A1 | DQ1 DQ

3 A\_gnd | DQ2 DQ A2 connected to

| simulator global reference

4 Pin\_I/O pin\_name A3 | DQ3 DQ

5 Pin\_I/O pin\_name A4 | DQ4 DQ

6 Buffer\_I/O pin\_name A1 | DQ1 DQ

7 A\_gnd | DQ2 DQ A2 connected to

| simulator global reference

8 Buffer\_I/O pin\_name A3 | DQ3 DQ

9 Buffer\_I/O pin\_name A4 | DQ4 DQ

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 15: Full Touchstone configuration with I/Os and A\_gnd reference,

| but without any PDN.

|

| A\_gnd can be used only at the N+1th terminal number as a reference.

[Interconnect Model Set] Full\_TS\_IO\_A\_gnd\_reference

|-----

[Interconnect Model] Full\_TS\_IO\_A\_gnd\_reference

File\_TS full\_ts\_buf\_pin\_io.s8p

Number\_of\_terminals = 9

Full\_TS\_IO\_A\_gnd\_reference

1 Pin\_I/O pin\_name A1 | DQ1 DQ

2 Pin\_I/O pin\_name A2 | DQ2 DQ

3 Pin\_I/O pin\_name A3 | DQ3 DQ

4 Pin\_I/O pin\_name A4 | DQ4 DQ

5 Buffer\_I/O pin\_name A1 | DQ1 DQ

6 Buffer\_I/O pin\_name A2 | DQ2 DQ

7 Buffer\_I/O pin\_name A3 | DQ3 DQ

8 Buffer\_I/O pin\_name A4 | DQ4 DQ

9 A\_gnd | Reference terminal connected to

 | simulator global reference

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

*Keyword:* [**End Interconnect Model**]

*Required:* Yes, for each instance of the [Interconnect Model] keyword

*Description:* Indicates the end of the Interconnect Model data.

*Example:*

[End Interconnect Model]