**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER:** 189.3

**ISSUE TITLE:** *Interconnect Modeling Using IBIS-ISS and Touchstone*

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**DATE SUBMITTED:** January 27, 2017

**DATE REVISED:** March 29, 2017; April 19, 2017; April 26, 2017

**DATE ACCEPTED:**

**STATEMENT OF THE ISSUE:**

This BIRD enhances IBIS with interconnect modeling features to support broadband, coupled package, and on-die interconnect using IBIS-ISS and Touchstone data.

The BIRD also adds a keyword for buffer rail mapping, to link to new terminal definitions defined for buffers.

**ANALYSIS PATH/DATA THAT LED TO SPECIFICATION:**

This BIRD has resulted from several years of discussion regarding the need for more flexible description of interconnects in IBIS. It was decided to avoid a keyword-based approach, in favor of a circuit language approach. IBIS-ISS was developed for this purpose, and a means to instantiate IBIS-ISS models from IBIS became the logical next step.

**SOLUTION REQUIREMENTS:**

The IBIS specification must meet these requirements:

Table : Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| 1. The model maker must be able to provide interconnect models representing die and package, using a combination of IBIS-ISS and Touchstone formats. | Might replace BIRD 125.1 |
| 1. Touchstone models without an IBIS-ISS wrapper circuit must be supported. | Might replace BIRD 158.1 |
| 1. An interconnect model may connect buffers to pins directly or separate models may be used for the buffer to pad and pad to pin connections (die and package portions). | Die is buffer to pad. Package is pad to pin. |
| 1. An interconnect model may connect one pin or any combination of pins on one [Component]. | Coupled models are supported. |
| 1. The buffer I/O, pad, and pin terminals associated with I/O pins must be assignable to interconnect model terminals directly by pin name. |  |
| 1. The buffer supply, pad, and pin terminals associated with POWER and GND rail pins must be assignable to interconnect model terminals directly by pin name, or indirectly by [Pin] signal\_name or [Pin Mapping] bus\_label. |  |
| 1. The model maker must be able to provide alternative interconnect models for any given set of pins. | For example for a given pin pair it must be possible to provide both coupled and uncoupled models, high and low bandwidth models, or both IBIS-ISS and Touchstone models. |
| 1. The model maker may use new interconnect models for some pins and legacy package models for other pins. |  |
| 1. The model user must be able, given a pin or set of pins it must analyze, to locate all interconnect models that include the pin(s), if any. | Simulation netlisting begins with a list of pins that must be simulated. |
| 1. The model user must be able to determine all of the pins that a given interconnect model includes. | Once a model is chosen, it may add more pins to the simulation. |
| 1. The model user must be able to determine how to terminate any terminals of an interconnect model not necessary for a particular analysis. | May need to handle s-parameter and circuit models differently. |
| 1. For any pin having an interconnect model, models encompassing the full path from buffer to pin must be present and identifiable by the user. |  |
| 1. The model user must have useful information needed to make the choice between alternative interconnect models that differ only in characteristics other than the model format and the set of pins included. | For example: coupled/uncoupled, low/high bandwidth. This will be used to choose which alternative model set to use. |
| 1. The order of precedence for new interconnect models and legacy forms of package models must be specified. | Probably will take precedence over [Package Model], [Pin] RLC, and [Package]. |
| 1. The model user must not be required to use both new interconnect and legacy package models to model any single pin or coupled set of pins of a [Component]. | For example, can’t use [Pin] RLC for through path and IBIS-ISS for coupling. |
| 1. The model user must be informed which pins of an interconnect model have been modeled with coupling to other pins, sufficient for the former to represent the victim pins and the latter all of the aggressor pins in a crosstalk simulation. | Pins near one “end” of the model will be coupled to pins on one side but probably not enough pins on the other side. |

**BACKGROUND INFORMATION/HISTORY:**

This BIRD was originally submitted to the IBIS Interconnect Task Group by Walter Katz in April, 2014. Subsequent revisions were created and reviewed in the Interconnect Task Group with contributions from Radek Biernacki, Justin Butterfield, Curtis Clark, Mike LaBonte, Arpad Muranyi, Michael Mirmak, Bob Ross, and Randy Wolff.

Parameter is shortened to Param (.param is legal in IBIS-ISS) to differentiate it further from Parameters in the multi-lingual syntax (Parameter has several meanings in IBIS and the Algorithmic Modeling Interface.)

File\_names are not quoted, to be consistent with Corner in the multi-lingual syntax. Multiple file names for corners are not supported here, however.

Entries for strings in Param are surrounded by double quotes to be consistent with string\_literal Parameters in the multi-lingual syntax (or where the AMI string\_literal parameter surrounded by double quotes is passed into the multi-lingual Parameters reference). The EDA tool needs to convert string\_literals into the parameter string syntax in IBIS-ISS.

Interaction of Param entries was not discussed. For example, for a transmission line, TD and Z0 could each have max and min entries, but the EDA tool could make available combinations of min/min, min/max, max/min or max/max for any corner. Due to parameter interactions, some mixing of corner combinations might not be realistic. (E.g., Z0min or Z0max might not correlate with TDmin or TDmax values, where TDmin=sqrt(LminCmin), Z0min=sqrt(Lmin/Cmax), etc.).

How corners of File\_IBIS-ISS and Params are processed might be based on vendor supplied documentation. For example some, but not all, combinations are shown below:

1. One file\_name for all corners, one .subckt name, and all corner settings controlled by Param settings
2. One file\_name, three .subckts (with internal default .param settings), additional corner settings controlled by Param settings or Param is not used
3. Three file\_names with the same .subckt name, but with distinct default .param settings, additional settings controlled by Param settings or Param is not used
4. Three file\_names with three distinct .subckt name and with distinct default .param settings, additional corner settings controlled by Param settings or Param is not used

No interpretation is given for Param typ, min, and max values. It is possible to independently use typ, min, or max values for any of the Param names that have been defined (e.g., the max value of one parameter may be used with the min value of another parameter).

Some concern has been noted that EDA tools may not be able to clearly define a complete interconnect path from separate Interconnect Models that specify only part of the electrical path. While several methods to do this are possible, an example flow for an EDA tool to assemble a complete interconnect path from separate Interconnect Models is as follows:

1. Read in the list of I/O buffers; this must contain:
   1. Pin\_I/O nodes
   2. Buffer\_I/O nodes
   3. Buffer\_Rail nodes; this also defines the respective rail attributes, including:
      1. Signal\_names
      2. Bus\_labels
      3. Rail pin\_names
2. Search models to find the smallest number of models that contain all Buffer\_I/O (this is List A)
   1. If List A contains all Pin\_I/O then
      1. Done with I/O
   2. Else search models to find the smallest number of models that contain the Pad\_I/O and Pin\_I/O that are missing in List A (this is List B)
3. If a power delivery network model is required
   1. If the models in List A and List B have connections to all Buffer\_Rail terminals and pins for each of the signal names in the Buffer\_Rail list, then
      1. Done with PDN
   2. Else search models that contain the Pad\_Rail and Pin\_Rail that are missing in List A and List B (this is List C)
4. Verify that no pin or buffer terminal is connected to two or more models
5. Verify that all pin and buffer I/O terminals are connected to a single interconnect model terminal
6. If a power delivery network is defined then
   1. Verify that all Buffer\_Rail terminals are connected to a single interconnect model terminal
   2. Verify that there is at least one Pin\_Rail terminal with a signal\_name defined in 3.a

The user may direct the EDA tool to use models from all of the available interconnect model sets, or from only a subset of the interconnect model sets.

The BIRD was submitted to the IBIS Open Forum January 27, 2017.

BIRD189.1 was created to correct several minor editorial issues, to clarify Unused\_port\_termination rules and the meaning of Aggressor\_Only, to remove a figure, and to update three other figures for clarity.

BIRD189.2 was created to update the list of authors, to correct the capitalization of “Aggressor\_Only”, to selectively change “IO” to “I/O”, and to change “Buf\_I/O” to “Buffer\_I/O” and “Buf\_Rail” to “Buffer\_Rail” (with appropriate re-formatting for the longer strings) to better match usage elsewhere in IBIS. A clarification of the meaning of “I/O” in the context of terminals was also added.

BIRD189.3 was created to correct a Param example, and to change “filename” to “base name” in the .ims file rules, for consistency with BIRD186.

**PROPOSED CHANGES:**

The following keyword should be added to Chapter 5, COMPONENT DESCRIPTION, after the [Alternate Package Models] keyword:

*Keyword:* [Interconnect Model Set Selector]

*Required:* No

*Description:* Used to list by name the [Interconnect Model Set] keywords available for the [Component].

*Usage Rules:* Interconnect Model Sets contain Interconnect Models used to describe pin, die pad or buffer terminal connections to IBIS-ISS subcircuits or Touchstone files.

A [Component] may have zero, one, or more than one [Interconnect Model Set] keywords (identified by a name) associated with it. All Interconnect Model Sets exist for the component shall be listed in this section. An Interconnect Model Set Selector is required even if there is only one Interconnect Model Set. If there are no Interconnect Model Sets, the [Interconnect Model Set Selector] keyword is illegal. The [Interconnect Model Set Selector] is hierarchically within the scope of the [Component] keyword.

The section under the [Interconnect Model Set Selector] keyword shall have two entries per line, with each line identifying one Interconnect Model Set associated with the component. The entries shall be separated by at least one white space. The first entry lists the Interconnect Model Set name (up to 40 characters long). The second entry is the name of the file containing the Interconnect Model Set, with the extension “ims”. If the Interconnect Model Set is in the same IBIS file as [Component], then the second entry shall be “NA”.

The files containing the Interconnect Model Sets with the ibs extension shall be located in the same directory as the .ibs file or in a directory under the .ibs file as determined by the directory path according to the file name rules given in Section 3, ’GENERAL SYNTAX RULES AND GUIDELINES’. An [Interconnect Model Set] with matching name shall be found in the stated location for each Interconnect Model Set named in the [Interconnect Model Set Selector].

Each Interconnect Model Set name may only appear once under the [Interconnect Model Set Selector] keyword for a given component.

*Example:*

[Interconnect Model Set Selector]

All\_pins\_iss NA | An [Interconnect Model Set] is

| present in the .ibs file

All\_pins\_touchstone 8\_pin\_s16p.ims | The [Interconnect Model Set] is

| stored in a separate .ims file

[End Interconnect Model Set Selector]

*Keyword:* [**End Interconnect Model Set Selector**]

*Required:* Yes, for each instance of the [Interconnect Model Set Selector] keyword

*Description:* Indicates the end of the data for one [Interconnect Model Set Selector].

*Example:*

[End Interconnect Model Set Selector]

The following keywords should be placed in section 5, COMPONENT DESCRIPTION, after the [Pin Mapping] keyword.

Keyword: [Bus Label]

*Required:* No

*Description:* Associates a POWER or GND signal\_name with one or more bus\_label names within a Component. The bus\_label names can be used to define terminals at the buffer, die pad or pin interfaces.

*Sub-Params:* signal\_name

*Usage Rules:* The first column shall contain a bus\_label. The second column, signal\_name, shall be a corresponding signal\_name entry for a pin under the [Pin] keyword that uses the model\_name POWER or GND.

The [Bus Label] keyword shall be followed by the string “signal\_name” as a column heading.

Duplicate bus\_labels are not permitted. A bus\_label may be defined also by the [Pin Mapping] keyword.

Column length limits are:

[Bus Label] 15 characters max

signal\_name 40 characters max

*Example:*

[Bus Label] signal\_name

VDD1 VDD

VDD2 VDD

VDD3 VDD

VSS1 VSS

VSS2 VSS

*Keyword:* **[Die Supply Pads]**

*Required:* No

*Description:* Associates signal\_names and bus\_labels to die pads connected to supply rails.

*Sub-Params:* signal\_name, bus\_label

*Usage Rules:*  Only die pads with signal\_names that occur on POWER or GND pins are allowed. Each line shall contain either two or three columns. The first column shall contain the supply die pad name (the column entry is also referred to as “pad\_name” elsewhere in this document). The second column, signal\_name, shall contain the signal name as given under the [Pin] keyword. The third column is optional. If it exists, it is a bus\_label. If the third column does not exist, then the bus\_label shall be the signal\_name.

The [Die Supply Pads] keyword shall be followed by the strings “signal\_name” and “bus\_label” as column headings.

*Other Notes:* The data in this section consists of a list of pad\_names and their corresponding signal\_names and bus\_labels, which can be used to mate package and on-die power delivery networks.

*Example:*

[Die Supply Pads] signal\_name bus\_label

VDDQ VDDQ

VDD1 VDD VDDa

VDD2 VDD VDDa

VDD3 VDD VDDb

VSS1 VSS

VSS2 VSS

The following text should be added at the beginning of Chapter 7, PACKAGE MODELING, after the chapter title.

**7.1 INTRODUCTION**

Several package modeling formats are available in IBIS. These include:

1. Lumped [Component]-level models for the entire [Component], using the [Package] keyword.
2. Lumped [Component]-level modeling per-pin, using the [Pin] keyword.
3. [Package Model] (including [Alternate Package Models] and [Define Package Model]).
4. [Interconnect Model Set Selector] and the keywords associated with it.

The lumped formats are described in the [Package] and [Pin] keyword definitions in Chapter 5. Keywords for use with the [Package Model] format are described in this chapter, while keywords for use with [Interconnect Model Set Selector] are described in Chapter 12.

**7.2 RULES OF PRECEDENCE**

The order of precedence for package model data to be used by EDA tools in simulation is defined below, in ascending order. If a package data format at a numerically higher position on the list is available in an IBIS or related file, that data shall be considered by the EDA tool to be more detailed and is therefore preferred.

1. [Component]/[Package]
2. [Component]/[Pin]
3. [Package Model] (including [Alternate Package Models] and [Define Package Model])
4. [Interconnect Model Set Selector]

Note that [External Circuit] and [Interconnect Model Set Selector] shall not be present within the same [Component]. [Package Model] and [Interconnect Model Set Selector] may both be present for the same [Component] but should not both be used at the same time,

**7.3 KEYWORDS FOR USE WITH [PACKAGE MODEL]**

The following new Chapter 12 should be added after Chapter 11.

**12 INTERCONNECT MODELING**

**12.1 INTRODUCTION**

IBIS supports broadband interconnect models describing connections between the pins of a component and its I/O buffers. These interconnect models may include descriptions of interconnect coupling and/or interconnect rail distributions.

Interconnect is defined between up to three nodes, referred to here as “terminals”:

* pin interface (also called pin), where a component connects to a printed circuit board
* die pad interface, where a component silicon die connects to the routing on a package substrate
* buffer interface, where the buffer itself connects to the silicon die substrate and routing

The relationship between the terminals at the buffer interface, die pad interface, and pins is shown in the figure below.



Figure 47 – Example Interconnect Model Structure

The connection between the pin and die pad interface is generally called “package interconnect”, while the connection between the die pad interface and the buffer interface is generally called “on-die interconnect.” The die pad is distinct from the buffer interface; the buffer includes the circuitry that would be described through the [Model] keyword and related keywords, and would not include transmission line behavior.

Interconnect models may be supplied separately for on-die interconnect and package interconnect, or may be supplied as a single model for the entire connection between the package pins and buffers.

The electrical behavior of an interconnect is described through either IBIS-ISS SPICE subcircuits or Touchstone network parameters. An [Interconnect Model] defines the connections to either an IBIS-ISS SPICE subcircuit or a Touchstone file. An [Interconnect Model] may describe the connection between the pins of the package and the buffers, the pins of the package and the die pads, or the die pads and buffers.

[Interconnect Model]s are organized into [Interconnect Model Set]s. An [Interconnect Model Set] consists of one or more [Interconnect Model]s. One [Interconnect Model Set] may contain groups of similar interconnect models or different interconnect models to describe the complete connections from the buffer to pin interface. These may include:

* Uncoupled I/O connections
* Coupled I/O connections
* Rail connections
* Uncoupled or coupled IBIS-ISS connections
* Uncoupled or coupled Touchstone file connections
* Combinations of the above

Each I/O pin is associated with one I/O buffer terminal and optionally one I/O die pad. By contrast, there is no required one-to-one relationship between rail pins, (optional) rail die pads, and buffer rail terminals.

Figure 48 below shows the [Interconnect Model] terminals for an I/O path on both package and on-die substrates.



Figure 48 – Package Substrate I/O Paths

The figure also shows on-die interconnect routes that may experience crosstalk effects. This example assumes that only a few routes out of a larger bus are shown. In such a model, the crosstalk on any one route *in the model* could only be caused by its nearest neighbors.

While each of the inner two routes in the figure may have all potential crosstalk represented in the model, the outer signals would not. The model maker would therefore indicate that connections to the outer routes’ terminals do not include all of their aggressors by adding the optional argument “Aggressor\_Only” to their terminals. The descriptions of the associated Terminals would not use the “Aggressor\_Only” designation for the inner routes. The EDA tool may therefore assume in simulation that the inner routes have all (or more practically most of) the coupling to their aggressor connections represented in the model.

Crosstalk simulations require Interconnect Models to have connections to multiple I/O pin\_names.

Figure 49 of a package and die shows graphically the potential [Interconnect Model] terminals for a rail connection. A single pin terminal for a supply rail connects to multiple die pads. Note that these terminals may be collapsed to a single terminal at the pin (as shown), or alternately at the die pad interface and/or the buffer rail terminals.



Figure 49 – Package Substrate Rail Terminals

The terminal section of an [Interconnect Model] describes how the terminals of an Interconnect Model subcircuit or Touchstone file instance are connected at a buffer terminal, die pad interface or pin/board interface.

**12.2 GENERAL INTERCONNECT SYNTAX REQUIREMENTS**

Terminal lines under the [Interconnect Model] keyword describe connections.

I/O terminals shall be connected using only the pin\_name qualifier at these locations:

* pins: I/O pin\_name
* die pads: I/O pin\_name
* buffer: I/O pin\_name

Rail terminal connections have more options to support direct connections to terminals or to groups of terminals using signal\_name, bus\_label, or pad\_name entries at the pin, die pad or buffer locations. For the following locations the rail terminal can connect to:

* pins
* a specific rail pin\_name
* all of the pins of a rail signal\_name
* all of the pins of a bus\_label
* die pads
* all of the die pads with a rail signal\_name
* all of the die pads with a rail bus\_label
* a specific die pad pad\_name
* buffer rail terminals
* all of the buffer rail terminals of a rail signal\_name
* all of the buffer rail terminals of a bus\_label
* a specific buffer rail terminal for an I/O buffer pin\_name

One or more Interconnect Model Sets may be included in a separate Interconnect Model Set file, with the extension “ims” or within the .ibs file where [Interconnect Model Set Selector] is used. The [Interconnect Model Set] keyword can contain the optional [Manufacturer] and [Description] keywords and one or more [Interconnect Model] keywords and the [Interconnect Model] associated subparameters, as is listed in Table 40.

Table 40 – Interconnect Modeling Keywords and Subparameters

| **Keyword or Subparameter** | **Notes** |
| --- | --- |
| [Interconnect Model Set] |  |
| [Manufacturer] | (note 1) |
| [Description] | (note 1) |
| [Interconnect Model] | (note 2) |
| Param |  |
| File\_TS | (note 3) |
| File\_IBIS-ISS | (note 3) |
| Unused\_port\_termination | (note 4) |
| Number\_of\_terminals | (note 5) |
| <terminal line> | (note 6) |
| [End Interconnect Model] | (note 7) |
| [End Interconnect Model Set] | (note 8) |
| Note 1 [Manufacturer] and [Description] are each optional keywords within any [Interconnect Model Set].  Note 2 At least one [Interconnect Model] is required for each [Interconnect Model Set].  Note 3 One of either the File\_TS or File\_IBIS-ISS subparameters is required.  Note 4 This subparameter shall be followed by the “=” character and a numeric value (integers and reals are acceptable), with both optionally surrounded by whitespace.  Note 5 This subparameter shall be followed by the “=” character and an integer value, with both optionally surrounded by whitespace.  Note 6 See text below.  Note 7 Required when the [Interconnect Model] keyword is used  Note 8 Required when the [Interconnect Model Set] keyword is used | |

When Interconnect Model Set definitions occur within a .ibs file, their scope is “local”— they are known only within that .ibs file and no other .ibs file. In addition, within that .ibs file, they override any interconnect package models defined using the [Package], [Pin], or [Define Package Model] keywords. Interconnect Models in separate .ims files referenced by the [Interconnect Model Set Selector] keyword in a .ibs file also override any interconnect package models defined in the same .ibs file using the [Package], [Pin], or [Define Package Model] keywords.

Usage Rules for the .ims file:

Interconnect models are stored in a file whose name uses the format:

<base name>.ims

The <base name> provided shall adhere to the rules given in Section 3, “GENERAL SYNTAX RULES AND GUIDELINES“. Use the “ims” extension to identify files containing Interconnect Models. The .ims file shall contain the [IBIS Ver], [File Name], [File Rev], and the [End] keywords. Optional elements include the [Date], [Source], [Notes], [Disclaimer], [Copyright], and [Comment Char] keywords. All of these keywords and associated subparameters follow the same rules as those for a normal .ibs file.

Note that the [Component] and [Model] keywords are not allowed in the .ims file. The .ims file is for Interconnect Models only.

*Keyword:* [Interconnect Model Set]

*Required:* No

*Description:* Used to contain Interconnect Models

*Usage Rules:* [Interconnect Model Set] has a single argument, which is the name of the Interconnect Model Set. The length of the Interconnect Model Set name shall not exceed 40 characters in length. Blank characters are not allowed. The [Interconnect Model Set]/[End Interconnect Model Set] keyword pair is hierarchically equivalent in scope to [Component] and [Model].

The section under the [Interconnect Model Set] keyword may contain a [Manufacturer] keyword section and [Description] keyword section and shall contain one or more Interconnect Models. See the section [Interconnect Model] for a description of the content of each Interconnect Model.

Model makers are recommended to ensure that each Interconnect Model Set contains a complete description, through Interconnect Models, needed for the path connecting the I/O buffers of interest to their associated pins, and for connecting all rails related to these I/O buffers.  This simplifies choices to be made by the user or automatically by the EDA tool.  It also assures that the full electrical structure that is simulated matches what the model provider intends.  Some EDA tools may support selecting several Interconnect Model Sets at once to form a complete path, but this requires additional user interaction and may risk generating less-accurate simulation data due to duplicate or missing content.

*Example:*

[Interconnect Model Set] Signal\_Integrity

[Manufacturer] Acme Packaging, Inc.

[Description] This set contains one model for each I/O buffer

[Interconnect Model] DQ1

…

[End Interconnect Model]

[Interconnect Model] DQ2

…

[End Interconnect Model]

[Interconnect Model] DQS

…

[End Interconnect Model]

[End Interconnect Model Set]

*Keyword:* [Manufacturer]

*Required:* No

*Description:* Specifies the name of the [Interconnect Model Set] manufacturer.

*Usage Rules:* The length of the manufacturer’s name shall not exceed 40 characters (blank characters are allowed, e.g., Oklahoma Instruments).

*Example:*

[Manufacturer] NoName Corp.

*Keyword:* [Description]

*Required:* No

*Description:* Provides a concise yet easily human-readable description of what kind of interconnect the [Interconnect Model Set] represents.

*Usage Rules:* The description shall be less than 60 characters in length, shall fit on a single line, and may contain spaces.

*Example:*

[Description] 220-Pin Quad Ceramic Flat Pack

*Keyword:* [**End Interconnect Model Set**]

*Required:* Yes, for each instance of the [Interconnect Model Set] keyword.

*Descriptiofn:* Indicates the end of the Interconnect Model Set data.

*Example:*

[End Interconnect Model Set]

*Keyword:* [Interconnect Model]

*Required:* No

*Description:* Marks the beginning of an Interconnect Model description that is used to define the interfaces to IBIS-ISS subcircuit or Touchstone files.

*Sub-Params:* Unused\_port\_termination, Param, File\_TS, File\_IBIS-ISS, Number\_of\_terminals

*Usage Rules:* [Interconnect Model] has a single argument, which is the name of the associated Interconnect Model. The length of the Interconnect Model name shall not exceed 40 characters in length. Blank characters are not allowed. The [Interconnect Model]/[End Interconnect Model] keyword pair is hierarchically scoped by the [Interconnect Model Set]/[End Interconnect Model Set] keywords.

The [Interconnect Model]/[End Interconnect Model] section defines both the association between a Touchstone file or IBIS-ISS subcircuit and an Interconnect Model, as well as defining the terminals and terminal usage for the Interconnect Model in the context of the given [Component].

An [Interconnect Model] shall contain one and only one of the following combinations:

* pins and buffer terminals (full package model)
* pins and die pads (package only model)
* or die pads and buffer terminals (on-die interconnect model)

*Other Notes:* If a full package model contains an I/O pin terminal for a pin\_name then it shall also contain an I/O buffer terminal for the same pin\_name. If a package only model contains an I/O pin terminal for a pin\_name then it shall also contain an I/O die pad for the same pin\_name. If an on-die interconnect model contains an I/O buffer terminal for a pin\_name then it shall also contain an I/O die pad for the same pin\_name.

An Interconnect Model may contain only terminals to I/O buffer power rail terminals.

An Interconnect Model may contain terminals to one or more than one buffer I/O terminals.

An Interconnect Model may contain terminals to both I/O buffer power rail terminals and one or more than one buffer I/O terminals.

Each terminal of an Interconnect Model passes current to the simulation node it is connected to and has a “voltage”. This, as stated, is imprecise. Voltage, by definition, is a potential difference between two points. It is common to probe and plot the potential difference between simulator nodes at a terminal and the simulator ideal Node 0. This is valid for non-power aware simulations when the local ground (or return path) node is forced to Node 0 by the simulator, or for “ground referenced” power aware simulations that lump the effect of the ground interconnect into the power rails. However, this is not valid when the voltages of the ground nodes are “floating”. In this case it is important that the actual rail node that is the reference node for measurements at the I/O buffer is included as a terminal in the Interconnect Model. If this is not done, then the Interconnect Model will not correctly account for all return currents, particularly from capacitive elements. If an Interconnect Model does not contain a reference terminal, then the user of these models should be aware that using these models in non-ground referenced power aware simulations will introduce potential errors in simulations.

The following subparameters are defined:

Unused\_port\_termination = <value>

Param

File\_IBIS-ISS

File\_TS

Number\_of\_terminals = <value>

In addition to these subparameters, the [Interconnect Model]/[End Interconnect Model] section may contain lines describing terminals and their connections. No specific subparameter name, token, or other string is used to identify terminal lines.

Unless noted below, no Interconnect Model subparameter requires the presence of any other subparameter.

Unused\_port\_termination rules:

This optional subparameter defines the termination that is to be applied by the EDA tool during simulation to the terminals of any IBIS-ISS subcircuit or Touchstone network that is not being used in the [Interconnect Model]/[End Interconnect Model] group. The subparameter name shall be followed by a single integer argument greater than zero on the same line. The argument shall be separated from the subparameter name by the “=” character. The subparameter name, “=” character, and argument may optionally be separated by whitespace.

If this subparameter is present, the EDA tool should connect the unused terminals to GND through a resistorwith the value of resistance in ohms provided in the argument.

If this parameter is not defined, the EDA tool may connect terminals to terminations as needed to prevent numerical instability in simulation (EDA tools are recommended to alert users when this occurs and document the termination value used). Note that the terminals remain technically open, and terminations connected by the EDA tool are intended to approximate open-circuit conditions.

Only one Unused\_port\_termination subparameter may appear for a given [Interconnect Model] keyword.

Param rules:

The subparameter Param is optional and only legal with the File\_IBIS-ISS subparameter documented below. Param is illegal with the File\_TS subparameter documented below. Param shall be followed by three arguments: an unquoted string argument giving the name of the parameter to be passed into the IBIS-ISS subcircuit, a reserved word for the parameter format, and one numerical value or one string value (surrounded by double quotes) for the parameter value to be passed into the IBIS-ISS subcircuit.

The numerical value rules follow the scaling conventions in Section 3, “GENERAL SYNTAX RULES AND GUIDELINES”. The EDA tool is responsible for translating IBIS specified parameters into IBIS-ISS parameters. For example, 1 megaohm, would be represented as 1M in Param value according to the Section 3 rules, but would be converted by the EDA tool to case-insensitive 1meg (1X is not recommended) or 1E6 for IBIS-ISS use. Quoted string parameters in IBIS are converted to the string parameter syntax in IBIS-ISS subcircuits. For example, the Param value "typ.s2p" would be converted to str('typ.s2p') in IBIS-ISS subcircuits.

*Examples:*

| Param name format value

Param abc Value 2m | 2E-3 in IBIS

Param def Value 4k | 4E3 in IBIS

Param ts\_file Value "typ.s2p" | file name string passed

| into IBIS-ISS

File\_IBIS-ISS rules:

Either File\_IBIS-ISS or File\_TS is required for a [Interconnect Model]/[End Interconnect Model] group*.* The File\_IBIS-ISS subparameter is followed by two unquoted string arguments consisting of the file\_name and circuit\_name (.subckt name) for an IBIS-ISS file. The IBIS-ISS file under file\_name shall be located in the same directory as the referencing .ibs file or .ims file or in a directory under the referencing file as determined by the directory path.

*Example:*

| file\_type file\_name circuit\_name(.subckt name)

File\_IBIS-ISS net.iss netlist\_typ

File\_TS rules:

Either File\_TS or File\_IBIS-ISS is required for a [Interconnect Model]/[End Interconnect Model] group.File\_TS is followed by one unquoted string argument, which is the file name for a Touchstone file. The Touchstone file under file\_name shall be located in the same directory as the referencing .ibs file or .ims file or in a directory under the referencing file as determined by the directory path.

*Example:*

| file\_type file\_name

File\_TS typ.s8p

Number\_of\_terminals rules:

The Number\_of\_terminals subparameter is required and defines the number of terminals associated with the Interconnect Model. The subparameter name shall be followed by a single integer argument greater than zero on the same line. The argument shall be separated from the subparameter name by the “=” character. The subparameter name, “=” character, and argument may optionally be separated by whitespace. Only one Number\_of\_terminals subparameter may appear for a given [Interconnect Model] keyword. The Number\_of\_terminals subparameter shall appear before any terminal lines and after all other subparameters for a given Interconnect Model.

Terminal line rules:

Terminal lines shall appear after the Number\_of\_terminals subparameter and before the [End Interconnect Model] keyword. No token or reserved word identifies terminal lines.

Each terminal line contains information on a terminal of an IBIS-ISS subcircuit (or Touchstone file).

Terminal lines are of the following form, with each identifier separated by whitespace:

<Terminal\_number> <Terminal\_type> <Terminal\_type\_qualifier> <Qualifier\_entry> [Aggressor\_Only]

Terminal\_number

Terminal\_number is an identifier for a specific terminal. Terminal\_number shall be a positive non-zero integer less than or equal to the value of the Number\_of\_terminals argument. This value will also match the number of terminals used in an associated IBIS-ISS subcircuit, or the number of ports plus 1 (N+1) used in a corresponding associated Touchstone file. The same Terminal\_number shall not appear more than once for a given Interconnect Model. If any terminals are not present for a given Interconnect Model, then those terminals are unused, and shall be terminated according to the Unused\_port\_termination rules.

The Terminal\_number entry shall match the IBIS-ISS terminal (node) position or the Touchstone file terminal (line) position, plus an undeclared reference line. The Terminal\_number entries may be listed in any order as long as there are no duplicate entries.

Terminal\_type  
Terminal\_type is a string that identifies whether the terminal is a supply or I/O terminal and whether the terminal is connected at the buffer, die pad, or pin level (note that “I/O” in this context is a synonym for “signal”, as opposed to “supply”; it is not intended to imply model type as used in the “Model\_type” subparameter). Further, if the terminal is connected to a buffer supply rail, Terminal\_type identifies to which specific buffer rail the terminal is connected. Terminal\_type shall be one of the following:

* Pin\_I/O
* Pad\_I/O
* Buffer\_I/O
* Pin\_Rail
* Pad\_Rail
* Buffer\_Rail
* Pullup\_ref
* Pulldown\_ref
* Power\_clamp\_ref
* Gnd\_clamp\_ref
* Ext\_ref

Buffer\_I/O, Pullup\_ref, Pulldown\_ref, Power\_clamp\_ref, Gnd\_clamp\_ref, Ext\_ref and Buffer\_Rail are terminals of an Interconnect Model that connect directly to I/O buffers.

Pad\_I/O and Pad\_Rail are terminals that are at the die pad interface.

Pin\_I/O and Pin\_Rail are terminals that are at the pin interface that can connect the package to the PCB.

Terminal\_type\_qualifier   
Terminal\_type\_qualifier is a string that identifies the association between a terminal and a specific pin\_name, signal\_name, bus\_label, or pad\_name. Only certain Terminal\_types may be used with pad\_names, pin\_names, signal\_names, or bus\_labels respectively, as outlined in the Connecting Pins, Pads, and Buffer Terminals section below and summarized in Table 41.

Qualifier\_entry   
The <Qualifier\_entry>, shown in angle brackets, is the name required for the following Terminal\_type\_qualifiers:

pin\_name <pin\_name\_entry>

signal\_name <signal\_name\_entry>

bus\_label <bus\_label\_entry>

pad\_name <pad\_name\_entry>

Aggressor\_OnlyMulti-line models may describe only a subset of a coupled structure (e.g., a 64-line bus may be described by a four-line model). As a result, while the interconnects at the edges of the model may induce crosstalk onto other interconnects nearby, nearby, being on the edge of the model, they may not themselves experience the full crosstalk impact that the corresponding interconnect experiences in the real, full structure. The optional Aggressor\_Only column entry is allowed on all terminal locations for I/O terminals to indicate such incomplete coupling. Terminals that include the Aggressor\_Only entry may not be suitable to be simulated as victims, as they do not experience the full coupling present in the real physical structure. If an I/O terminal is not identified as Aggressor\_Only, then the interconnect to that I/O terminal includes coupling to all interconnections deemed necessary for coupled signal analysis. If a particular terminal is identified as Aggressor\_Only, then the entire path of the associated pin\_name is to be considered Aggressor\_Only.

Touchstone Files

For an Interconnect Model using File\_TS with N ports, N equals the number of ports present in the data of the associated Touchstone 1.x file, or the value associated with the [Number of Ports] keyword in the associated Touchstone 2 file. The Number\_of\_terminals entry in the Interconnect Model shall be an integer equal to N+1. Terminal rules are described below:

* The EDA tool shall use the pin\_name or signal\_name specified for the associated terminal “N+1” entry as the reference node for each of the N ports. For an Interconnect Model with N ports, the terminals and ports are associated as follows:
  + Terminal              Port
  + 1                              1
  + 2                              2
  + …
  + N                             N
  + N+1 reference
* Terminal N+1 shall be either directly connected to a pin with a signal\_name of POWER or GND, or connected to a pad or buffer terminal which is in turn connected to a pin with a signal\_name of POWER or GND.

The Terminal\_types Buffer\_I/O, Pad\_I/O and Pin\_I/O are used only for any single terminal of a buffer described by the [Model] keyword and for any Model\_type subparameter listed in Section 5, Table 1.  The Model\_types Series and \*\_diff are used for two-terminal configurations, and their terminals are described by two separate Buffer\_I/O, Pad\_I/O and Pin\_I/O Terminal\_type lines.

Connecting Pins, Pads and Buffer Terminals

Terminal lines describe the IBIS-ISS node or Touchstone port that each terminal should be connected to. Terminals may be at pins, die pads or the buffer. The arrangement of the terminal line entries (columns) is described below.

* The first column, Terminal\_number, contains an integer between 1 and the Number\_of\_terminals that describes the ordinal (positional) number of the IBIS-ISS node in the [Interconnect Model] subcircuit or Touchstone file port. The second column is Terminal\_type, the third column is Terminal\_type\_qualifier, the fourth column is Qualifier\_entry and there is an optional fifth column “Aggressor\_Only”
* The second column, Terminal\_type, determines if the terminal is at a pin, die pad or buffer.
  + For I/O connections
    - At pins, die pads or buffers
      * Terminal\_type can be Pin\_I/O, Pad\_I/O and Buffer\_I/O
      * Terminal\_type\_qualifier shall be pin\_name.
      * Qualifier\_entry shall be the pin\_name of an I/O pin.
  + For rail connections
    - At pins
      * Terminal\_type shall be Pin\_Rail
      * Terminal\_type\_qualifier shall be one of the following
        + pin\_name

Qualifier\_entry shall be a rail pin\_name

* + - * + signal\_name

Qualifier\_entry shall be a rail signal\_name

* + - * + bus\_label

Qualifier\_entry shall be a bus\_label

* + - At die pads
      * Terminal\_type shall be Pad\_Rail
      * Terminal\_type\_qualifier shall be
        + signal\_name

Qualifier\_entry shall be a rail signal\_name

* + - * + bus\_label

Qualifier\_entry shall be a bus\_label

* + - * + pad\_name

Qualifier\_entry shall be the pad\_name of a rail pad

* + - At buffers
      * Terminal\_type shall be Buffer\_Rail or any of the five \*\_ref terminals associated with an I/O buffer below
      * Buffer\_Rail Terminal\_type\_qualifier shall be
        + signal\_name

Qualifier\_entry shall be a rail signal\_name

* + - * + bus\_label

Qualifier\_entry shall be a bus\_label

* + - * Pullup\_ref, Pulldown\_ref, Power\_clamp\_ref, Gnd\_clamp\_ref or Ext\_ref Terminal\_type\_qualifiers shall be
        + pin\_name

Qualifier\_entry shall be the I/O buffer pin\_name

Table 41 summarizes the rules described above.

Table 41 – Allowed Terminal\_type Associations1

| **Terminal\_type** | **Terminal\_type\_qualifier** | | | | **Aggressor\_Only** |
| --- | --- | --- | --- | --- | --- |
| **pin\_name** | **signal\_name** | **bus\_label** | **pad\_name** |
| Pin\_I/O | X |  |  |  | A |
| Pad\_I/O | X |  |  |  | A |
| Buffer\_I/O | X |  |  |  | A |
| Pin\_Rail | Y | Y | Y |  |  |
| Pad\_Rail |  | Y | Y | Z |  |
| Buffer\_Rail |  | Y | Y |  |  |
| Pullup\_ref | X |  |  |  |  |
| Pulldown\_ref | X |  |  |  |  |
| Power\_clamp\_ref | X |  |  |  |  |
| Gnd\_clamp\_ref | X |  |  |  |  |
| Ext\_ref | X |  |  |  |  |

Notes

1. In the table, “X” refers to I/O pin names. “Y” and “Z” are POWER and GND names. The letter “A” designates "Aggressor\_Only".

Three classes of pins are defined for a component: signal pins, supply pins and no-connect pins. Supply pins have a model\_name of either POWER or GND. No-connect pins have model\_name NC. All other pins are classified as signal pins. Interconnect Models defined in this section assume that there is one Buffer\_I/O terminal and one die pad for each signal pin. Pins are assumed to use the names listed under the first column of the [Pin] keyword (the pin\_name column).

The model of an I/O buffer has supply terminals in addition to the Buffer\_I/O. These supply (or rail) terminals can be Pullup\_ref, Pulldown\_ref, Power\_clamp\_ref, Gnd\_clamp\_ref and/or Ext\_ref. The Pullup\_ref, Pulldown\_ref, Power\_clamp\_ref, Gnd\_clamp\_ref and/or Ext\_ref terminals of a buffer are associated either with a bus\_label under the [Pin Mapping] keyword or a signal\_name under the [Pin] keyword. These terminals can be connected to Interconnect Models one of two ways:

1. By specifying a unique interconnect terminal for each I/O buffer Pullup\_ref, Pulldown\_ref, Power\_clamp\_ref, Gnd\_clamp\_ref and/or Ext\_ref terminal
2. By assuming that all I/O buffer supply terminals connected to a supply signal\_name or bus\_label are shorted together. This is done by specifying a unique terminal (of Terminal\_type Buffer\_Rail) for all I/O buffer terminals that are connected to a specific signal\_name or bus\_label on at least one supply pin.

Pads are the location of the interface between the die and the package (also called the die pad interface). Interconnect Models can either be between the pins of a component and the I/O buffers, or they can be split into models between the pins of a component and the pads of the die and models between the pads of the die and the I/O buffers. There is exactly one Pad (of Terminal\_type Pad\_I/O) for each signal pin. There can be any number of pads (of Terminal\_type Pad\_Rail) for each signal\_name or bus\_label on supply pins. If Interconnect Models of supply (rail) networks are split between Pin/Pad and Pad/Buffer models, then the interface of supply connections at the die pad interface can be handled in one of two ways:

1. By defining a list of die supply pads, and specifying terminals for some or all of the die supply pads that are connected to a bus\_label or signal\_name on at least one supply pin.
2. By assuming that all supply pads connected to a supply signal\_name or bus\_label are shorted together. This is done by specifying a unique terminal (of Terminal\_type Pad\_Rail) for all pads that are connected to a specific signal\_name on at least one supply pin.

Pins may be terminals of the Interconnect Model that connect directly to a printed circuit board or other type of system connection to an IBIS component. Pins can be signal pins (Pin\_I/O), or supply pins (Pin\_Rail). An Interconnect Model can connect supply pins in one of two ways:

1. By specifying terminals for some or all of the supply pins.
2. By assuming that all supply pins connected to a supply signal\_name or bus\_label are shorted together. This is done by specifying a unique terminal (of Terminal\_type Pin\_Rail) for all pins that are connected to a specific signal\_name on at least one supply pin.

The terminals of an Interconnect Model may be located at pins and die pads, pins and buffers, or die pads and buffers. A single Interconnect Model shall not have terminals at pins, die pads and buffers simultaneously.

Any one pin shall not be included in more than one terminal of an Interconnect Model.

Any one die pad shall not be included in more than one terminal of an Interconnect Model.

Any one buffer terminal shall not be included in more than one terminal of an Interconnect Model.

*Examples:*

| All examples show a [Interconnect Model Set] under [Component] for

| complete grouping of the [Interconnect Model] descriptions

|

| Naming convention for [Interconnect Model Set] is below

| ([Interconnect Model] may show additional details)

|

| Full – Includes all I/O pins

| A1 or A1\_A3 – Designated pin or pins

| TS - Touchstone representation

| ISS - IBIS-ISS representation

| PDN - Includes power delivery network, can also be PU and PD

| IO - Only if modified differently than PDN below for buf\_pad\_pin

| buf\_pad\_pin – Includes models for buf\_pad, pad\_pin; if missing, buf\_pad

| sn - Uses signal\_name; if missing assumes pin\_name

| bl - Uses bus\_label; if missing assumes pin\_name

| pn - Uses pad\_name; if missing assumes pin\_name

| XTALK - Cross talk analysis (coupled nets may include Aggressor\_Only)

| Examples 1 – 11 apply to the configuration below:

[Pin] signal\_name model\_name      R\_pin   L\_pin   C\_pin

A1    DQ1         DQ

A2    DQ2         DQ

A3    DQ3         DQ

D1    DQS+        DQS

D2    DQS-        DQS

P1    VDD         POWER

P2    VDD         POWER

P3    VDD         POWER

P4    VDD         POWER

P5    VDD         POWER

G1    VSS         GND

G2    VSS         GND

G3    VSS         GND

G4    VSS         GND

[Diff Pin] inv\_pin  vdiff  tdelay\_typ tdelay\_min tdelay\_max

D1         D2       NA     NA         NA         NA

[Die Supply Pads]  signal\_name bus\_label

VDD1 VDD

VDD2 VDD

VDD3 VDD

VSS1 VSS

VSS2 VSS

[Pin Mapping] pulldown\_ref pullup\_ref gnd\_clamp\_ref power\_clamp\_ref ext\_ref

A1            VSS          VDD        NC            NC              NC

A2            VSS          VDD        NC            NC              NC

A3            VSS          VDD        NC            NC              NC

D1            VSS          VDD        NC            NC              NC

D2            VSS          VDD        NC            NC              NC

| Pins below are optional per [Pin Mapping] rules

P1 NC VDD

P2 NC VDD

P3 NC VDD

P4 NC VDD

P5 NC VDD

G1 VSS NC

G2 VSS NC

G3 VSS NC

G4 VSS NC

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 1: Terminals for full IBIS-ISS component with PDN, as depicted below.

[Interconnect Model Set] Ful1\_ISS\_PDN\_1

|-----

[Interconnect Model] Full\_ISS\_buf\_pin\_1

File\_IBIS-ISS full\_buf\_pin\_1.iss full\_buf\_pin\_typ

Number\_of\_terminals = 29

1  Pin\_I/O      pin\_name A1  |  DQ1         DQ

2  Pin\_I/O      pin\_name A2  |  DQ2         DQ

3  Pin\_I/O      pin\_name A3  |  DQ3         DQ

4  Pin\_I/O      pin\_name D1  |  DQS+        DQS

5  Pin\_I/O      pin\_name D2  |  DQS-        DQS

6  Pin\_Rail     pin\_name P1  |  VDD         POWER

7  Pin\_Rail     pin\_name P2  |  VDD         POWER

8  Pin\_Rail     pin\_name P3  |  VDD         POWER

9  Pin\_Rail     pin\_name P4  |  VDD         POWER

10 Pin\_Rail     pin\_name P5  |  VDD         POWER

11 Pin\_Rail    pin\_name G1  |  VSS         GND

12 Pin\_Rail     pin\_name G2  |  VSS         GND

13 Pin\_Rail     pin\_name G3  |  VSS         GND

14 Pin\_Rail     pin\_name G4  |  VSS         GND

15 Buffer\_I/O pin\_name A1  |  DQ1         DQ

16 Buffer\_I/O pin\_name A2  |  DQ2         DQ

17 Buffer\_I/O pin\_name A3  |  DQ3         DQ

18 Buffer\_I/O pin\_name D1  |  DQS+        DQS

19 Buffer\_I/O pin\_name D2  |  DQS-        DQS

20 Pullup\_ref pin\_name A1  |  DQ1         DQ

21 Pullup\_ref pin\_name A2  |  DQ2         DQ

22 Pullup\_ref pin\_name A3  |  DQ3         DQ

23 Pullup\_ref pin\_name D1  |  DQS+        DQS

24 Pullup\_ref pin\_name D2  |  DQS-        DQS

25 Pulldown\_ref pin\_name A1  |  DQ1         DQ

26 Pulldown\_ref pin\_name A2  |  DQ2         DQ

27 Pulldown\_ref pin\_name A3  |  DQ3         DQ

28 Pulldown\_ref pin\_name D1  |  DQS+        DQS

29 Pulldown\_ref pin\_name D2 |  DQS+        DQS

[End Interconnect Model]

[End Interconnect Model Set]



Figure 51 – Electrical Connections for Full Buffer Pin Model with Power Routing



Figure 52 – Electrical Terminals for Full Buffer Pin Model with Power Routing

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 2: Same as Example 1 except the PDN networks are simplified with

| signal\_name qualifiers to create a pair of POWER terminals and a pair

| of GND terminals

[Interconnect Model Set] Full\_ISS\_PDN\_sn\_2

|-----

[Interconnect Model] Full\_ISS\_buf\_pin\_2

File\_IBIS-ISS full\_buf\_pin.iss full\_buf\_pin\_2\_typ

Number\_of\_terminals = 14

1  Pin\_I/O      pin\_name A1    |  DQ1         DQ

2  Pin\_I/O      pin\_name A2    |  DQ2         DQ

3  Pin\_I/O      pin\_name A3    |  DQ3         DQ

4  Pin\_I/O     pin\_name D1    |  DQS+        DQS

5  Pin\_I/O     pin\_name D2    |  DQS-        DQS

|

| POWER and GND terminals with signal\_names

|

6  Pin\_Rail    signal\_name  VDD   |  VDD         POWER

7  Pin\_Rail     signal\_name   VSS   |  VSS         GND

|

8  Buffer\_I/O pin\_name A1    |  DQ1         DQ

9  Buffer\_I/O pin\_name A2    |  DQ2         DQ

10 Buffer\_I/O pin\_name A3    |  DQ3         DQ

11 Buffer\_I/O pin\_name D1    |  DQS+        DQS

12 Buffer\_I/O pin\_name D2    |  DQS-        DQS

|

| POWER and GND terminals with signal\_names

|

13 Buffer\_Rail signal\_name   VDD   |  VDD         POWER

14 Buffer\_Rail signal\_name   VSS   |  VSS         GND

|

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 3: Single I/O Touchstone connection with one extra terminal for the

| N+1 .s2p reference connection terminal

[Interconnect Model Set] A1\_TS

|-----

[Interconnect Model] A1\_TS\_buf\_pin

File\_TS dq\_ts\_buf\_pin.s2p

Number\_of\_terminals = 3

1 Pin\_I/O      pin\_name A1

2 Buffer\_I/O pin\_name A1

3 Pulldown\_ref pin\_name A1 | VSS reference for .s2p file

| Rail connections to Buffer\_I/O through

| [Pin Mapping] or a [Model] reference

| voltage used if no external rails

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 4: Single I/O pin documenting both IBIS-ISS and Touchstone files and

| showing that the Touchstone N+1 reference connection is to the VSS rail

[Interconnect Model Set] A1\_IBIS\_ISS\_buf\_pad\_pin

|-----

[Interconnect Model] A1\_TS\_pad\_pin

File\_TS dq\_ts\_buf\_pad.s2p

Number\_of\_terminals = 3

1 Pin\_I/O     pin\_name A1

2 Pad\_I/O     pad\_name A1

3 Pin\_Rail signal\_name VSS | VSS reference for .s2p file

| | Requires Pin\_Rail VSS connection

[End Interconnect Model]

[Interconnect Model] A1\_ISS\_buf\_pad

File\_IBIS-ISS dq\_iss\_pad\_pin.iss DQ\_pad\_pin\_typ

Number\_of\_terminals = 3

1 Pad\_I/O      pin\_name A1

2 Buffer\_I/O pin\_name A1

3 Pulldown\_ref pin\_name A1 | A reference terminal for capacitor

| connection

| If missing a Node 0 might be used with

| reduced accuracy

|

| [Pin Mapping] connections used to connect external rails, or default

| internal [Model] rails used if no external rails

|

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 5: Full I/O IBIS-ISS configuration with PDN terminals

| under separate [Interconnect Model]s

[Interconnect Model Set] Full\_ISS\_PDN\_3

|-----

[Interconnect Model] Full\_ISS\_buf\_pin\_IO

File\_IBIS-ISS full\_buf\_pin.iss full\_buf\_pin\_typ

Number\_of\_terminals = 11

1  Pin\_I/O      pin\_name A1  |  DQ1         DQ

2  Pin\_I/O      pin\_name A2  |  DQ2         DQ

3  Pin\_I/O      pin\_name A3  |  DQ3         DQ

4  Pin\_I/O      pin\_name D1  |  DQS+        DQS

5  Pin\_I/O      pin\_name D2  |  DQS-        DQS

6 Buffer\_I/O  pin\_name A1  |  DQ1         DQ

7 Buffer\_I/O  pin\_name A2  |  DQ2         DQ

8 Buffer\_I/O  pin\_name A3  |  DQ3         DQ

9 Buffer\_I/O  pin\_name D1  |  DQS+        DQS

10 Buffer\_I/O  pin\_name D2  |  DQS-        DQS

11 Pin\_Rail signal\_name VSS | Reference at the Pin\_Rail

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pin\_PDN\_1

File\_IBIS-ISS full\_ISS\_buf\_pin\_pdn.iss full\_buf\_pin\_PDN\_typ

Number\_of\_terminals = 19

1  Pin\_Rail    pin\_name P1  |  VDD         POWER

2 Pin\_Rail    pin\_name P2  |  VDD         POWER

3  Pin\_Rail    pin\_name P3  |  VDD         POWER

4  Pin\_Rail    pin\_name P4  |  VDD         POWER

5 Pin\_Rail    pin\_name P5  |  VDD         POWER

6 Pullup\_ref  pin\_name A1  |  DQ1         DQ

7 Pullup\_ref  pin\_name A2  |  DQ2         DQ

8 Pullup\_ref  pin\_name A3  |  DQ3         DQ

9 Pullup\_ref  pin\_name D1  |  DQS+        DQS

10 Pullup\_ref  pin\_name D2  |  DQS-        DQS

11 Pin\_Rail    pin\_name G1  |  VSS         GND

12 Pin\_Rail   pin\_name G2  |  VSS         GND

13 Pin\_Rail   pin\_name G3  |  VSS         GND

14 Pin\_Rail   pin\_name G4  |  VSS         GND

15 Pulldown\_ref pin\_name A1  |  DQ1         DQ

16 Pulldown\_ref pin\_name A2  |  DQ2         DQ

17 Pulldown\_ref pin\_name A3  |  DQ3         DQ

18 Pulldown\_ref pin\_name D1  |  DQS+        DQS

19 Pulldown\_ref pin\_name D2  |  DQS-        DQS

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 6: Full IBIS-ISS IOs and separate PDNs, all with buf\_pad and

| pad\_pin [Interconnect Model]s

[Interconnect Model Set] Full\_ISS\_buf\_pad\_pin\_PDN\_4

|-----

[Interconnect Model] Full\_ISS\_pad\_pin\_IO

File\_IBIS-ISS full\_pad\_pin\_io.iss full\_pad\_pin\_IO\_typ

Number\_of\_terminals = 11

1  Pin\_I/O      pin\_name A1  |  DQ1         DQ

2  Pin\_I/O     pin\_name A2  |  DQ2         DQ

3  Pin\_I/O     pin\_name A3  |  DQ3         DQ

4  Pin\_I/O     pin\_name D1  |  DQS+        DQS

5  Pin\_I/O     pin\_name D2  |  DQS-        DQS

|

6 Pad\_I/O  pin\_name A1  |  DQ1         DQ

7 Pad\_I/O  pin\_name A2  |  DQ2         DQ

8 Pad\_I/O  pin\_name A3  |  DQ3         DQ

9 Pad\_I/O  pin\_name D1  |  DQS+        DQS

10 Pad\_I/O  pin\_name D2  |  DQS-        DQS

11 Buffer\_Rail signal\_name VSS | Reference for I/Os

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pad\_IO

File\_IBIS-ISS full\_buf\_pad\_io.iss full\_buf\_pad\_IO\_typ

Number\_of\_terminals = 11

1  Pad\_I/O      pin\_name A1  |  DQ1         DQ

2  Pad\_I/O      pin\_name A2  |  DQ2         DQ

3  Pad\_I/O      pin\_name A3  |  DQ3         DQ

4  Pad\_I/O     pin\_name D1  |  DQS+        DQS

5  Pad\_I/O      pin\_name D2  |  DQS-        DQS

|

6 Buffer\_I/O  pin\_name A1  |  DQ1         DQ

7 Buffer\_I/O  pin\_name A2  |  DQ2         DQ

8 Buffer\_I/O  pin\_name A3  |  DQ3         DQ

9 Buffer\_I/O  pin\_name D1  |  DQS+        DQS

10 Buffer\_I/O  pin\_name D2  |  DQS-        DQS

11 Pin\_Rail signal\_name VSS | Reference for I/Os

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_pad\_pin\_PDN

File\_IBIS-ISS full\_iss\_pad\_pin\_pdn.iss full\_iss\_pad\_pin\_PDN\_typ

Number\_of\_terminals = 14

1  Pin\_Rail pin\_name P1    |  VDD         POWER

2 Pin\_Rail pin\_name P2    |  VDD         POWER

3  Pin\_Rail pin\_name P3    |  VDD         POWER

4  Pin\_Rail pin\_name P4    |  VDD         POWER

5 Pin\_Rail pin\_name P5    |  VDD         POWER

|

6 Pad\_Rail pad\_name VDD1 |  VDD         POWER

7 Pad\_Rail pad\_name VDD2 |  VDD         POWER

8 Pad\_Rail pad\_name VDD3 |  VDD         POWER

|

9  Pin\_Rail pin\_name G1   |  VSS         GND

10 Pin\_Rail pin\_name G2   |  VSS         GND

11 Pin\_Rail pin\_name G3   |  VSS         GND

12 Pin\_Rail pin\_name G4   |  VSS         GND

|

13 Pad\_Rail pad\_name VSS1 |  VSS         GND

14 Pad\_Rail pad\_name VSS2 |  VSS         GND

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pad\_PDN

File\_IBIS-ISS full\_iss\_buf\_pad\_pdn.iss full\_iss\_buf\_pad\_PDN\_typ

Number\_of\_terminals = 15

1 Pad\_Rail pad\_name VDD1 |  VDD         POWER

2 Pad\_Rail pad\_name VDD2 |  VDD         POWER

3 Pad\_Rail pad\_name VDD3 |  VDD         POWER

|

4 Pullup\_ref  pin\_name A1   |  DQ1         DQ

5 Pullup\_ref  pin\_name A2   |  DQ2         DQ

6 Pullup\_ref  pin\_name A3   |  DQ3         DQ

7 Pullup\_ref  pin\_name D1   |  DQS+        DQS

8 Pullup\_ref  pin\_name D2   |  DQS-        DQS

|

9 Pad\_Rail pad\_name VSS1 |  VSS         GND

10 Pad\_Rail pad\_name VSS2 |  VSS         GND

|

11 Pulldown\_ref pin\_name A1   |  DQ1         DQ

12 Pulldown\_ref pin\_name A2   |  DQ2         DQ

13 Pulldown\_ref pin\_name A3   |  DQ3         DQ

14 Pulldown\_ref pin\_name D1    |  DQS+        DQS

15 Pulldown\_ref pin\_name D2    |  DQS-        DQS

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 7: Full IBIS-ISS model with I/O only [Interconnect Model] and a

| separate PDN [Interconnect Model] with signal\_name qualifiers

[Interconnect Model Set] Full\_ISS\_PDN\_sn\_5

|-----

[Interconnect Model] Full\_ISS\_buf\_pin\_IO

File\_IBIS-ISS full\_buf\_pin.iss full\_buf\_pin\_typ

Number\_of\_terminals = 11

1 Pin\_I/O pin\_name A1 | DQ1 DQ

2 Pin\_I/O pin\_name A2 | DQ2 DQ

3 Pin\_I/O pin\_name A3 | DQ3 DQ

4 Pin\_I/O pin\_name D1 | DQS+ DQS

5 Pin\_I/O pin\_name D2 | DQS- DQS

6 Buffer\_I/O pin\_name A1 | DQ1 DQ

7 Buffer\_I/O pin\_name A2 | DQ2 DQ

8 Buffer\_I/O pin\_name A3 | DQ3 DQ

9 Buffer\_I/O pin\_name D1 | DQS+ DQS

10 Buffer\_I/O pin\_name D2 | DQS- DQS

11 Pin\_Rail signal\_name VSS | Reference at the Pin\_Rail

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pin\_PDN\_2

File\_IBIS-ISS full\_iss\_buf\_pin\_pdn\_2.iss full\_iss\_buf\_pad\_PDN\_2

Number\_of\_terminals = 4

1  Pin\_Rail     signal\_name VDD  |  VDD         POWER

2 Buffer\_Rail signal\_name VDD  | VDD         POWER

3  Pin\_Rail     signal\_name VSS  |  VSS         GND

4 Buffer\_Rail signal\_name VSS  |  VSS         GND

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 8: Same full IBIS-ISS model with PDN as in Example 7, but with the

| [Interconnect Model]s describing buf\_pad and pad\_pin connections

| separately

[Interconnect Model Set] Full\_ISS\_buf\_pad\_pin\_PDN\_sn\_6

|-----

[Interconnect Model] Full\_ISS\_pad\_pin\_IO

File\_IBIS-ISS full\_pad\_pin\_io.iss full\_pad\_pin\_IO\_typ

Number\_of\_terminals = 11

1 Pin\_I/O pin\_name A1 | DQ1 DQ

2 Pin\_I/O pin\_name A2 | DQ2 DQ

3 Pin\_I/O pin\_name A3 | DQ3 DQ

4 Pin\_I/O pin\_name D1 | DQS+ DQS

5 Pin\_I/O pin\_name D2 | DQS- DQS

|

6 Pad\_I/O pin\_name A1 | DQ1 DQ

7 Pad\_I/O pin\_name A2 | DQ2 DQ

8 Pad\_I/O pin\_name A3 | DQ3 DQ

9 Pad\_I/O pin\_name D1 | DQS+ DQS

10 Pad\_I/O pin\_name D2 | DQS- DQS

11 Buffer\_Rail signal\_name VSS | Reference for I/Os

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pad\_IO

File\_IBIS-ISS full\_buf\_pad\_io.iss full\_buf\_pad\_IO\_typ

Number\_of\_terminals = 11

1 Pad\_I/O pin\_name A1 | DQ1 DQ

2 Pad\_I/O pin\_name A2 | DQ2 DQ

3 Pad\_I/O pin\_name A3 | DQ3 DQ

4 Pad\_I/O pin\_name D1 | DQS+ DQS

5 Pad\_I/O pin\_name D2 | DQS- DQS

|

6 Buffer\_I/O pin\_name A1 | DQ1 DQ

7 Buffer\_I/O pin\_name A2 | DQ2 DQ

8 Buffer\_I/O pin\_name A3 | DQ3 DQ

9 Buffer\_I/O pin\_name D1 | DQS+ DQS

10 Buffer\_I/O pin\_name D2 | DQS- DQS

11 Pin\_Rail signal\_name VSS | Reference for I/Os

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_pad\_pin\_PDN\_3

File\_IBIS-ISS full\_iss\_pad\_pin\_pdn\_3.iss full\_iss\_pad\_pin\_pdn\_3

Number\_of\_terminals = 4

1  Pin\_Rail     signal\_name VDD  |  VDD         POWER

2 Pad\_Rail     signal\_name VDD  |  VDD         POWER

3  Pin\_Rail     signal\_name VSS  |  VSS         GND

4 Pad\_Rail     signal\_name VSS  |  VSS         GND

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pad\_PDN\_3

File\_IBIS-ISS full\_iss\_buf\_pad\_pdn\_3.iss full\_iss\_buf\_pad\_pdn\_3

Number\_of\_terminals = 4

1  Buffer\_Rail  signal\_name VDD  |  VDD         POWER

2 Pad\_Rail     signal\_name VDD  |  VDD         POWER

3  Buffer\_Rail  signal\_name VSS  |  VSS         GND

4 Pad\_Rail     signal\_name VSS  |  VSS         GND

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 9: Same full IBIS-ISS configuration with PDN as in Example 8, except

| that I/O connections are direct from buf\_pin while the PDN connections are

| from buf\_pad and pad\_pin using the signal\_name qualifier

[Interconnect Model Set] Full\_ISS\_IO\_buf\_pad\_pin\_PDN\_sn\_7

|-----

[Interconnect Model] Full\_ISS\_buf\_pin\_IO

File\_IBIS-ISS full\_buf\_pin.iss full\_buf\_pin\_typ

Number\_of\_terminals = 11

1 Pin\_I/O pin\_name A1 | DQ1 DQ

2 Pin\_I/O pin\_name A2 | DQ2 DQ

3 Pin\_I/O pin\_name A3 | DQ3 DQ

4 Pin\_I/O pin\_name D1 | DQS+ DQS

5 Pin\_I/O pin\_name D2 | DQS- DQS

6 Buffer\_I/O pin\_name A1 | DQ1 DQ

7 Buffer\_I/O pin\_name A2 | DQ2 DQ

8 Buffer\_I/O pin\_name A3 | DQ3 DQ

9 Buffer\_I/O pin\_name D1 | DQS+ DQS

10 Buffer\_I/O pin\_name D2 | DQS- DQS

11 Pin\_Rail signal\_name VSS | Reference at the Pin\_Rail

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_pad\_pin\_PDN\_3

File\_IBIS-ISS full\_iss\_pad\_pin\_pdn\_3.iss full\_iss\_pad\_pin\_pdn\_3

Number\_of\_terminals = 4

1 Pin\_Rail signal\_name VDD | VDD POWER

2 Pad\_Rail signal\_name VDD | VDD POWER

3 Pin\_Rail signal\_name VSS | VSS GND

4 Pad\_Rail signal\_name VSS | VSS GND

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pad\_PDN\_3

File\_IBIS-ISS full\_iss\_buf\_pad\_pdn\_3 full\_iss\_buf\_pad\_pdn\_3

Number\_of\_terminals = 4

1 Buffer\_Rail signal\_name VDD | VDD POWER

2 Pad\_Rail signal\_name VDD | VDD POWER

3 Buffer\_Rail signal\_name VSS | VSS GND

4 Pad\_Rail signal\_name VSS | VSS GND

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 10: Terminals A1\_A3 set up for and IBIS-ISS connections with coupling

| for cross-talk analysis – Aggressor\_Only terminals at the Buffer are

| designated

[Interconnect Model Set] A1\_A3\_DQ\_TS\_XTALK

|-----

[Interconnect Model] A1\_A3\_DQ\_TS\_buf\_pin\_XTALK

File\_TS dq\_iss\_buf\_pin\_xtalk.s6p

Number\_of\_terminals = 7

1 Pin\_I/O     pin\_name A1 Aggressor\_Only

2 Buffer\_I/O pin\_name A1 Aggressor\_Only

3 Pin\_I/O     pin\_name A2

4 Buffer\_I/O pin\_name A2

5 Pin\_I/O     pin\_name A3 Aggressor\_Only

6 Buffer\_I/O pin\_name A3 Aggressor\_Only

7 Pulldown\_ref pin\_name A1 | Reference Node

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 11: Same as Example 10, but with a PDN network added

[Interconnect Model Set] A1\_A3\_DQ\_TS\_XTALK\_ISS\_PDN

|-----

[Interconnect Model] A1\_A3\_DQ\_TS\_buf\_pin\_XTALK

File\_TS dq\_iss\_buf\_pin\_xtalk.s6p

Number\_of\_terminals = 7

1 Pin\_I/O pin\_name A1 Aggressor\_Only

2 Buffer\_I/O pin\_name A1 Aggressor\_Only

3 Pin\_I/O pin\_name A2

4 Buffer\_I/O pin\_name A2

5 Pin\_I/O pin\_name A3 Aggressor\_Only

6 Buffer\_I/O pin\_name A3 Aggressor\_Only

7 Pulldown\_ref pin\_name A1 | Reference Node

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pin\_PDN\_2

File\_IBIS-ISS full\_iss\_buf\_pin\_pdn\_2.iss full\_iss\_buf\_pad\_PDN\_2

Number\_of\_terminals = 4

1 Pin\_Rail signal\_name VDD | VDD POWER

2 Buffer\_Rail signal\_name VDD | VDD POWER

3 Pin\_Rail signal\_name VSS | VSS GND

4 Buffer\_Rail signal\_name VSS | VSS GND

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 12 applies to the configuration below

[Pin] signal\_name model\_name      R\_pin   L\_pin   C\_pin

A1    DQ1         DQ

A2    DQ2         DQ

A3    DQ3         DQ

A4    DQ4         DQ

P1    VDD         POWER

P2    VDD         POWER

G1    VSS         GND

G2    VSS         GND

[Bus Label] signal\_name

VDD1 VDD

VDD2 VDD

[Pin Mapping] pulldown\_ref pullup\_ref gnd\_clamp\_ref power\_clamp\_ref ext\_ref

A1            VSS           VDD1        NC            NC              NC

A2            VSS           VDD1        NC            NC              NC

A3            VSS           VDD2        NC            NC              NC

A4            VSS           VDD2        NC            NC              NC

| Entries below may optionally be deleted and replaced with [Bus Label] per

| [Bus Label] and [Pin Mapping] rules

P1            NC           VDD1        NC            NC              NC

P2            NC           VDD2        NC            NC              NC

G1            VSS           NC         NC            NC              NC

G2            VSS           NC         NC            NC              NC

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 12: Full IBIS-ISS configuration with PDN described using both

| bus\_label and signal\_name qualifiers for the Rails

[Interconnect Model Set] Full\_ISS\_IO\_PDN\_bl\_sn\_6

|-----

[Interconnect Model] Full\_ISS\_buf\_pin\_IO\_4

File\_IBIS-ISS full\_iss\_buf\_pin\_io\_4.iss full\_iss\_buf\_pin\_IO\_4\_typ

Number\_of\_terminals = 9

1  Pin\_I/O     pin\_name A1  |  DQ1         DQ

2  Pin\_I/O      pin\_name A2  |  DQ2         DQ

3  Pin\_I/O     pin\_name A3  |  DQ3         DQ

4  Pin\_I/O     pin\_name A4  |  DQ4         DQ

5 Buffer\_I/O pin\_name A1  |  DQ1         DQ

6 Buffer\_I/O pin\_name A2  |  DQ2         DQ

7 Buffer\_I/O pin\_name A3  |  DQ3         DQ

8 Buffer\_I/O pin\_name A4  |  DQ4         DQ

9 Pin\_Rail signal\_name VSS | Reference for I/Os

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_PDN\_bl\_sn

File\_IBIS-ISS buf\_pin\_pdn.iss buf\_pin\_PDN\_typ

Number\_of\_terminals = 5

1  Pin\_Rail     signal\_name VDD  |  VDD         POWER

2  Pin\_Rail     signal\_name VSS  |  VSS         GND

|

3 Buffer\_Rail bus\_label VDD1  |  VDD         POWER

4 Buffer\_Rail bus\_label VDD2  |  VDD         POWER

5 Buffer\_Rail signal\_name VSS  |  VSS         GND

[End Interconnect Model]

[End Interconnect Model Set]

| The EDA tool connects the terminals and pins as follows:

|

| 1 Pins P1 and P2

| 2 Pins G1 and G2

| 3 Pullup\_ref of buffers A1 and A2

| 4 Pullup\_ref of buffers A3 and A4

| 5 Pulldown\_ref of buffers A1, A2, A3 and A4

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

*Keyword:* [**End Interconnect Model**]

*Required:* Yes, for each instance of the [Interconnect Model] keyword

*Description:* Indicates the end of the Interconnect Model data.

*Example:*

[End Interconnect Model]